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In this advanced card you get a professional quality computer that meets today's engineering needs. And it's one that's complete. It lets you be up and running fast. All you need is a power supply and your ROM software.

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Besides all these features the Cromemco single card computer gives you enormous expandability if you ever need it. And it's easy to expand. First, you can expand with the new Cromemco 32K BYTESAVER PROM card mentioned above. Then there's Cromemco's broad line of 5100-bus-compatible memory and I/O interface cards. Cards with features such as relay interface, analog interface, graphics interface, optoisolator input, and A/D and D/A conversion. RAM and ROM cards, too.

EASY TO USE
Another convenience that makes the Model SCC computer easy to use is our Z-80 monitor and 3K Control BASIC (in two ROMs). With this optional software you're ready to go. The monitor gives you 12 commands. The BASIC, with 36 commands/functions, will directly access I/O ports and memory locations — and call machine language subroutines.

Finally, to simplify things to the ultimate, we even have convenient card cages. Rugged card cages. They hold cards firmly. No jiggling out of sockets.

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The Cromemco Model SCC is available now at a low price of only $450 factory assembled ($395 kit). So act today. Get this high-capability computer working for you right away.

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Your range of choice includes our advanced System Three with up to four 8" disk drives. Or choose from the System Two and Z-20 with 5" drives. Then for ROM-based work there’s the Z2. Each of these computers further offers up to 1/2 megabyte of RAM (or ROM).

We say these are the industry’s most professional microcomputers because they have outstanding features like these:

- **Z-80A microprocessor** — operates at 250 nano second cycle time — nearly twice the speed of most others.

  "Rated in *The 1977 Computer Store Survey* by Image Resources, Westlake Village, CA.

- Up to 512 kilobytes of RAM and 1 megabyte of disk storage

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- 21 card slots to allow for unparalleled system expansion using industry-standard S-100 cards.

- S-100 bus — don’t overlook how important this is. It has the industry’s widest support and Cromemco has professionally implemented it in a fully-shielded design.

- Cromemco card support of more than a dozen circuit cards for process control, business systems, and data acquisition including cards for A-D and D-A conversion, for interfacing daisy-wheel or dot-matrix printers, even a card for programming PROMs.

- The industry’s most professional software support, including COBOL, FORTRAN IV, 16K Disk-Extended BASIC, Z-80 Macro Assembler, Cromemco Multi-User Operating System, Data Base Management System, Word Processing System — and more coming.

- Rugged, professional all-metal construction for rack (or bench or floor cabinet) mounting. Cabinets available.

FOR TODAY AND TOMORROW

Cromemco computers will meet your needs now and in the future because of their unquestioned technical leadership, professionalism and enormous expandability.

See them today at your dealer. There’s no substitute for getting the best.
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The advent of the personal computer has made possible the calculation of the fast Fourier transform (FFT) on the small system. Applications of this powerful design tool include speech and music analysis as well as circuit design and development. Read Fast Fourier Transforms on Your Home Computer by William D Stanley and Steven J Peterson. page 14

Quite often a software approach to a problem is easier to implement than a hardware approach to the same problem. Tom Munnecke describes the software used in Designing a Universal Turing Machine and compares it to a comparable hardware approach. page 26

Steve Garcia describes a simple but useful addition to your computer in Build an Octal/Hexadecimal Output Display. This circuit can help you to convert from octal to hexadecimal (and vice versa) or give you the status of a byte during program execution. page 32

Our cover theme this month (painted by Robert Tinney) is the game of Life. In Life with Your Computer, Justin Millen, Judy Reardon and Peter Smart give a starting point for developing your own version of this exciting game. page 45

Researchers probing cellular automata have used Conway's game of Life as a tool in creating a collection of strange and exciting patterns. In David Buckingham's article Some Facts of Life we find a description of discoveries made since the original flurry of activity several years ago. page 54

One-Dimensional Life is an intriguing variant on John Conway's famous game. Out of this restricted format comes a surprising variety of familiar Life figures such as the flip flop and glider. Dr Jonathan K Millen leads us down the Life line in One-Dimensional Life. page 68

The same folks who brought you Chess 4.6 now bring you a new, improved version, Chess 4.7. Read the story of the epic battle of the mighty computer and the tenacious, clever human chess master in an article by J R Douglas, Chess 4.7 versus David Levy. page 84

In many microcomputer applications it is desirable to have a cheap method for printing numerical data. Robert H Astmann describes a way to interface a Texas Instruments 5050M printing calculator to an 8080A based computer in Interface Your Computer to a Printing Calculator. page 94

In This BYTE

When building a computer system it is frequently advisable to have your most often used basic routines stored in read only memory so that they will always be readily available. To make the best use of read only memory, the experimenter should be able to program his own. G H Gable describes one system for programming read only memory in his article, Zapper: A Computer Driven ER0M Programmer. page 100

Are you having trouble affording enough hardware to support a high level language such as BASIC? Are you finding it difficult to program in your machine's assembler language? If your answer to either of those questions is "yes," then what you're looking for is An Easy Programming System. In this article, Joe Weisbecker gives an introduction to hexadecimal interpretive programming, an alternative to high level languages and assemblers alike. page 108

Computer aided instruction is an excellent microcomputer application. To perform this function correctly, it helps to have a programming language designed for the purpose. Prof George A Gerhold describes some of the features such a language should possess in Teaching with a Microcomputer. page 124

If you have a need for multiplication and division circuits and don't want to worry about timing circuits, read Mike Weed's discussion of some Clockless Multiplication and Division Circuits you can work with. page 128

This month we present the second half of Chess 0.5 in the series Creating a Chess Player by Peter W Frey and Larry R Atkin. The program was written by Larry Atkin, who is co-author with David Slate of the world championship computer chess program, Chess 4.6. The program is written in Pascal and is readily adaptable to personal computers having Pascal systems such as the UCSD Pascal project software. page 140

To get the most out of your floppy disk units, you should know how to handle the data that will be stored on them efficiently. A I Halsema introduces us to the concept of Partitioned Data Sets and briefly describes a method for implementing them. page 168

What is the world going to be like in twenty years? That's a difficult question to answer, but the chances are that microcomputers will be part of it. Lawrence Willard takes a light-hearted look at one possible future in his story, The Mother Chip. page 186

FORTRAN is one of the antecedents to a number of computer languages. The ever popular BASIC is in some respects a simplification of FORTRAN. A number of later languages build upon the computer science learning experience which was FORTRAN and its compilers in the late 1950s and early 1960s. FORTRAN is even now becoming available in floppy disk based systems at the high end of the personal computing performance range. In this issue, W Douglas Maurer provides readers with an article on FORTRAN and Its Generalizations, good background reading on an important and still much used language. page 194
New from North Star
Double Density Performance at Single Density Prices

The new HORIZON computer and Micro Disk System now record in double density! That means each new Shugart SA-400 minifloppy disk drive accesses 180K bytes of on-line information. All double density HORIZON computers and Micro Disk Systems have a redesigned controller which allows the use of quadruple capacity disk drives as they become available in early 1979. A three-drive North Star System with quadruple capacity disk drives will access over a megabyte of on-line information. But, best of all there's no price increase for double density models.

North Star BASIC and DOS have been upgraded to accommodate the increased capacity and yet run existing programs with little or no change. The new disk system also supports single density, so existing single density diskettes can still be used. Single density SA-400 drives previously purchased with North Star systems can also be used.

Pricing
HORIZON with one double density SA-400 minifloppy (180K bytes), 16K RAM, Z80A processor and serial I/O port: $1599 kit, $1899 assembled.
MICRO DISK SYSTEM with one double density SA-400 minifloppy, controller board and power regulation: $699 kit, $799 assembled. (Cabinet and power supply $39 extra each.)

North Star Computers
2547 Ninth Street
Berkeley, California 94710
(415) 549-0858

Specifications:
S-100 compatible. MFM encoding, 35 tracks with ten 512-byte sectors per track. 179,200 bytes on double density SA-400 and North Star BASIC, DOS, and Monitor included.

For further information, write for full color catalog or contact your local computer store.
New Wonders of the Computer Age

by Carl Helmers

In recent months, trends in the development of integrated circuit technology have reached new heights of accomplishment, such that it is possible to note some exciting possibilities for design in the next year or so. These new highs are on a broad front of semiconductor technology which is required for the small computers our readers buy and use. The effects of this new technology may not be seen in the retail marketplace for another year or so, since there is a finite delay design time between the availability of a part's design specification and its appearance in finished products.

The first new high in semiconductor technology is the announcement of several new 64 K bit dynamic memory parts (see the Texas Instruments TMS 4164 described on page 209 of this issue). What are the implications of this technology for personal computers? Quite simply, they are new low prices for the same functions we see now in the marketplace. Eventually the prices of the 64 K parts will fall to the under $20 level now seen in 16 K chips purchased in volume. Where it once took 32 chips of 16 K bits per chip to saturate a personal computer's address space, it will now take only eight chips (and perhaps a dynamic memory controller chip) to do the same thing. It is now possible to combine a current model microprocessor, a video controller chip, a dynamic memory interface chip, a floppy disk controller chip, and one or two parallel interface chips with eight memory chips and obtain a very complete electronics module for a small computer that uses only 13 or 14 integrated circuits, yet has the performance of a large scale minicomputer of several years ago. In short, the memory address...
The small computer that won't fence you in.

A lot of semantic nonsense is being tossed around by some of the makers of so-called "personal" computers. To hear them tell it, an investment of a few hundred dollars will give you a computer to run your small business, do financial planning, analyze data in the engineering or scientific lab — and when day is done play games by the hour.

Well, the game part is true. The rest of the claims should be taken with a grain of salt. Only a few personal computers have the capacity to grow and handle meaningful work in a very real sense. And they don't come for peanuts.

**Remember, there's no free lunch.**

So before you buy any personal computer, consider Sol®. It costs more at the start but less in the end. It can grow with your ability to use it. Sol is not cheap. But it's not a delusion either.

Sol small computers are at the very top of the microcomputer spectrum. They stand up to the capabilities of mini systems costing four times as much.

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**Build computer power with our software.**

At Processor Technology we've tailored a group of high-level languages, an assembler and other packages to suit the wide capabilities of our hardware.

Our exclusive Extended BASIC is a fine example. This BASIC features complete matrix functions. It comes on cassette or in a disk version which has random as well as sequential files.

Processor Technology FORTRAN is similar to FORTRAN IV and has a full set of extensions designed for the "stand alone" computer environment.

Our PILOT is an excellent text oriented language for teachers.

**Sold and serviced only by the best dealers.**

Sol Systems are sold and serviced by an outstanding group of conveniently located computer stores throughout the U.S. and Canada.

For more information contact your nearest dealer in the adjacent list. Or write Department B, Processor Technology, 7100 Johnson Industrial Drive, Pleasanton, CA 94566. Phone (415) 829-2600.

**In sum, all small computers are not created equal and Sol users know it to their everlasting satisfaction.**

ProcessorTechnology
Why Apple II is the world's best selling personal computer.

Which personal computer will be most enjoyable and rewarding for you? Since we delivered our first Apple® II in April, 1977, more people have chosen our computer than all other personal computers combined. Here are the reasons Apple has become such an overwhelming favorite.

Apple is a fully tested and assembled mainframe computer. You won't need to spend weeks and months in assembly. Just take an Apple home, plug it in, hook up your color TV* and any cassette tape deck — and the fun begins.

To ensure that the fun never stops, and to keep Apple working hard, we've spent the last year expanding the Apple system. There are new peripherals, new software, and the Apple II Basic Programming Manual. And wait till you see the Apple magazine to keep owners on top of what's new.

Apple is so powerful and easy to use that you'll find dozens of applications. There are Apples in major universities, helping teach computer skills. There are Apples in the office, where they're being programmed to control inventories, chart stocks and balance the books. And there are Apples at home, where they can help manage the family budget, control your home's environment, teach arithmetic and foreign languages and, of course, enable you to create hundreds of sound and action video games.

When you buy an Apple II you're investing in the leading edge of technology. Apple was the first computer to come with BASIC in ROM, for example. And the first computer with up to 48K bytes RAM on one board, using advanced, high density 16K devices. We're working to keep Apple the most up-to-date personal computer money can buy. Apple II delivers the features you need to enjoy the real satisfaction a personal computer can bring, today and in the future.

15 colors & hi-resolution graphics, too.

Don't settle for a black and white display! Connect your Apple to a color TV and BASIC gives you instant command of three display modes: Text, 40h x 48v Color-graphics in 15 color and a 280h x 192v High Resolution array that lets you plot graphs and compose 3-D images. Apple gives you the added capability of combining text and graphics, too.

Back to basics, and assembly language too.

Apple speaks three languages: fast integer BASIC, floating point BASIC for scientific and financial applications, and 6502 assembly language. That's maximum programming flexibility. And to preserve user's space, both integer BASIC and monitor are permanently stored in 8K bytes of ROM, so you have an easy-to-use, universal language instantly available. BASIC gives you graphic commands: COLOR=, VLIN, HLIN, PLOT and SCRN. And direct memory access, with PEEK, POKE and CALL commands.

Software: Ours and yours.

There's a growing selection of pre-programmed software from the Apple Software Bank—Basic Finance, Checkbook, High Resolution Graphics and more. Now there's a User Section in our bank, to make it easy for you to obtain programs developed
other Apple owners. Our Software
ink is your link to Apple owners all
er the world.

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ex sound
music.
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sclusive built-in
speaker delivers
added dimension of sound to your
programs. Sound to compose electronic
music. Sound to liven up games and
lucational programs. Sound, so that
your program can “talk” back to you.
that's an example of Apple's “people
compatible” design. Another is its light,
natural injection-molded case, so you
can take Apple with you. And the
professional quality, typewriter-style
keyboard has n-key rollover, for fast,
error-free operator interaction.

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Apple is a state-of-the-art single
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board and built-in diagnostics sim-
plify troubleshooting. In fact, on our
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test new Apples.

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are smart peripherals.
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highly practical programs are available now.
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continuously
updated
stock quotes for
more than
6000 com-
panies listed
on six major U.S.
exchanges. Current
activity for stocks in
the investors portfolio is delivered
automatically: ask/open, bid/close, high,
low and last prices, and volume traded.
Our Portfolio Evaluator enables
you to analyze current value of your
portfolio, and short- and long-term gain/
loss for each stock—or for your entire
portfolio.
Cost of Apple's Dow Jones service
is a one time contract fee of $25, which
includes the Stock Quote Reporter pro-
gram. An additional $3 charge is made
for the first three minutes of any transac-
tion and 50¢ per minute thereafter.
To take advantage of Apple's new
financial services, Apple II users need
only a communications card, a modem
and an ordinary telephone. This equip-
ment, the Dow Jones Series, and a broad
selection of other Apple software are
now in stock at your local Apple dealer.

Programming is a snap!
I'm halfway through Apple's BASIC
manual and already I've programmed
my own space wars game.

Those math programs I wrote
last week—I just rewrote them using
Apple's mini-assembler and got them
to run a hundred times faster.

Apple's smart peripherals make
expansion easy. Just plug 'em in and
they're ready to run. I've already
added two disks, a printer and the
communications card.
PASCAL PRAISE

I have just finished absorbing the Pascal articles and editorial in the August 1978 BYTE. If I were a crowd, I’d carry you off on my shoulders, cheering.

The pressure of monthly deadlines seems to have reduced most computerist periodicals to compendia of “How I Did This” and “How to Make That.” Recent themed issues of BYTE, though, show exceptional maturity and some solid planning. Your reasoned advocacy of a powerful, common language, with supportive material gathered into one reference issue, ranks as the most important contribution yet.

Pascal appears satisfactory for all our purposes. The concept of p-code provides the mechanism for bringing it to fruition.

Onward, computerists! The milling matron trumpeter. One half (left side) is clothed and the other half is exposed so that the mechanism is visible. Pressed in any information they may have, including any programming information which might be helpful.

Paul F. Doering
56 Elmore Rd
Rochester NY 14618

AUTOMATON TRUMPETER LIVES

On pages 105 and 106 of “Antique Mechanical Computers, Part 2” in August 1978 BYTE there are references to automaton trumpeters and a statement that none survive.

I just returned from Europe and observed at the Deutsches Museum in Munich Germany a life-sized automaton trumpeter. One half (left side) is clothed and the other half is exposed so that the mechanism is visible. Pressed for time, I was not able to find out if it still operates, or who constructed it.

William Harmon
2662 Grand Summit
Torrance CA 90505

COMPUTERS AND ADVERTISING

I am working on both a book and a magazine piece about the use of computers in the field of advertising—particularly in media control, including production scheduling, space acquisition and scheduling for print and broadcast media.

I would be grateful if any BYTE readers with experience in this relatively untapped software area could send me any information they may have, including any programming information which might be helpful.

I am also interested in a program which not only includes production and scheduling control, but carries the whole program right through to a daily alert printout, client billing, and acquisition of advertising space and time.

Maybe I’m asking for too much—but I have a feeling that someone out there may have already worked this out or is at work on it.

In any event, to anyone who would care to send me information I can use in my projected book and article, I would be most grateful.

Larry Ashman
1624 Dole St #1004
Honolulu HI 96822

SIGNETICS 2650: A CORRECTION

I have just finished reading “How to Choose a Microprocessor” by Lou Frenzel, page 124, in July 1978 BYTE. I feel that the advice he gives is excellent; however I also feel compelled to correct an inaccuracy in his section on the Signetics 2650. I own and constantly use a 2650 based microcomputer made by the Central Data Corp. This is available in a basic 1 board configuration complete with on board programmable memory, read only memory, cassette and video input and output (10). It is expandable to an S-100 system with floppy disks, 8 K and 12 K BASIC interpreters, assembler/editor, and debugging program. Central Data also publishes a regular newsletter to communicate with the already large number of users of this system.

I have programmed PDP-11s, 8080s, the 2650, and a SC/MPS. The 2650 instruction set comes closest to the power of the PDP-11, and I find it a real pleasure to use.

Gordon Brandly
RR 2
Fort Sask
Alberta CANADA T8L 2N8

SOME REFERENCES ON NETWORKING AND PROTOCOLS

Concerning your editorial in July 1978 BYTE, there are two pieces of literature which your readers may want to review. Both concern the Octopus computer network in use at Lawrence Livermore Laboratory in Livermore, CA, which is one of the campuses of the University of California.

The first article is in Datamation, April 19 1973, pages 58 thru 63. The second article is in Computer Design, July 1978, pages 77 thru 86.

The most impressive points of the Octopus network design are simplicity of both software and hardware implementation; suitability for use with standard, inexpensive, byte oriented, asynchronous modem hardware; and easy

Continued on page 158
If the truth is that you want a computer... then we want to be your computer store.

We're ComputerLand, the #1 computer store chain in the U.S. What's meaningful about that fact is, that ComputerLand has been chosen by more people as having what they've been looking for. And, since you're looking, let us tell you what you'll find, when you visit a ComputerLand store.

You'll find a product line that's continually evaluated to provide you with the widest and best selection in quality, brand name microcomputers anywhere. You'll find an enthusiastic and knowledgeable staff able to interpret all the equipment specifications, in terms of how they apply to you, and in a way you'll understand. You'll find demonstration areas where you can get a firsthand experience of running a computer yourself.

**COMPUTERS FOR BUSINESS**

You'll find educational materials to give you a total insight into the world of microcomputers.

You'll find a fully equipped service department to provide whatever assistance is required to keep your computer running in top-notch condition. You'll find computer user's clubs to join, where you can share ideas with people as enthusiastic as yourself. And, with each new visit, you'll find excitement—from the people you deal with, the equipment they offer, and from your own ever-growing personal involvement.

Enough about us. How about what computers do. To attempt to describe all the things your computer might do, would be to describe your imagination. So instead, we'll briefly list some of the many things for which small computers are already being used.

**In business,** the advent of the versatile and compact microcomputer has put the benefits of computing within reach of small companies. With systems starting at less than $6000, the businessman can computerize things like accounting, inventory control, record keeping, word processing and more. The net result is the reduction of administrative overhead and the improvement of efficiency which allows the business to be managed more effectively.

**In the home,** a computer can be used for personal budgeting, tracking the stock market, evaluating investment opportunities, controlling heating to conserve energy, running security alarm systems, automating the garden's watering, storing recipes, designing challenging games, tutoring the children... and the list goes on.

**In industry,** the basic applications are in engineering development, process control, and scientific and analytical work. Users of microcomputers in industry have found them to be reliable, cost-effective tools which provide computing capability to many who would otherwise have to wait for time on a big computer, or work with no computer at all.

And now we come to you, which leads us right back to where we started: **If you want a computer, then we want to be your computer store.**

Whether you want a computer for the home, business or industry, come to ComputerLand first. We'll make it easy for you to own your first computer. Because, simply put, we really want your business. When you come right down to it, that's what makes us #1.
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ARE ALL BUSINESS
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When we designed our new small business computers, we meant business.

As basic as that seems, it is unique. Just about every other microcomputer being sold as a small business system today was originally designed as a kit for hobbyists.

Every design decision was made with quality and reliability in mind. The result is dependable performance and a solid appearance for business, professional and scientific applications.

FIRST SMALL SYSTEM WITH BIG SYSTEM STORAGE

Many applications handle large quantities of information, so the DB8/2 uses two quad density 5-inch disk drives with our exclusive Dual Density Disk Controller for up to 1.2 megabytes of formatted storage. That’s more capacity than two single density 8-inch drives.

If you need more storage, our DB8/4 has two 8-inch drives with up to 2 megabytes capacity, more than any other dual floppy disk system on the market.

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Continuous Fourier Transform

Before discussing the FFT in particular, it is desirable to briefly survey some of the general concepts of the classical continuous Fourier (pronounced "foor-yay") transform. The terminology used refers to time and frequency since they are among the most common variables of interest in many applications, although the theory involved applies to a variety of different types of physical phenomena.

Consider the waveform \( x(t) \) shown in figure 1a which is displayed as a function of time (denoted by \( t \)). The waveform can also be described by the frequencies present in the signal. This description is called the spectrum of the time signal. Mathematically, it is the Fourier transform of the time function. The process of Fourier transformation is represented by the mathematical function

\[
X(f) = \int_{-\infty}^{\infty} x(t) e^{-j2\pi ft} \, dt
\]

where \( X(f) \) is the Fourier transform of \( x(t) \). [The constant \( j \) is used in electrical engineering to denote \( \sqrt{-1} \), also called \( i \). The number \( e, 2.71828 \), is the base of the natural algorithms.] For all but fairly simple functions, this mathematical process represented a formidable operation for many years. Prior to the development of the digital computer, many analytical and experimental methods were investigated for determining the approximate spectra of functions that arose in physical systems.

The magnitude of a typical spectrum is shown in figure 1b and is denoted by \(|X(f)|\), where \( f \) represents the frequency in Hertz (Hz). For example, if \( x(t) \) were a music signal, strong peaks of the spectrum at low frequencies would be characteristic of a significant amount of bass content such as...
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drums or tubas. Conversely, many string instruments such as the violin display stronger peaks at higher frequencies in the audio spectrum. The frequency spectrum (or Fourier transform) thus provides a plot of the relative weight of different frequencies that comprise or represent the given signal.

If the Fourier transform or spectrum of a signal is known, the time function may be determined from the inverse transformation which is given by

\[ x(t) = \int_{-\infty}^{\infty} X(f) e^{j2\pi ft} df \]

Observe that the inverse transform has essentially the same general form as the direct transform except for the sign of the exponential argument.

The concept of the frequency spectrum has long played a most important role in numerous scientific applications and has been of interest to mathematicians, engineers and scientists of many different disciplines. Among the areas where spectral analysis has been employed are sound and music analysis, communications systems design, analysis of mechanical vibrations, ocean wave analysis, statistics and many others.

Discrete Fourier Transform

The heart of the FFT is a mathematical operation known as the discrete Fourier transform (DFT). In the DFT, a set of integers n and m are defined to represent the equivalent in a sense of the time and frequency variables, respectively, of the continuous Fourier transform. This correspondence is best seen by observing the sampled signal x(n) shown in figure 2a. There are assumed to be N samples of the signal spaced T seconds apart. Thus, as n varies from 0 to N−1, the N samples of the time signal are generated. The duration of the time signal is \( t_p = N T \).

The DFT of x(n) is defined by the finite summation

\[ X(m) = \sum_{n=0}^{N-1} x(n) W^{mn} \]

where

\[ W = e^{-j2\pi n/N} \]

The function X(m) represents a discrete spectrum with m serving the same purpose in frequency as n did in time. The frequency increment between successive components is \( F = 1/t_p \) so that the spectral component at a frequency mF is X(m). For x(n) real and for N time points, a unique spectrum can be computed only at N/2 frequency points. Actually, X(m) is periodic in m with N points in each period, but only N/2 are unique. X(m) is, in general, a complex function consisting of a real and an imaginary part at each frequency. For many applications, the magnitude spectrum \( |X(m)| \) is the quantity of most significance. Some of the preceding points are illustrated in figure 2b.

As in the case of continuous signals, an inverse discrete Fourier transform (IDFT) can be defined. In this case, the inverse transformation is
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The resulting function is periodic in the variable \( n \) and has \( N \) points in one period. Thus, even if the original time signal were not periodic, the operation of the IDFT produces a function capable of providing the desired results in one cycle, but the pattern continues to repeat itself if the interval is extended outside of the basic range.

Observation of the definition of the DFT reveals that there are approximately \( N \) complex multiplications and about the same number of complex additions required to compute the spectrum at one particular value of \( m \). Since there are \( N/2 \) unique spectral components, the total number of computations required to generate a complete spectrum is of the order of \( N^2 \). The Cooley-Tukey algorithm, published in 1965, demonstrates one way to perform this transformation with a number of computations of the order of \( N \log_2(N) \), which turns out to be an enormous savings in computational time for long signal records. The Cooley-Tukey algorithm, along with subsequent variations, is referred to as the fast Fourier transform (FFT). Thus, the FFT is a high-speed algorithm for computing the discrete Fourier transform.

While the DFT is a finite summation and the classical Fourier transform is an integral transform, the DFT may be used to closely approximate the continuous function under many circumstances. Some of the concepts involved with such an approximation are considered later in this article.

The various FFT algorithms work best when the number of points in the sample record is an integer power of 2, i.e.: \( N = 2^k \), where \( k \) is an integer. The form of one of the basic algorithms is shown in figure 3 for the case of \( N = 8 \). Obviously, \( N = 8 \) is far too small for most applications, but the flow graph is of interest in understanding the form of the general computational algorithm. This particular algorithm is referred to as an in place algorithm since at each stage of the computation, the data may be stored in the same memory locations from which they were obtained.

**Implementation of In Place Algorithm**

The in place algorithm previously discussed was implemented on the Digital Group Z-80 System using BASIC. The program is given in listing 1. The particular system used had 18 K bytes of memory, of which about 12 K bytes were required for the BASIC software. It was determined that a 256 point transform could be computed with this system and the program listed uses this capacity. It could be readily expanded or contracted as the available memory size dictates. However, the size selected should be chosen as an integer power of 2 as previously noted. Thus, the next smaller size should be 128 and the next larger size should be 512.

In order to reduce the memory requirements, the trigonometric functions are generated as they are required in the program. This approach is not nearly as efficient from the standpoint of computation time as would be the process of initially generating and storing the functions in

\[
x(n) = \sum_{m=0}^{N-1} X(m)w^{-mn}
\]
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Listing 1: Fast Fourier transform routine described in text. Lines 10 to 499 are available for the user to describe the time function that is to be studied.

2 DIM X1(256), X2(256)
4 N=256: L=B： P1=3.14159
6 REM -- GENERATE TIME FUNCTION --
10 REM
20 REM LINE NUMBERS 10-499 ARE USLD TO
30 REM GENERATE OR INPUT THE TIME FUNCTION
40 REM
50 PRINT 'DO YOU WANT A LISTING OF THE GENERATED TIME FUNCTION ?'
510 INPUT A$
520 IF A$='NO' THEN 440
530 IF A$='YES' THEN 500
540 B=X1(0)
550 FOR Z=0 TO N-1
560 IF ABS(X1(Z))>B THEN B=ABS(X1(Z))
580 NEXT Z
600 FOR Z=0 TO N-1
610 PRINT X1(Z) TAB(4) X2(Z) TAB(4)
650 FOR Z=0 TO N-1
650 PRINT 'HARMONIC ITABLE 30 1 X1<Z> HAR1NACY ITABLE 50 I X2<Z>
670 REM -- SCALE INPUT TIME FUNCTION --
680 REM GENERATE OR INPUT THE FUNCTION
700 REM LINE NUMBERS 410 TO 799 ARE USLD TO
710 PRINT
800 REM -- OUTPUT RESULTS --
810 PRINT 'IN WHAT FORM DO YOU WANT THE OUTPUT ?'
820 INPUT A$
830 IF A$='YES' THEN 870
840 IF A$='NO' THEN 990
850 END
880 REM - OUTPUT RESULTS -
890 PRINT 'IN WHAT FORM DO YOU WANT THE OUTPUT ?'
900 PRINT 'MAGNITUDE SPECTRUM PLOT (1)'
910 PRINT 'TABLE OF VALUES (2)'
920 REM
930 REM
940 IF A=1 THEN 970
950 IF A=2 THEN 1130
960 PRINT 'INCORRECT INPUT (1 OR 2)' : GOTO 890
970 REM - OUTPUT MAGNITUDE SPECTRUM PLOT -
980 PRINT 'CALCULATIONS IN PROGRESS -
990 REM - OUTPUT RESULTS -
1000 IF A=1 THEN 1100
1010 IF A=2 THEN 1270
1020 PRINT 'IN WHAT FORM DO YOU WANT ANOTHER OUTPUT (YES, NO) ?'
1030 IF A$='YES' THEN 1240
1040 REM
1050 IF A$='NO' THEN 990
1060 END

memory so that they can simply be called as required. However, where speed is not a major priority, this approach minimizes the total memory required.

Statements 10 through 499 in the program represent the particular input signal for which the transform is being computed. The time function may be generated by appropriate equations or an algorithm as will be demonstrated for several cases later. For experimental data, the values could be listed point by point if the function cannot be readily described by an equation.

Applying the Program

In order to effectively utilize an FFT program for spectral analysis, it is necessary to understand some of the peculiarities of the DFT and its relationship to the continuous Fourier transform. Although the FFT treats the signal as if it were periodic. The total duration of the time signal is the period $T_p$, and for the program being considered, this period contains 256 points. If $T$ is the time increment between samples, then $T_p=256T$. The spectrum obtained from the DFT is also periodic and contains $N$ (or 256) spectral components. However, for a time function that is real (which incidentally is the case for all signals considered in this article), it can be shown that half of the components are ambiguous; i.e. they are similar to the other half and do not represent any actual spectral information. Thus, there are $N/2$ (or 128) meaningful complex spectral components that are obtained with the FFT. These components are spaced apart in frequency by $F=1/T_p$. The value for $m=0$ corresponds to the DC component, $m=1$ is the fundamental, $m=2$ is the second harmonic, etc. According to sampling theory, a time signal must be sampled at a rate at least equal to (practically speaking, greater than) twice the highest frequency contained in the spectrum. Thus, if the highest frequency contained in a spectrum
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Listing 2: Three different generating routines that can be used with listing 1 as the time functions. The first routine generates a pulse function that lasts 25 percent of the time that is being analyzed. The second routine also generates a pulse but half as long as the first routine. The third and fourth routines generate sine waves which are only slightly different.

Figure 4: Rectangular pulse for which the FFT is partially displayed in photos 1 and 2. The pulse is unity for 64 of the 256 points in the time record and zero for the remainder.

Figure 5: Rectangular pulse for which the FFT is partially displayed in photo 3. The pulse is unity for 32 of the 256 points in the time record and zero for the remainder. Since this pulse is shorter than the one of figure 4, the spectrum is broader. In general, there is an inverse relationship between the width of a pulse-like time function and the width of the frequency spectrum. This property is an important concept in signal transmission and results in the requirement of larger bandwidths for transmitting shorter pulse signals.
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large number of points, the function is shown as a continuous curve.) The video display of the first 14 spectral components in tabular form is shown in photo 1, and the first 15 components of the magnitude spectrum are displayed in photo 2. Henceforth, only the magnitude spectra will be shown.

When the pulse duration is changed to 12.5 percent of the period or 32 points as indicated in figure 5, the magnitude spectrum changes to the form shown in photo 3.

It should be pointed out that the bandwidth of a rectangular pulse is theoretically infinite in extent and so there is some aliasing error in each of these cases. However, the effects of aliasing are not pronounced in these two examples over the frequency range shown in the photos. At larger harmonic

---

**Photo 1:** The first 14 components (DC and harmonics up through the 13th) of the FFT spectrum corresponding to the pulse shown in figure 4. The program lists the real part of $X(m)$, the imaginary part of $X(m)$ and the magnitude $|X(m)|$.

---

**Photo 2:** Video graphics display of the magnitude spectrum corresponding to the pulse shown in figure 4. The display is of course rotated $90^\circ$ from the basic mathematical form illustrated in figure 2.

---

**Photo 3:** Video graphics display of the magnitude spectrum corresponding to the pulse shown in figure 5.
values for the given signals and at shorter pulse widths for the given frequency range, the aliasing errors would be more significant.

A sine wave representing an assumed frequency of 1000 Hz and an assumed sampling time of \( T = 0.1953 \text{ ms} \) was generated and analyzed. The resulting spectrum is shown in photo 4. Note that the frequency resolution is \( F = \frac{1}{(0.1953 \times 10^{-3} \times 256)} = 20 \text{ Hz} \) so that 1000 Hz corresponds to harmonic number 50. Observe that an ideal single line appears as one might hope. On the other hand, when the frequency is changed to 1010 Hz while maintaining the same value of \( T \), the spectrum changes to the form shown in photo 5. The reasons for the striking difference are as follows: In the first case, the frequency corresponds exactly to one of the harmonic numbers (50th harmonic), and a property of the DFT is that no other line components appear in this case. However, in the second case, the component would theoretically appear halfway between the 50th and 51st harmonics so that the imperfections of the finite time duration of the observed sinusoid are now apparent. The phenomenon observed is called leakage. It can also be readily verified that the first sinusoid was observed over an exact integer number of cycles, while in the second case, the sinusoid was truncated during a cycle.

This example illustrates the necessity of understanding some of the limitations of the truncation and sampling processes in order to properly evaluate results. The phenomena just noted can be reduced by smoothing the data to be transformed with certain window functions before computing the FFT. Window functions smooth the beginning and end of a record length and reduce the effects of leakage on the spectrum.

More Examples

Other applications include the use of an analog to digital converter to sample speech and music waveforms or the waveforms encountered in electronic systems. The sample points could be stored for later spectral analysis using the FFT program. We hope readers will be encouraged to experiment with the program on their own computers.

REFERENCES


Photo 4: Video graphics display of the magnitude spectrum corresponding to a sine wave whose assumed frequency is 1000 Hz with a sampling interval \( T = 0.1953 \text{ ms} \). This assumption results in an integer number of cycles (50) in the record duration \( t_p \), which corresponds to 50 ms. The frequency then corresponds exactly to the 50th harmonic and the spectrum appears as a single line.

Photo 5: Video graphics display of the magnitude spectrum corresponding to a sine wave whose assumed frequency is 1010 Hz with a sampling interval \( T = 0.1953 \text{ ms} \). This frequency corresponds to the midpoint between the 50th and 51st harmonics, and the imperfections of the DFT in representing a continuous time signal now can be seen.
Designing a Universal Turing Machine

A Software Approach

Hardware or software; which is best? This question faces many designers when creating new systems. This article describes a software version of a hardware project detailed in December 1976 BYTE by Jonathan K. Millen in his article "A Universal Turing Machine," page 114.

The universal Turing machine (UTM) is elegantly simple and capable of emulating the instruction set of any computer. The Turing machine was invented by Alan Turing (1912-1954). It is an abstract computing device that contains all the fundamental properties a computer system must possess and is used to study computer concepts. Although difficult to program, its back-to-basics nature is alluring to anyone interested in the fundamentals of computers.

The universal Turing machine designed by Jonathan Millen has two memories: one for program storage and the other for the main storage or "tape." The tape is a supposedly infinite (but actually 1024 bits long) memory which is a series of 1s and 0s. A bit on the tape is pointed to by a counter known as the head. A program counter points to a state in the program being executed. Each state consists of two instructions: one to be used if the current bit under the head of the tape is a 1, the other if it is a 0. Each instruction contains fields describing whether to write a 1 or a 0 on the tape, which direction to move the tape (left or right one position), and the address of the next state to be executed.

Each instruction contains the following information:

- **Bit 0:** Write bit. Write this bit on the tape after the head is adjusted.
- **Bit 1:** Direction bit. If this is a 0, move the tape to the left; if it is a 1, move the tape to the right.
- **Bits 2 thru 7:** Next state. These six bits are the number of the next state to be executed.

The reader is referred to Millen's article for a complete description of the universal Turing machine. His design implements this machine with about 15 integrated circuits. The memories are 2102s, the head and program counter are counters, and the control logic consists of various flip flops, shift registers, clocks and decoders. The memories are loaded and examined with switches and a 7 segment light emitting diode (LED). The design is capable of executing about 40,000 instructions per second.

A Software Approach

The program in listing 1 is the logical equivalent of Millen's hardware version for the Motorola 6800 processor. The program storage, tape, program counter and head are parts of the computer's memory set aside for those purposes. The memory organization is shown in Table 1. The rest of the logic is programmed via the 6800's instruction set. Table 2 is a comparison of the various functions and their implementation in the two approaches.

The program is a relatively straightforward programming of the hardware version. The basic cycle of functions to be performed is:

- Test the bit on the tape under the head.
- Write a 1 or 0 according to the write bit of the instruction indicated by the program counter and the tape bit.
- Move the tape (adjust the head) according to the instruction's direction bit.
- Set the program counter equal to the address specified by the address bits of the instruction.
- Go back to the first step.

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Circle 320 on inquiry card.
The universal Turing machine program is stored in the first 128 bytes of memory. Each state consists of two 1 byte instructions, so that the instruction's address in memory is the state number multiplied by 2. The 6800 has no multiply instructions, but in this case the same effect may be accomplished by the rotate left instruction:

Before shift 0 0 1 0 0 0 1 0 = decimal 41 state number.

After shift 0 1 0 1 0 0 1 0 = decimal 82 state address.

Hardware versus Software

Although there is probably not a great practical need for Turing machines of this type, the two designs provide some insights into the benefits and costs of each approach.

The most significant benefit of the hardware approach is speed. The program can only process 10,000 universal Turing machine instructions per second, or 25 percent of the circuit's capability.

The most significant benefit of the software approach is its flexibility. For example, suppose the address field of the instruction

Listing 1: 6800 assembler version of the universal Turing machine, which imitates the hardware version built by Jonathan Millen. This program is capable of executing 10,000 universal Turing machine instructions per second.

<table>
<thead>
<tr>
<th>Address</th>
<th>Hexadecimal</th>
<th>Label</th>
<th>Op Code</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
</table>
| 0200    | DE FE       | BEGIN | LDX     | HEAD    | GET HEAD OF TAPE ADDR.
| 0202    | D6 FD       | BEGIN | LDA B   | MASK    | MASKS OUT BIT ON HEAD
| 0204    | E5 00       | BEGIN | BIT B   | 0,X     | IS BIT ON TAPE 0?
| 0206    | 27 03       | BEQ   | ZEROBIT |         | YES, DON'T INCREMENT PROGRAM COUNTER
| 0208    | 7C 00 FC    | INC   | PC+1    |         | NO, INCREMENT PROGRAM COUNTER
| 020B    | DE FB       | ZEROBIT | LDX    | PC    | GET ADDRESS OF NEXT TURING INSTRUCTION
| 020D    | A6 00       | LDA A | 0,X    |         | GET TURING INSTRUCTION IN REGISTER A
| 020F    | 0C          | CLC   |         |         | CLEAR CARRY PRIOR TO TEST
| 0210    | DE FE       | BEGIN | LDX    | HEAD    | GET HEAD BYTE AGAIN
| 0212    | 85 40       | BIT A | #$40   |         | MASK OFF DIRECTION
| 0214    | 27 07       | BEQ   | DEC    |         | DECOLUMN IF IT IS ZERO
| 0216    | 56          | ROR B |         |         | ROTATE RIGHT IF IT'S A ONE
| 0217    | 24 09       | BCC   | OK     |         | NO CARRY TO NEXT BYTE
| 0219    | 08          | INX   |         |         | INCREMENT HEAD BYTE
| 021A    | 56          | ROR B |         |         | SHIFT CARRY THROUGH
| 021B    | 20 05       | BRA   | OK     |         | ALL DONE
| 021D    | 59          | DEC   |         |         | ROTATE MASK LEFT ONE BIT
| 021E    | 24 02       | BCC   | OK     |         | NO CARRY TO NEXT BYTE
| 0220    | 09          | DEX   |         |         | DECREMENT HEAD BYTE
| 0221    | 59          | ROL B |         |         | ROTATE THRU CARRY
| 0222    | DF FE       | OK    | STX    | HEAD   | RESTORE HEAD POINTER
| 0224    | D7 FD       | STA B | MASK   |         | RESTORE MASK
| 0226    | 4D          | TST A |         |         | CHECK LEFT BIT OF INSTRUCTION
| 0227    | 28 05       | BMI   | WRITE1  |         | SKIP IF IT IS ON COMPLEMENT MASK TO
| 0229    | 53          | COM B |         |         | WRITE A ZERO
| 022A    | E4 00       | AND B | 0,X    |bra, branch | 'AND' IN A ZERO
| 022C    | 20 02       | BRA   | branch |         | SKIP AROUND THE
| 022E    | EA 00       | ORA B | 0,X    |branch | 'OR' IN A LOGIC
| 0230    | E7 00       | BRANCH | STA B | 0,X   | PUT BYTE BACK TO TAPE
| 0232    | 84 3F       | AND A | #$3F   |         | MASK OFF TWO LEFT
| 0234    | 49          | ROL A |         |         | BITS
| 0235    | 97 FC       | STA A | PC+1   |         | STORE AS NEW PROGRAM COUNTER
| 0237    | 7E 02 00    | JMP   | BEGIN  |         | EXECUTE NEXT UTM INSTRUCTION

The logic to test the current bit is:

| TEST | LDX HEAD | Load head byte address.
| LDA B MASK | Load bit mask within byte.
| BIT B 0,X | Test corresponding bit in memory.
| BEQ ITSONE | Yes, it's a 1.
| ITSONE | logic if bit was a 0.
| ITSONE | logic if bit was a 1.

The program increments the head position (moves tape to right) by rotating the mask to the right. If the bit is rotated out and into the carry, the HEAD address is incremented. The procedure is similar for moving the tape left.

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The most significant benefit of the software approach is its flexibility. For example, suppose the address field of the instruction

<table>
<thead>
<tr>
<th>Hexadecimal Addresses</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 thru 007F</td>
<td>Universal Turing machine program and state storage area.</td>
</tr>
<tr>
<td>0080 thru 00FF</td>
<td>Universal Turing machine tape storage area.</td>
</tr>
<tr>
<td>00FB thru 00FC</td>
<td>Universal Turing machine program counter address of next state.</td>
</tr>
<tr>
<td>00FD</td>
<td>Tape head mask.</td>
</tr>
<tr>
<td>00FE thru 00FF</td>
<td>Tape head address.</td>
</tr>
<tr>
<td>0200 thru 0237</td>
<td>6800 interpreter program (listing 1).</td>
</tr>
</tbody>
</table>

Table 1: Memory allocation for the software implementation of the universal Turing machine.
More and more, you see the North Star HORIZON computer at work: in business, research, and education. Its high performance qualifies the HORIZON for demanding professional applications. Over 10,000 users during the past two years have proven that North Star hardware has the reliability for day-in, day-out computing. The HORIZON is now a serious candidate for any small system installation.

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is to represent a signed displacement from the current program counter, as Millen suggests in his article. In hardware, this would require adding a 6 bit adder between the address bus and the program counter, plus some temporary latches to hold the results. In software, a store instruction must be changed to an add instruction. In hardware, the board must be modified to accommodate the new circuitry, and the clock re-adjusted. In software, under MIKBUG, the change can be made with seven keystrokes.

If this system were to be widely distributed, complete documentation would have to be written. The hardwired approach requires a circuit board layout, a schematic diagram, parts list and written commentary. In the software version, comments in the program serve to document the system, along with a written commentary.

The software approach allows a building block technique. The program may be easily combined with other programs. The external programs need to know only the addresses of the various blocks in the universal Turing machine program’s logic. The universal Turing machine circuit would have to be modified to adapt it to other equipment. The software version uses MIKBUG’s load and dump routines to save the tape contents, but this would have to be a specially constructed circuit for the hardwired design.

The design, implementation and testing times of the software version were two, one and two hours, respectively. I don’t know the exact times required for the hardware approach, but they should be at least several times more than the software approach.

In order to build the hardwired circuit, the experimenter must obtain all the circuitry, a circuit board, wire, power supply, etc., which may or may not be used in future experiments. However, once you have a microcomputer to work with, no extra items are needed and the computer is usable for any other projects without losing the ability to reload the universal Turing machine program.

This example cannot be taken as a complete treatment of the trade-offs of the two approaches. Each designer must judge the merits of an approach according to the particular needs of the problem to be solved. If the universal Turing machine were to be mass-produced for time-critical applications, the hardware approach would be best. If the design is to be used for the Sunday afternoon project of a microcomputer enthusiast who already has a system the software approach would be best.

<table>
<thead>
<tr>
<th>Function</th>
<th>Hardware Version</th>
<th>Software Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program storage</td>
<td>2102</td>
<td>Memory locations hexadecimal 00 thru 7F</td>
</tr>
<tr>
<td>Tape storage</td>
<td>2102</td>
<td>Memory locations hexadecimal 80 thru FF</td>
</tr>
<tr>
<td>Program counter</td>
<td>Two 74161s</td>
<td>Memory locations hexadecimal FB thru FC</td>
</tr>
<tr>
<td>Head</td>
<td>Three 74191s, 7474</td>
<td>Memory locations hexadecimal FD thru FF</td>
</tr>
<tr>
<td>Sequencing</td>
<td>7404,74161,74154</td>
<td>Conditional branching</td>
</tr>
<tr>
<td>Display</td>
<td>7 segment LED</td>
<td>MIKBUG print/punch command</td>
</tr>
<tr>
<td>Initializing tape</td>
<td>74157,7400,switch</td>
<td>MIKBUG load command</td>
</tr>
<tr>
<td>Saving tape</td>
<td></td>
<td>MIKBUG print/punch command</td>
</tr>
<tr>
<td>Debugging design</td>
<td>Logic probe and</td>
<td>MIKBUG break command</td>
</tr>
<tr>
<td></td>
<td>oscilloscope</td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Correspondence chart of the functions of the two approaches and the means with which they are implemented.

REFERENCES

1. Millen, J. "A Universal Turing Mac"


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<tr>
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<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
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<td>$495.</td>
</tr>
<tr>
<td>MEGABOX dual drive double density system</td>
<td>$2,295.</td>
</tr>
<tr>
<td>ZEPHIER — Per Sci double density system</td>
<td>$2,595.</td>
</tr>
<tr>
<td>Z-PLUS — MEGABOX 32 KZ-80 computer</td>
<td>$4,295.</td>
</tr>
</tbody>
</table>

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“Steve, I think we have a little problem!” Ray charged into the basement and hovered over me waiting for a response.

I slowly rotated in my swivel chair. The rate was barely sufficient to overcome static friction, but I finally made it. As I raised my head to talk I was interrupted.

“Steve, I think we have a problem with that EROM.” Before he could finish, his expression abruptly changed and almost without a pause he ended the sentence with, “...what happened to you? You look like death warmed over!”

I could barely see the person standing before me with his hands on his hips. I also experienced a strange sensation of either a veil covering my face or an advanced case of furry eyeballs. Whatever the cause, Ray was still standing there awaiting a reply. It was a chore to speak. As the muscles contracted to produce the necessary air flow, I could sense a sudden recurrence of physical problems which I had hoped were on the wane.

“Steve you look terrible! You should be raring to go after two weeks in Acapulco, basking in the sun.”

Ray was referring to an engineering consulting job I had just completed in Acapulco for CBS. The Miss Universe Pageant, which was broadcast live from Mexico, included a new twist this year. A computerized judging system. It sounded like a fun consulting job as opposed to the usual, “design me a computer for...” type. The final rationalization was, I needed a vacation anyway. I wouldn’t want anyone to think that the 70 contestants had anything to do with my decision to go.

The other lucky members of our engineering party were Gus Calabrese (formerly with Digital Group) and George Watson and Dale Walker of CBS. Gus and I maintained the hardware; Dale supported the software; and, while George’s official function was the electrical scoring system, his unofficial title was chief taco tester. He had this uncanny ability to sort through all the various smells emanating from a restaurant and evaluate palatability. If he didn’t turn green as he walked through the door, it was Americanized enough for us to eat there.

This smooth sailing trip was punctuated by a succession of daily crises. For instance, George’s wife, having thoughtfully packed his suitcase without underwear, gave us the hoped for opportunity to take a crash course in Mexican capitalism and to venture out to the market place. The cab driver who “drove” us there (I use the word loosely) was subject to suicidal fits. From then on everything went downhill. The list goes on and on. Reliving the past two weeks in my thoughts heightened the sense of physical malaise I was experiencing. Fortunately, Ray spoke again in time to bring me back to reality.

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“Let’s just say it has something to do with a guy called Montezuma.”

“You’re not supposed to drink. . . .”

“Yeah, I know! Don’t drink the water!”

Ray looked at me and decided his problem still needed attention, even though I was dying. “Steve, I was about to check the EROM contents against the listing you gave me when I noticed that it was in octal. We need to use that EROM tomorrow and we had better find the error in it tonight. I made a hexadecimal dump of the EROM contents but I still can’t check it against your listing.”

The response was obvious. “Why don’t you convert it by hand?”

“Sure,” said Ray, “I can convert it, but a thousand conversions is more than I have time for tonight. Can we assemble it in hexadecimal on your system?”

My temples were starting to throb. I hadn’t used my computer in three weeks. Nothing was hooked up and I was in no condition to either attach and fire up my own programmer or write the simple algorithm to perform this minor calculation. It was hard enough for me to remember how to operate my own system without explaining the intricacies to Ray.

“Look, Ray, any night but tonight. I’ve got it in octal, decimal, hexadecimal, binary, —anything you want, but not tonight. I just don’t think I can hack it. You understand, don’t you?”

He was disappointed, but being a good friend he understood. “Can I borrow your TI programmer and some desk space? A thousand entries times five button pushes . . . shouldn’t take more than an hour or two. Got your battery charger handy?”

It seemed a shame to make Ray go to such lengths. If my system were up it would take only a matter of seconds to print out Ray’s listing. It may have been a very powerful Z-80 computer on any other occasion but tonight it wasn’t processing anything.

As I reached for the calculator in my briefcase I spied a relic that might provide a solution to the problem. “Ray, see that rectangular box with all the printed circuit boards plugged into the top of it?” I pointed to a bookcase that contained everything but books. “Bring it here and plug it in, and search through that pile of tapes over there until you find one marked with the same name as your listing. I made a binary dump on tape at the same time I made your listing.” There are some advantages to being ill—letting others fetch and carry is one of them.

Relying mostly on Ray’s high level of hardware expertise, interspersed with whatever limited verbal input I could manage, we successfully fired up my Sclbi-8B 8008 microcomputer. Even though I hadn’t used it for well over a year, the read only memory based operating system brought it to life immediately. The recognizable pattern on the light emitting diode (LED) display indicated it was ready to read input data, so I slapped in the cassette that Ray had found. Fortunately the data was stored in a format acceptable by both machines, and totally independent of the processor. I couldn’t execute the Z-80 EROM listing I had loaded, but I could display it.

“OK, Ray. Now that we’ve loaded the data we can step through it on single step and look at it on this output port display, which I built a while back.”

“How’s that going to help?” Ray looked at the 3 character display as he pressed the single step a few times. “The 8008 is an octal machine. Even the data on your display is coming out octal,” he said.

It was hard to smile but I managed a slight variation on the theme as I said, “Flip the switch next to the display.” Instantaneously, the 257 previously displayed changed to AF, its hexadecimal equivalent.

“Hey, that’s not bad, a combination octal and hexadecimal display! All I have to do is step through and copy down the hexadecimal equivalents, right?”

I nodded and Ray started to write. Barely ten entries had been made when his hardware curiosity got the best of him. “I was thinking of putting one of these on my system but it looked like too many components. By the way, I only see two chips. Where are you hiding the rest?”

“Remind me to tell you when I recover.”

Build a Combination Octal/Hexadecimal Display

Some people may consider hexadecimal displays a trivial addition to an expensive computer system, but sometimes these little add-ons make program debugging easier. I can’t help but wonder whether other computer experimenters would have need for such a display. I don’t expect it to replace the video display; but often, when debugging a program, it’s nice to be able to display a byte here and there to verify proper program execution. It will never replace the stepper and breakpoint monitor I now use, but it’s great to display keyboard or IO data quickly with a single output instruction.

There are many methods to display hexadecimal numbers on a 7 segment LED. Figure 1 and table 1 show an example of the usual brute force method using a read only memory as a hexadecimal decoder. Programming the 82523 was described in the
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Fortunately there are other products on the market that can solve the problem. I've been using the Hewlett-Packard HP7340 hexadecimal display for a number of years. Those familiar with it can rightfully say how trivial the solution was, while those who are not may find it a revelation. Photo 1 illustrates the physical size of the HP7340. A hexadecimal A is displayed in a dot pattern. These hexadecimal displays depart from standard 7 segment format by being capable of displaying a capital B and D in hexadecimal. This is accomplished by controlling the corner dots which give the appearance of "rounding." This ability discriminates a B from an 8 or a D from a 0. There are 16 distinctly different characters.

An additional feature of the HP7340 is that it contains a 4 bit latch and the decoder/driver as well. The result is a single 8 pin hexadecimal display which successfully accomplishes the function of all the circuitry in figure 1. The specification of the individual pins are in figure 4.

Figures 2 and 3 demonstrate how the HP7340 can be configured to function as a 2 digit hexadecimal output port or a 3 digit octal port. No 8 bit latch is required since it

Table 1: Program for IC2 in figure 1.

<table>
<thead>
<tr>
<th>Input Code</th>
<th>82523 Program</th>
<th>7 Segment Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCBA</td>
<td>d7 d6 d5 d4 d3 d2 d1 d0</td>
<td>1</td>
</tr>
<tr>
<td>0000</td>
<td>0 1 1 1 0 1 1 1</td>
<td>1</td>
</tr>
<tr>
<td>0001</td>
<td>0 1 0 0 0 0 0 1</td>
<td>1</td>
</tr>
<tr>
<td>0010</td>
<td>0 1 1 0 1 1 0 1</td>
<td>1</td>
</tr>
<tr>
<td>0011</td>
<td>0 1 1 0 1 0 1 0</td>
<td>1</td>
</tr>
<tr>
<td>0100</td>
<td>0 1 0 1 0 1 0 0</td>
<td>1</td>
</tr>
<tr>
<td>0101</td>
<td>0 1 1 1 0 1 0 0</td>
<td>1</td>
</tr>
<tr>
<td>0110</td>
<td>0 1 1 1 1 1 1 1</td>
<td>1</td>
</tr>
<tr>
<td>0111</td>
<td>0 1 1 0 0 0 0 0</td>
<td>1</td>
</tr>
<tr>
<td>1000</td>
<td>0 1 1 1 1 1 1 1</td>
<td>1</td>
</tr>
<tr>
<td>1001</td>
<td>0 1 1 1 0 0 0 0</td>
<td>1</td>
</tr>
<tr>
<td>1010</td>
<td>0 1 1 1 1 0 1 0</td>
<td>1</td>
</tr>
<tr>
<td>1011</td>
<td>0 1 0 0 1 1 1 1</td>
<td>1</td>
</tr>
<tr>
<td>1100</td>
<td>0 1 1 0 1 1 0 0</td>
<td>1</td>
</tr>
<tr>
<td>1101</td>
<td>0 1 1 1 1 1 1 0</td>
<td>1</td>
</tr>
<tr>
<td>1111</td>
<td>0 1 1 0 0 1 1 0</td>
<td>1</td>
</tr>
<tr>
<td>1111</td>
<td>0 1 1 1 1 1 0 0</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 1: Hexadecimal latch, decoder and driver using a standard 7 segment light emitting diode (LED). Line CS on IC2 can be used to perform the blanking operation. This circuit can be replaced by a Hewlett-Packard HP7340 or equivalent (see table 2).
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Photo 2: Prototype board of the circuit in figure 4. Two similar circuits were built on the same board. When in the hexadecimal mode (shown at left in the picture), the leading digit is blanked. The display at the right shows the octal mode. Each is wired as an independent output port, but the computer sends the same data to both.

Figure 2: Hexadecimal latch, decoder and driver display circuit.

Table 2: Pin functions for the Hewlett-Packard HP7340 binary coded decimal (BCD) to hexadecimal display. Similar displays are made by Dialite and Texas Instruments.

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input B</td>
</tr>
<tr>
<td>2</td>
<td>Input C</td>
</tr>
<tr>
<td>3</td>
<td>Input D</td>
</tr>
<tr>
<td>4</td>
<td>Blank Control (blank = +5 V)</td>
</tr>
<tr>
<td>5</td>
<td>Latch enable (latch = 0 V)</td>
</tr>
<tr>
<td>6</td>
<td>Ground</td>
</tr>
<tr>
<td>7</td>
<td>+5 V</td>
</tr>
<tr>
<td>8</td>
<td>Input A</td>
</tr>
</tbody>
</table>

Figure 3: Octal latch, decoder and driver display circuit.
Figure 4: Combination hexadecimal and octal display circuit.

Table 3: Power wiring table for figures 1, 2, 3 and 4.

<table>
<thead>
<tr>
<th>Number</th>
<th>Type</th>
<th>+5 V</th>
<th>Gnd</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>7475</td>
<td>5</td>
<td>12</td>
</tr>
<tr>
<td>IC2</td>
<td>82523</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC3</td>
<td>HP7340</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>IC4</td>
<td>HP7340</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>IC5</td>
<td>HP7340</td>
<td>7</td>
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<td>HP7340</td>
<td>7</td>
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</tr>
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<td>IC11</td>
<td>HP7340</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>IC12</td>
<td>HP7340</td>
<td>7</td>
<td>6</td>
</tr>
</tbody>
</table>

already contains one. The 7340s can simply be attached to the data bus at any other parallel output port and strobed from a chip select decoder.

Figure 4 is the circuit of the unit similar to the one Ray used. Two multiplexer circuits alternate the input connections to the displays so that when switch 1 (SW1) is in the octal position, the circuit performs as figure 2, and when in the hexadecimal position, as figure 3. The leading character is blanked when in the hexadecimal mode. Two of these circuits are combined in the prototype board of photo 2. The left display is in the hexadecimal mode showing B7 while the right is in the octal mode displaying an equivalent 267 octal. The same binary information is being sent to each port; only the switch setting differs.

Usually these or equivalent displays are advertised only as hexadecimal displays. All strictly hexadecimal displays that I’ve seen contain these same electronics. While alphanumeric displays will also work, they require extensive scanning logic and are an overkill for this application.

In Conclusion

I hope this simple circuit will eliminate any frustration you may have in the area of hexadecimal displays.

If you have any comments about this or any other article I have written, please write and include a stamped, self-addressed envelope. The mail volume has risen to the point where I’m asked similar questions by many experimenters. A few of these letters will be included each month in BYTE’s “Letters” column when appropriate.

One question I’m often asked is whether my introductions are true. So far everything I’ve written is based upon actual people or events. While I take considerable poetic license in describing the situations, it is not necessary to invent fiction when experience is often so much more humorous.
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Many games are only the point of departure for exploration by the hobbyist. One could extend many of these to any home built computer. A lot of thought went into this book and it shows. I think the book does the best possible thing for a hobby: it makes the hobby more fun.

Noel K. Jukowski
Naval Environmental Prediction Research Facility
Monterey CA 93940

The Pocket Calculator Game Book
by Edwin Schlossberg and John Brockman
William Morrow and Company Inc
New York 1975
158 pages hardbound
$6.95

For many of us, the introduction to the microcomputer is the pocket calculator. However, after we learn its functions, it often ends up in a drawer except for shopping and checkbook balancing. It shouldn’t. There are many ways to use your calculator for enjoyment.

I like the competitive aspect of this computer business, either against the machine or another player. Therefore I like those books which show me new games to play. In this collection of 50 games, the authors present a variety which will appeal to everyone. There are applications for the “four-banger” as well as the more complex scientific models. You can play with one or more calculators, and one or more players. You may throw in dice or playing cards for variety.

There are easy games and hard ones, offering a range for all ages. Several have two versions, a simple method and complex one for those of you with the costlier machines. “1001” is one of several games whose object is to reach a particular number using the fewest moves. Use dice to determine your move, and hope for luck. There is “Calculator Poker” with betting strategy to guide you. For the business minded, there is “Economy” with all the trappings of high finance. The student of political science will find meat in “Cold War” or “Detente.” There are puzzles, mazes and much more. As a puzzle freak, I found my favorite among these pages. By multiplying and dividing in a judicious manner, one can deduce the proper path to follow. A game is a valuable test to see whether your calculator can handle certain operations. This would be an excellent way to check out a calculator that you are considering buying.

Throughout the book, the authors offer samples of how each game should be played, as well as winning strategy. In the introduction are explanations for those concepts which may be new to some readers, such as random numbers, and a glossary of hand calculator terms. A handy index divides the games into like categories, such as number of players, or games with dice, and so forth.
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The fun way into computers.
What can you do with your computer? After hearing about the game of Life, you may never ask the question again. Within the capabilities of a very minimal system, Life gives the computer the kind of job it does best: an enormous amount of repetitive logical operations. [The authors' system demonstrates this point: it had 2 K memory and a video terminal at the time of this writing.] This leaves you, the user, free to apply your creative energy on this fascinating game.

Developed by John Horton Conway, a British mathematician at the University of Cambridge, Life was first described in the October 1970 Scientific American by Martin Gardner in his "Mathematical Games" column. Its name comes from its resemblance to changing societies of living organisms which can grow, move and occasionally die out.

The Game of Life

An easy way to understand this game is to imagine an immense gridwork or checkerboard. We call each square in the checkerboard a cell, and the entire board a cellular space. Each cell is identical and can perform a number of specific functions. We won't worry about the edge of the board; let's say the space is large enough so that we never know there is an edge. In the game of Life, each cell can sense its eight neighboring cells (as in figure 1). Each cell in our space is in one of two states: it is either alive, or not alive (quiescent). The cellular space changes with time; time advances over the entire space at once, in steps. Each of these steps is called a generation.

The rules which determine the state of a given cell in the next generation are what give Life its delightful properties. They were chosen with great care by Conway, with reasons in mind that will be discussed later. [For mathematical background information see the book, Introduction to Artificial Intelligence by Philip C Jackson, published in 1974 by Petrocelli-Charter. A discussion of cellular automata and pointers to several detailed references are found in chapter 8.] Let us say there is a pattern of cells in the cellular space, some living, some not. The rules tell which presently living cells survive, which living cells die, and which cells that are not now alive will be living in the next generation. The rules are as follows:

- Each cell presently alive which has either two or three of its eight neighboring cells alive will be living in the next generation.
- Each cell presently alive which has other than exactly two or three live neighbors will not be alive in the next generation.
- If a cell is presently not alive, and exactly three of its eight neighboring cells are alive, it will be living in the next generation.

The above rules are applied all at once in the program for the game of Life. Every cell in the space is checked, as are its neighbors. The fate of that cell in the next generation is then determined. Note that this will amount to many thousands of checks in each generation for a cellular space filling even a small video display screen.

When the program has been loaded into the computer and you've entered the pattern, what can happen as the pattern evolves? There are a number of possibilities.

Figure 1: The center cell (0) has eight neighbors, as does every cell except those bordering the edges of the cellular space in any finite buffer in a computer program. Treating boundary conditions for a finite Life buffer is a fine point of Life program design.

Figure 2: Examples of still life cell patterns, the block (a) and the beehive (b).
Types of Patterns

The pattern may die, leaving you with an empty display as you search your imagination for another possibility to try.

It may stop at what Conway calls a still life. A simple example (figure 2) is the block, another the beehive. These patterns, when left undisturbed, remain the same generation to generation (a little more interesting than a blank screen, perhaps).

The pattern may develop a repeating cycle. The simplest of these is the blinker, which returns to its original self every other generation (see figure 3). A more sophisticated periodically repeating pattern has been described in the February 1971 Scientific American. Discovered by G D Collins Jr, it is called the tumbler (figure 4). It has a period of 14 generations, but after seven it is an upside-down copy of the original pattern; hence its name. Watching the tumbler change, you will notice that in every generation there is a row of empty cells separating two mirror image patterns. Each half helps keep the other half under control. If left to itself, half a tumbler will run over 100 generations before settling down.

There are patterns which have most intriguing properties of motion. The glider shown in figure 5 is one such pattern. It is so named because the way that it moves is called glide reflection, or reflection from a diagonal line. In four generations the glider produces a replica of itself, facing the same direction but displaced one square diagonally. After only two generations, it is a copy of itself pointing 90° from its original orientation. There are actually just two unique patterns in the life history of the glider, but it takes four generations for the orientation to match that of the original pattern.

Another example of a moving pattern is the lightweight spaceship shown in figure 6. This pattern also requires four generations to move and to complete a full cycle; it also has only two unique patterns if we disregard their orientation. Note that this pattern moves along a line of cells, as opposed to the glider's diagonal motion.

Finally, patterns exist which continue indefinitely, forever evolving. (It was not certain that such infinite patterns should exist for some time after Life was developed.)

Infinite Evolution a Possibility?

Conway selected the rules of Life to meet the following considerations:

- It should not be obvious that an initial pattern will grow without limit. (Conway specified that cells can die from overcrowding.)
- It should seem possible (but not obvious) that some patterns will grow without limit.
- Some initial patterns should grow and change for a considerable period of time.

As reported in the original Scientific American series of articles, Conway conjectured that there were no patterns which would actually grow without limit. At that time he offered a $50 prize to the first person to prove or disprove his conjecture. A short time afterwards a group from MIT disproved it by their discovery of a glider gun. The glider gun produces a glider every 30 generations. Since the glider moves away from its birthplace, we may consider the glider gun to be a special type of repeating pattern (see figure 7). The MIT group also discovered other remarkable events in Life by observing such things as collisions between numerous gliders.

Symmetry

A rather curious property in the evolution of many patterns is their tendency to gain symmetry. As an example, let us begin with a pattern with only partial symmetry called the snowflake, shown in figure 8a. In 15 generations it becomes the pattern called...
the honey farm, shown in figure 8b. (This initial pattern used for producing a honey farm differs from the one discovered by Conway and his collaborators.) Within the brief history of this pattern, it gains new symmetry it can never lose. Apparently, unless the pattern dies out completely, symmetry can only be gained, never lost.

Another example of a pattern increasing its symmetry is given in figure 9. Again, beginning with only partial symmetry, it evolves into another known pattern, a beautiful oscillating pattern called Pulsar CP 48-56-72. It reaches this pattern in 26 generations during which it gains its symmetry. (The initial pattern given here is again an alternative path to the known pattern.) The oscillating period of the Pulsar is three generations, and it provides a very interesting display.

The “Garden of Eden”

Up to now, the evolution of patterns has been considered, using some initial pattern. Can this initial pattern itself have unusual properties? It has been proven that a so-called “Garden of Eden” pattern must exist for the game of Life. A “Garden of Eden” pattern is one which cannot be produced by any other pattern. In other words, no pattern ever becomes a “Garden of Eden” pattern.
Figure 7: The glider gun is shown in mid-cycle with two generated gliders, the arrow indicating their direction of travel. A more detailed description of this pattern is given in the February 1971 Scientific American column by Martin Gardner, page 114.

of Eden" pattern. Such a pattern can only exist, therefore, as an initial pattern specified in generation zero.

It has been shown that a "Garden of Eden" pattern for Life can exist within a square with 10 billion squares on each side, but possibly it could be much smaller.

Perhaps one way to find a "Garden of Eden" pattern is to apply some programming skill, and all your computer's spare time. You start with a pattern you devised or one your computer generated, randomly or otherwise. The computer could then attempt to find a pattern which generates your pattern by trying out all the patterns possible in a larger space than your pattern uses. If it did not succeed in generating your pattern, you would have found a "Garden of Eden" pattern. A lucky application of this brute force technique may come up with the answer, but the going will be very slow. Perhaps some clever shortcut could be developed.

A Warning

The game of Life is downright addictive because there is always another pattern that you'll want to try out in your search for attractive, unusual or unpredictable patterns. Examining properties of symmetry and motion, and looking for "Garden of Eden" patterns and patterns like the glider gun will test your ability to predict fate in the game of Life.

The Program

A program for Life could be written in BASIC or some other high level language, but it would be grossly inefficient, both in size and speed. First of all, only a single bit is required to store each cell, but there is no simple way to manipulate individual bits in BASIC. You would therefore be forced to use one element of a floating point array for each cell, and since a floating point number typically uses three bytes, you would only make use of one out of every 24 bits. That would mean for a 64 by 64 cellular array you would need 12 K bytes. (Actually, you would need twice this number since two copies of the cellular array are needed in the simple Life program to be described.) The obvious way to reduce the size is to use every bit; a 64 by 64 cellular array would then require only 512
I haven't stopped laughing since I read Steve Ciarcia's new book, "TAKE MY COMPUTER...PLEASE!" It's Steve's first full length book, and it's the funniest to come along in years! It's even funnier if you're into computers! Just one crazy misadventure after another, based on Steve's true experiences, and his computer's inability to cooperate. You'll roar when you read how he tries to win at Jai-Alai and gets beaten at his own game. Or how he attempts a stock market killing that goes wrong when he logs into his broker's computer circuit! Imagine what happens when our hero sets up a computerized speed trap! And you'll fall on the floor when our hero builds a foolproof computer burglar alarm, and then locks himself out of the house with a souffle in the oven! You can't beat this book for computerized belly laughs. It's got lots of hilarious drawings that make Steve's easy writing style come to life even more. And, you can't beat the low, low price of only $5.95 + S/H!

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Figure 8: The snowflake (a) and the pattern it generates after 15 generations, the honey farm (b).

Figure 9: This seed pattern (a) generates pulsar CP 48-56-72. One of the four cycle phases of the pulsar is shown in (b).

Figure 10: Flowchart of a Life program. [Authors' note: We have written a Life program for the SwTTPC 6800 system from this flowchart. Our version requires about 1.5 K of memory for a 2000 cell array, and takes only 6 seconds per generation. Our program can be configured for any size array up to a maximum of 2016 cells. Our 6800 Life program can be obtained from The Computer Warehouse Store, 584 Commonwealth Av, Boston MA 02215.]

bytes. The most efficient way to manipulate individual bits is to use assembly language. This will also be about ten times faster than a corresponding BASIC program, due to direct execution.

A general flowchart for a Life program is shown in figure 10. The program requires two workspaces, each the full size of the desired cellular array. The initial pattern is entered into workspace #1. The program then creates the next generation in workspace #2, since the original generation must not be altered until the new one is completed. After determining the new generation in workspace #2, it is copied back into workspace #1. The pattern is then displayed, and the procedure is repeated until the program is stopped.

As can easily be seen, Life can be a very interesting game. There are certainly moving patterns other than those described herein, and the possibility exists that one of you reading this could find a previously unknown moving pattern. If you make any discoveries while running Life, we would be glad to hear from you. Enjoy Life!
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</tr>
<tr>
<td>TI 745 KSR Portable Terminal</td>
<td>$1650</td>
</tr>
<tr>
<td>Hazeltine 1400 Terminal (ass'd)</td>
<td>$770</td>
</tr>
<tr>
<td>Hazeltine 1500 Terminal (ass'd)</td>
<td>$995</td>
</tr>
<tr>
<td>Bally Arcade</td>
<td>$299</td>
</tr>
<tr>
<td>Centronics 779 with tractors</td>
<td>$1095</td>
</tr>
</tbody>
</table>

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Some Facts of Life

David J Buckingham
Computer Communications
Network Group
E4, room 236BA
University of Waterloo
Waterloo, Ontario
CANADA N2L 3G1

Introduction

Life is a game that was developed by Prof. John H. Conway at the University of Cambridge and first presented by Martin Gardner in the October 1970 "Mathematical Games" column in Scientific American. The game is derived from a field of mathematics known as automata theory (in this case cellular automata). In the February 1971 "Mathematical Games" column the game was described again along with a good introduction to automata theory.

The game is played on a uniform cellular grid (in this case an area divided into squares, such as graph paper) where every cell is surrounded by eight immediate neighbors (i.e., cells touching the center cell under consideration). Each cell, or automaton, can be in either a 1 or 0 state (on or off — alive or dead). The population of cells is changed by a set of predetermined rules. These changes proceed in intervals called generations.

The rules are as follows:

- If a live cell is surrounded by two or three live cells in the present generation, it will remain on (or live) in the next generation.
- If an empty cell is surrounded in the present generation by exactly three neighbors, the cell will be on (i.e., born) in the next generation.
- If a cell has no neighboring live cells, or only one neighbor, it dies of loneliness and will be turned off in the next generation.
- If a cell has four or more live cells neighboring it, it will die in the next generation from overcrowding.

These rules are to be applied simultaneously to every cell in the pattern. The application of the rules to every bit in the field constitutes a generation. See figure 1 for an example of rule applications.

Unresolved Questions

What is a unique object in this universe of cells? What is a collection of objects? How do we tell them apart? These are difficult questions to answer conclusively. For the purposes of this article, an object is a cluster of connected bits or cells, a collection of clusters which will cause births by being near one another, or a collection of clusters that prevent some birth that would otherwise occur. Figure 2 gives some examples of patterns that would be objects and some that would not.

A collection of distinct objects is referred to as a constellation. Some constellations are so common that they are named as though they were a single object. Some of these are presented in figure 3.

Objects

Most people with access to some sort of computer have probably had a chance to observe the variety of patterns that exist within Life and to note some of the special properties particular to some of these objects. In order to be able to manipulate these objects, they have been classified.

The major groupings of classification are still lifes, oscillators, spaceships, uniform propagators, and a catch-all group of random objects. A rough outline of this system is shown in table 1. I shall attempt to describe...
Table 1: Classes and subclasses of objects occurring in Life, along with supplementary information.

<table>
<thead>
<tr>
<th>Class</th>
<th>Subclass</th>
<th>Number of objects known</th>
<th>Smallest object(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class I (still lifes)</td>
<td>subdivided by symmetry</td>
<td>(\infty)</td>
<td>block</td>
</tr>
<tr>
<td>Class II (oscillators)</td>
<td>((1a1)) flip flops ((1a2)) on-offs</td>
<td>(\infty)</td>
<td>blinker beacon</td>
</tr>
<tr>
<td></td>
<td>((1b)) billiard table configurations</td>
<td>(&gt;100)</td>
<td>MIT oscillator</td>
</tr>
<tr>
<td></td>
<td>((1c)) inductors</td>
<td>4</td>
<td>tumbler</td>
</tr>
<tr>
<td></td>
<td>((1d)) pulsators</td>
<td>8</td>
<td>mazing, pentadecathlon</td>
</tr>
<tr>
<td></td>
<td>((1e)) shuttles</td>
<td>5</td>
<td>shuttle</td>
</tr>
<tr>
<td></td>
<td>((1f)) eater bound</td>
<td>23</td>
<td>two eaters</td>
</tr>
<tr>
<td>Class III (spaceships)</td>
<td>((1la)) diagonal</td>
<td>1</td>
<td>glider</td>
</tr>
<tr>
<td></td>
<td>((1lb)) orthogonal</td>
<td>3</td>
<td>lightweight spaceship (LWSS)</td>
</tr>
<tr>
<td>Class IV (uniform propagators)</td>
<td>((1Va)) stationary</td>
<td>2</td>
<td>glider gun</td>
</tr>
<tr>
<td></td>
<td>((1Vb)) moving (puffer trains)</td>
<td>4</td>
<td>switch engine</td>
</tr>
<tr>
<td>Class V (random)</td>
<td>subdivided by type of objects in census</td>
<td>(\infty)</td>
<td>bit (single cell)</td>
</tr>
</tbody>
</table>

Table 2: The number of small still life patterns which occur for each number of live cells up to 14.

<table>
<thead>
<tr>
<th>Number of live cells</th>
<th>Number of still life patterns</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
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<td>5</td>
<td>6</td>
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<td>11</td>
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</tr>
<tr>
<td>12</td>
<td>121</td>
</tr>
<tr>
<td>13</td>
<td>240</td>
</tr>
<tr>
<td>14</td>
<td>619</td>
</tr>
</tbody>
</table>

Figure 3: Commonly occurring constellations. These are not a single object, but bear names for convenience, as follows: a, traffic light; b, honeyfarm; c, fleet; d, bakery.

Figure 4: An assortment of still life objects. These remain stable from generation to generation when not disturbed by other objects. They bear names as follows: (top row, left to right) a, block; b, tub; c, boat; d, beehive; e, ship; f, barge; g, snake; h, aircraft carrier; (bottom row, left to right) i, burloaf; j, long boat; k, long snake; l, period 3 eater; m, pond; n, long barge; o, shillelagh; p, hat.
each class and some of the objects of particular note within each class.

Class I: Still Lifes

Still lifes are objects in which there are no births or deaths and so remain the same from generation to generation. These particular objects are fairly easy to enumerate. An associate of mine, Peter Raynham, wrote a program which found all still lifes of less than 15 bits. The statistics of their distribution are presented in Table 2. Some of the smaller ones are shown in Figure 4.

One of the most practical uses of a still life is as an eater. An eater is an object capable of destroying or modifying another object and being able to return to its original configuration. Still lifes are good for this since they are able to attack any configuration at any phase (they are period 1 objects and do not change).

At present we know of three different eaters, each able to attack different types of objects. By differing objects, I mean objects that have different border configurations. Since the eater attacks only the outside surface of an object, this outer surface determines which type of eater might be suitable for use. Each eater will be described with an object that it can "eat" to show how that eater works.

The smallest member of the eater family is the block, shown in Figure 4a. The block is effective in consuming objects that have one connected bit in the row facing it (as in Figure 5). Its other reason for utility is the fact that it is very small. In oscillators and spaceship guns, where there may be little room for the removal of spurious debris, there is usually enough room for a block.

The second object of this family is the period 2 oscillator, which if traced, will reveal a flip flop, deaths occur because of under-population. (This is almost always true. Figure 9 is a period 2 oscillator, which if traced, will reveal that it adheres to both definitions.) A variety of small period 2 oscillators is shown in Figure 8; the type of each oscillator is also given.

Next in the hierarchy are billiard table objects that exhibit a flat connected outer border that is at least two bits long. Figure 6 shows such an attack. Almost all objects will develop this type of border if they expand. This property renders the period 3 eater invaluable. Although it is not quite as small as the block, it is still very much smaller than any other of the eater family.

The third such object, the period 6 eater, exhibits similarities to the period 3 eater in the way it eats; however it requires six generations to dispose of its prey and return to its initial state, whereas the previous eater takes three generations. This increase in time is important for success if the object being eaten has left some transient debris near the eater. If the eating mechanism were to reform itself quickly, this debris could kill the eater. In this case, the eater does not reform for an extra three generations, during which time this debris may well vanish.

Most of the period 6 eater's prey are the same as the period 3 eater's; but both are able to attack certain additional objects, complementing each other very nicely. Figure 7 shows the period 6 eater conveniently disposing of a block.

Class II: Oscillators

Oscillators are nonmoving objects with periods of two and greater. A blinker, shown in Figure 8a, is a simple oscillator consisting of three cells alternating in subsequent generations between a vertical and horizontal row. At present, we know of roughly 150 unique oscillators with a period greater than two.

There is a large undetermined number of period 2 oscillators, since they are very easy to construct. The oscillators have been subclassified by relating their mechanisms and their degree of naturalness. (Natural objects are those which may evolve from random patterns of live cells without intervention by the experimenter.)

Since there are only two basic ways in which a period 2 oscillator can work, these objects are very well defined. Therefore, they are assigned to their own subclass (class IIa). They must work as flip flops, on-offs or a combination of the two. In a flip flop, deaths occur because of under-population. In an on-off, any deaths that occur are due to over-population. (This is almost always true. Figure 9 is a period 2 oscillator, which if traced, will reveal that it adheres to both definitions.) A variety of small period 2 oscillators is shown in Figure 8; the type of each oscillator is also given.

Figure 5: A block devours a beehive. This process requires seven generations, as shown here.
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Figure 6: The most versatile eater object, the period 3 eater, devours the precursor pattern to beehive. While in isolation a 7 cell still life, this eater attacks other objects with a flat connected outer border at least two cells in length.

Figure 7: A period 6 eater attacks and eats a block. This new eater is notably more symmetrical than the period 3 eater. Functionally, each complements the capability of the other.

Figure 8: A variety of small period 2 oscillators. These objects alternate in succeeding generations between two patterns. Those on the top row bear names as follows (left to right): a, blinker; b, beacon; c, clock; d, toad; e, bipole; f, tripole; those on the bottom row are unnamed flip flops. The beacon is the only example here of an on-off type oscillator.

Figure 9: A period 2 oscillator which functions both as a flip flop and as an on-off.
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Figure 10: Billiard table configurations. These oscillate within an enclosed area, as do balls on a billiard table. These are artificial objects which have not occurred unless specifically constructed by the experimenter. They tend to be large; the smallest is composed of 18 live cells. Those illustrated bear names as follows: a, MIT oscillator (a period 3 object); b, burloferimeter (period 7); c, an unnamed period 8 object; d, wavefront (period 4); e, an unnamed period 5 oscillator; f, an unnamed period 9 object.

Figure 11: Inductor and pulsator oscillators. These are natural objects which may appear from automation of random patterns. Inductors possess an imaginary line of symmetry which pulsators lack. They are called by the following names: a, pulsar (an inductor of period 3); b, tumbler (period 14 inductor); c, an unnamed period 8 inductor; d, pentadecathlon (pulsator of period 15); e, mating (period 4 pulsator); f, unix (period 6 pulsator). The pentadecathlon is of particular historical significance.
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configurations (class I1b). These oscillators are configurations that oscillate within an enclosed area, like balls on a billiard table. Billiard table configurations are considered to be very artificial, since they have not turned up in the histories of any random objects. By this, I mean that if live cells are placed randomly on the plane, the patterns which they generate probably will never evolve into an artificial object, such as a billiard table configuration.

They are quite large, as evidenced by the examples in figure 10. The first example is the smallest such object, and it consists of 18 bits. This subclass of oscillators contains the only known examples of oscillators with periods of 7, 10 and 11.

The next class, inductors (class I1c), are natural oscillators that exist in two or four pieces with an imaginary line of symmetry between them (exhibiting one-way or two-way orthogonal symmetry). Pulsators (class I1d) are also so far considered to be natural oscillators except that they do not have this line of symmetry. One of their properties is that they require no external stimulus to continue oscillating.

The aforementioned subclasses have greatly similar characteristics, so I have grouped them together. Most of the initial oscillators that were found were from this group, since the methods for harnessing random objects into oscillators were not known at the time.

Some of these oscillators are presented in figure 11; the most important of these is the *pentadecathlon*. This object throws off several sparks (small collections of dying bits) that can be used to reflect a glider, reflect two gliders, turn a glider into a block, turn a block into a glider, etc. Some of the early research into Life probably might not have occurred if this object had not been discovered.

Shuttles (class IIe) are important for the existence of much of the interesting research into Life. Shuttles are objects that move back and forth with a relatively long period. The two primary shuttles, the *basic shuttle* and the more complex *twin bees*, leave debris at their extremities which would fatally wound the shuttles if the debris were not removed before they returned (see figure 12). This is one of the uses of the eaters that was discussed in the section on still lifes. In the examples I have used blocks to remove the debris from the ends, but just about any of the eaters would have suited some phase of this debris. The debris left behind may at first seem to be somewhat of a bother, but without it there would most likely not be any known glider guns (defined later).

The very last class (class I1g) contains *eater bound oscillators*. These oscillators consist of patterns which generally must be manipulated in order for the object to return to its initial state. In figure 13 a good example of two eater bound oscillators is given that also shows the differentiation between two eaters acting on the same object (which is not often possible). A period 52 oscillator (figure 14) is shown to illustrate the unusual properties of objects being eaten. The center object will be attacked by one eater twice each time it rotates (the object rotates 90° every 13 generations). The example in figure 15 is a period 6 oscillator using the period 6 eater. The 7 bit eater is not suitable here because it would have returned to its original state too soon and would have attacked the reforming object. (If the 7 bit eater

---

**Figure 12:** Shuttle objects. Object a is the basic shuttle; object b is the twin bees shuttle. These move back and forth with a relatively long period. Eaters are used to remove debris from their path.

**Figure 13:** Two eater bound oscillators. These differ in that they are stabilized by two different eaters. Oscillator a has a period of 6; oscillator b has a period of 5.
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is used, the patterns results in two blinkers, six blocks, and one tub in 110 generations.)

Class III: Spaceships

Regrettably, there have been no new spaceships reported since the orthogonal spaceships presented in *Scientific American* in 1971. These are summarized in figure 16. The glider (figure 16a), which features diagonal movement, has been used for many simulations and constructions.

Movement by an object of one space in one generation is referred to as movement at the speed of light (c). There is no distinction made between diagonal and orthogonal movement, even though algebraically the distances are not the same. The glider travels at c/4 and the three other spaceships travel at c/2. The interesting thing to note is that the three larger spaceships travel orthogonally. The orthogonal spaceships are most useful in several of the types of puffer trains to be discussed in the next section.

Class IV: Pattern Producing Mechanisms

Class IV is divided into two sections: the

Spaceship Guns

Class IVa consists of spaceship guns. These objects eject projectiles of class III objects. The main two objects of class IVa are the glider guns of primary period 30 and 46. There are no primary guns which produce any of the other three spaceships. However, such a mechanism can be built using glider guns.

The period 30 glider gun (figure 17) works by having two shuttles of the type presented earlier aimed at one another. The debris that would normally be removed by eaters collides and just happens to create a glider that escapes without harming the shuttles. The period 30 glider gun is of paramount importance to simulations in Life and the possible existence of computing mechanisms. These implications will be discussed in a later article.

The period 46 gun, known as a newgun, also works by having two shuttles collide. It may be seen in figure 18. In this case the shuttle consists of two B heptominoes (described later) travelling opposite one another to produce debris at both ends of travel. A glider is produced when these two shuttles, which are of the twin bees type, collide at right angles. There are other arrangements of this shuttle that produce gliders in other ways, including an ambidextrous variety.

There is another interesting variation: if one of the debris removing blocks is removed from the end of one of the twin bee shuttles, the gun will still work.

Puffer Trains

Puffer trains are patterns that move and leave debris in their wake. Because these patterns do move, as opposed to the stationary spaceship guns, they are not only able to produce moving debris but also trails consisting of stationary objects. Leaving stable objects is useful when the intention is to produce a train of puffers to build some sort of construction on the fly.

The three basic puffer trains all work by different means. The train which was discovered first is presented in figure 19. The center object is a *pre-B heptomino*, which, if traced, will seem to move forward until the debris in the back of it stops the uniform forward motion. In this case, the B heptomino is bounded by two light-weight spaceships able to control the object; the whole configuration puffs along at c/2.

---

*Figure 14: A long period eater bound oscillator. This object has a period of 52; 13 generations are required for 90° of rotation. The central section is attacked twice by one eater each time it rotates.*

*Figure 15: A period 6 oscillator which employs the period 6 eater. This matching of period frequencies prevents the eater from disrupting the reforming central group.*
This object reaches a stable period of 140 after a startup time of over 1000 generations. Additional spaceships may be added to the end of the object to further adjust the output from it in order to reduce the final period, the startup time necessary to reach a stable period and to adjust the output to blocks, gliders, etc.

A type of puffer similar to the previous one is called a Schick ship (after its discoverer). This is an interesting object (consult figure 20) in that the "engine" is really a tagalong, an object capable of being pulled along behind another object (usually a spaceship). Here, a heptomino follows a pair of mirrored spaceships. It is quite remarkable that this configuration leaves a small trail of debris behind it and that, although this debris would die if left alone, additional spaceships following behind are able to trigger the debris into varying forms of static debris. The static debris can be left behind and used later. It is relatively useful for building armadas because of the relative simplicity of creating this object from gliders (producing a basic ship requires 11 gliders).

The last type of puffer train is the smallest, a mere 11 bits at startup — the size is somewhat larger when the final repeat cycle is known, since there is transient debris in the field. This particular train travels very slowly, taking 96 generations to traverse eight spaces (speed c/12). It is also very unusual in that it is the only known puffer train that travels diagonally — the same direction as the glider, but three times as slow.

Unlike the other puffer engines, this train does not require that any other spaceship exist to bound it. To stabilize the basic engine, a block must be placed somewhere in the debris produced by the object to prevent the debris from destroying it. If the engine is run without a stabilizing block, some rising debris finally catches the engine after 11 full cycles and destroys it. The remaining field settles down to a final census only after 3911 generations!

Pertinent to the above paragraph is the fact that random patterns are quite often able to produce certain types of edge configurations, which enable them to surge forward with a great burst of speed for short periods of time. In the case of the switch engine, when some random exhaust manages this type of movement, this slow moving engine is easily caught.

The switch engine (presented in figure 21) will produce, after its startup time, eight blocks every 288 generations. Other debris can be produced, including gliders. Since this train travels so slowly, there are presently no real uses for it.

Figure 16: The four known spaceships which occur in Life. Their appellations are: a, glider; b, lightweight spaceship; c, middleweight spaceship; and d, heavyweight spaceship. The glider travels diagonally at a rate of one space every four generations. The other three travel orthogonally at one space per two generations.

Figure 17: This glider gun, which has a period of 30 generations, was the first object of class IVa to be discovered. It periodically emits a glider which travels away diagonally. The four block still lifes are used as eaters to dispose of debris. Glider guns are of great importance in simulations, where gliders are made to collide, thus forming new objects.

Figure 18: A period 46 glider gun which is called the newgun. Two twin bees shuttles collide at right angles to produce one glider every 46 generations. As before, the block still lifes are used to remove debris which could cause disruption of the formation.
known 1105 objects of less than 15 bits in size.

Buckingham's most productive area of research has been the devising of glider collisions to produce objects of classes I thru IV. As of August 1978, he has managed to create collisions to produce all of the presently known 1105 objects of less than 15 bits in size.

A random object is simply anything that does not fit in any of the above classes. It appears that all random objects eventually become something from one of the above classes. It has been assumed that there are no objects that expand irreguarly forever (this is a common problem in other cellular spaces using other rules). There are some very popular nonterminals in life, which, due to their commonality, have been given names. In some cases these have been rather heavily investigated. In figure 22 are some of the more common nonterminals and their names.

The most common object of this class must be the oft published R pentomino (figure 22a), which many people still believe runs forever. The result of this pattern was, however, published in Scientific American; it runs for 1103 generations, producing four blinkers, eight blocks, one boat, four beehives, one ship, one burloaf, and six gliders.

The B heptomino (figure 22b), with a census of three blocks, one ship and two gliders in 148 generations, is one of the more heavily investigated objects, as is evidenced by some of the material presented in this article. It has the following interesting property: the front configuration of the object moves along to reappear the same every other generation, but flipped over.

A close relative of the previous object is the $\pi$ heptomino (figure 22c) with a census of five blinkers, six blocks and two ponds in 173 generations. Phase 1 of this object was called a blasting cap by the artificial intelligence researchers at Massachusetts Institute of Technology (MIT); we call phase 3 a house. If you trace the house for 30 generations, you will notice that a house reappears at the front of the debris ten spaces ahead of where it started. The house does not appear again after this because the debris catches up with it and kills it. Many attempts have been made to stabilize this object, with no success as yet.

A random object that consists of fewer than ten bits and that has descendants enduring for more than 50 generations is referred to as a Methuselah. The acorn pattern (figure 22d) is presently the record holder for duration. This is presented as a challenge to anyone who would like a difficult object to trace.

We hope that some of our investigations into the more exotic corners of Life will inspire readers to try their hands at this fascinating pastime.
Early issues of BYTE carried a never completed series by Carl Helmers inadvertently entitled "LIFE Line," which was also the name used for Robert Wainwright's newsletter. These Helmers articles appeared as follows:

"LIFE Line 1," September 1975 BYTE, volume 1, number 1, pages 72 thru 80;
"LIFE Line 2," October 1975 BYTE, volume 1, number 2, pages 34 thru 42;
"LIFE Line 3," December 1975 BYTE, volume 1, number 4, pages 48 thru 55;

A bibliography of Scientific American information on LIFE (all references are to Martin Gardner's "Mathematical Games" column).

October 1970: page 120. This is the original Life article, including the definition of the facts of Life, and illustration of numerous fundamental patterns.

November 1970: page 118. Answers to several questions posed in the first article on the subject, including definition of the several varieties of spaceships.

January 1971: pages 105, 106 and 108. Continued progress on the Life front including answers to several unsolved questions and results of a flurry of computer Life activity.

February 1971: Special "Mathematical Games" article on "cellular automata theory."

March 1971: pages 108 and 109. Short note about progress made by John Conway and R William Gosper, plus illustration of a large scale flip flop pattern which is delicately balanced and easily destroyed by minor disturbances such as impact of a glider.

April 1971: pages 116 and 117. Examples of fuses, the 5 cell cross series, and announcement of Robert T Wainright's Lifeline newsletter.

November 1971: page 120. Short note on continued progress at the MIT AI Laboratory.

January 1972: page 107. The discovery of the eater by Bill Gosper at MIT.

Hurry down to your public library if you wish to use these references, as due to lack of space some local libraries may be committing the unspeakable crime of throwing away Scientific American. . . . CH

The January 1979 Issue of BYTE will contain an article by Mark Niemiec which describes several algorithms for Life. Readers who wish to experiment with Life patterns will find these algorithms useful in writing efficient Life programs for their computers.

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One-Dimensional Life

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The game of Life is known to many computer experimenters for its beautiful, symmetrical two-dimensional displays and for its imaginary population of blinkers, beehives, gliders, and other strange, pseudoliving organisms. Invented by the British mathematician John Conway, the game was described in the “Mathematical Games” section of Scientific American in October 1970 and February 1971. A series of articles on how to program it for a home computer also appeared in three of the earliest issues of BYTE (“LIFE Line 1, 2, and 3,” BYTE September 1975, page 72; October 1975, page 34; December 1975, page 48). It is an attractive home computer software project, but the program requirements in memory capacity, processor speed and display capability were more than I possessed in my homebrew machine. The programming effort also looked formidable. I developed One-Dimensional Life as a small scale substitute.

Conway’s Two-Dimensional Life traces successive generations of a pattern of cells in an infinite square array of cells like an uncolored checkerboard. The generation rules determine the state of a cell in the next generation based on its present state and the states of its neighbors, the eight cells touching it.

Each cell has two possible states: off and

Figure 1: The state of a cell in the next generation is computed from its present state and the states of the four other cells in its neighborhood. The neighborhood of a cell consists of all cells within a distance of two cells from the cell in question.

(a)

Figure 2: The generation rules, illustrated here for a few representative cases. Each cell is marked with a dot if it is on, and left as an empty square if it is off. The next generation of the middle cell in each neighborhood is shown below it. 2a illustrates the rule that a cell is “born” if and only if it has two or three on neighbors in its neighborhood (in each example, the square being examined is shown in color). 2b illustrates that a cell survives if and only if it has two or four neighboring on cells. Note that a cell dies if it has three on neighbors.
A cell is "born" (i.e., goes on when previously off) if exactly three of its neighbors are on. A cell survives (i.e., stays on) with two or three neighbors on. Otherwise it is off in the next generation.

**Generation Rules**

In a one-dimensional version, patterns have to exist in a single row of cells. Each cell in the row has two cells touching it. I tried all possible generation rules involving a cell and its two neighbors, and I was disappointed in the results with all of them. It finally occurred to me to try a larger neighborhood including not only the adjacent cells but also the two adjacent to them (see figure 1). It still took several tries to come up with generation rules that seemed to yield a game approaching the richness of the two-dimensional game. The rules illustrated in figure 2 met my criteria for interest, which included the existence of oscillating patterns with long periods, patterns with long lifespans that eventually vanish, and gliders. The rules can be summarized as follows: Each cell is viewed with respect to a 5 cell region including itself and two neighboring sights on either side. Cells with two or three neighbors on are born and those with two or four neighbors on survive. The rest are off in the next generation.

The bare rules are rather plain without some biological "facts of life" to dress them up. The following explanation is offered:

**Rule 1: Birth.** Cells that are off but have either two or three neighbors on, go on.

**Rule 2: Survival.** Cells that are on and have two or four neighbors on stay on. Those with zero or one neighbors on die from loneliness; those with three neighbors on die from overcrowding. What keeps a cell with four neighbors on from dying is not clear. Maybe there is just not enough room to lie down.

**Examples**

Let us trace the life spans of a few patterns. The simplest oscillating pattern consists of two adjacent cells on. Its next generation has two cells on with two cells off in between, and the third generation regenerates the original pattern. Figure 3 shows three generations of this pattern. Note that the successive generations of a one-dimensional pattern form a two-dimensional pattern.

Another period 2 pattern is the flip flop in figure 4. A line of five adjacent cells on is also periodic, but with period 6. Seven generations of it are shown in figure 5.

A glider is shown in figure 6. It looks the same in every generation, but in each generation it moves one cell to the right. It is easily proved, incidentally, that One-Dimensional Life, unlike Two-Dimensional Life, has no stable patterns that repeat in one generation in the same place.

**Figure 3:** The simplest oscillating pattern, consisting of two adjacent cells on. Three generations are shown. Every second generation recreates the original pattern, so this pattern is said to have period 2. Its alter ego, the pattern with two cells on separated by two cells off, also has period 2. The three generations are separated in order to emphasize that they are separate generations rather than part of a Two-Dimensional Life configuration.

**Figure 4:** A pattern with period 2 that oscillates between the starting pattern and its mirror image. These kinds of patterns are sometimes called flip flops in conventional Life terminology. (Note that each line is the complete state of the Life universe in one generation.)

**Figure 5:** A line of five cells that regenerates itself after six generations. In my experience, this pattern has the longest period of any One-Dimensional Life pattern.

**Figure 6:** A glider pattern, so called because it regenerates itself in a steadily moving position. This glider has a period of 1.
We have seen a glider of period 1 and two static oscillating patterns of periods 2 and 6.

Are there patterns with all possible periods? I generated the life spans of lines with up to 15 cells and found one new oscillating pattern: a line of 12 cells that oscillates with period 4. This suggested that static oscillating patterns could be found for even periods, though I have not yet found any with periods longer than six. Of course if one starts a line of 12 (period 4) and a line of five (period 6) far enough apart to keep them from interacting, the pattern as a whole will not repeat until the twelfth generation, because 12 is the least common multiple of 4 and 6.

What about odd periods? Having found a glider of period 1, I tried a number of similar but longer patterns and discovered the period 3 glider shown in figure 7. Readers may enjoy discovering for themselves another period 3 glider that is one cell longer than the one in figure 7. It is tempting to conjecture that gliders exist with all odd periods. If anyone finds oscillating patterns or gliders of period 7 or greater, I would like to hear about it.

### Tabulation

There is an obvious notation for specifying a pattern without drawing a picture. A one-dimensional pattern, being just a sequence of on and off cells, may be regarded as a binary number. By convention, we can consider the pattern proper as just the cells between the leftmost on cell and the rightmost on cell, inclusive. Thus, the number for a pattern will always be odd, except for the "all off" pattern, 0. Pattern numbers can be reported in decimal, octal or hexadecimal to save space. For example, the first generation shown in figure 3 (two adjacent cells) can be represented by binary 11 (or hexadecimal 3). The second generation in figure 3 would then be represented by binary 1001 (or hexadecimal 9). The pattern of binary 11111 (hexadecimal 1F) goes through the following cycles, all noted in hexadecimal: 6B, 17D, 49, 1B, 55 and back to 1F. (Note the 3-digit hexadecimal number 17D, which is needed because the figure is nine cells wide at that point in the cycle.)

This numbering system also provides a handy way of enumerating patterns in a systematic sequence. This gives rise to the idea of constructing a dictionary of patterns in numerical order, listing for each pattern its vital statistics: whether it oscillates, glides, dies or leads to a noninteracting collection of oscillating patterns and gliders. By way of illustration, the first 28 entries in such a table are shown in table 1.

Theoretically there is also the possibility that a pattern may grow in mass (ie: the total number of cells on) without bound, like the glider gun found for Two-Dimensional Life. No such infinitely growing pattern has yet been found for One-Dimensional Life.

### Implementation

The discoveries of the period 4 pattern and the large period 3 gliders were made on my Turing machine computer. Implementing the One-Dimensional Life rules was easy and would probably have been easier if
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I had had a more conventional computer to work with, instead of a Turing machine (see "A Universal Turing Machine," December 1976 BYTE, page 114). The algorithm for producing new generations according to the rules is illustrated in figure 8, visualizing the memory requirements, and figure 9, a flowchart. Note that, as in Two-Dimensional Life, there is one complication to bear in mind when computing the next generation: When you change the state of a cell, you must remember the old state long enough to use it in computing the next state of its neighbors. If the program scans the row from left to right, changing cells as it goes, it needs a temporary memory of three cells. When the front of the scan is at cell N, the program is able to recompute cell N, after saving it, using its memory of the prior states of cells N - 1 and N - 2, together with the present states of cells N, N + 1 and N + 2. The old state of N - 2 may then be forgotten and the scan moved right one cell.

I will spare you the details of how this algorithm can be accomplished in Turing machine language. A more universal problem is how to get the patterns displayed. My only output device, at first, was a single LED (light emitting diode) that could be stepped through memory, to display it one bit at a time. To improve on this I built a visible shift register, a cascade of two 8 bit shift registers with an LED on each output, giving me a movable 16 bit window on memory. I was considering extending the window to 32 bits when I was lucky enough to get a long term loan of a SwTPC CT-1024 video display from a friend who had no present need of it.

There is a coincidental resemblance between a Turing machine and a video display: both normally change memory addresses by ±1. It turned out to be easy and natural to patch in the CT-1024 memory in place of the Turing machine "tape" memory. Turing machine computations were then directly visible as they progressed on the video screen. One more refinement was all that was needed to display successive generations of a pattern below one another as in the
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Figure 9: Flowchart for the One-Dimensional Life algorithm.

Photo 1: One-Dimensional Life display. On the author's system, 1s are represented by exclamation points and 0s by blanks. Each line represents one generation of One-Dimensional Life.

figures: up and down cursor control. Outputs were created by decoding the last three instruction address bits, effectively yielding eight 1 bit output ports that were strobed every time an instruction with the appropriate address was executed. Two of these outputs became cursor control outputs.

After all this hardware activity and some program modifications, the result was the kind of display shown in photo 1. The screen has the first 16 generations of a line of seven cells. This pattern settles down after 40 generations to a collection of non-interacting oscillating patterns, but before that happens it produces one of the most intriguing displays of its kind, one that I would never have seen without the help of a home computer. Of course, readers can verify these discoveries with any home computer and share in some of the excitement of exploration which I found.
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The game of Life was developed by John Horton Conway and was introduced in the “Mathematical Games” section of the October 1970 Scientific American magazine. Life is played on a grid of squares (in this case a 22 by 22 matrix). A given square is either occupied or empty. The program user specifies which squares are occupied initially.

The game of Life program produces new generations of the matrix by applying life’s laws for birth, survival and death to the present generation. These laws are:

**Birth:** An unoccupied square becomes occupied if in the preceding generation exactly three of the eight neighboring squares were occupied (squares that touch horizontally, vertically or diagonally are said to be neighboring squares).

**Survival:** An occupied square remains occupied if in the preceding generation two or three neighboring squares were occupied.

**Death:** An occupied square becomes unoccupied if in the preceding generation fewer than two or more than three neighboring squares were occupied.

Text continued on page 82

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**Listing 1: BASIC E program and sample run of the game of Life. A sequence of eight states of Life demonstrates operation of the program.**
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About the Author

William Englander is a self-employed computer programmer as well as an instructor at San Diego State University and National University.

Listing 1, continued:

RUN LIFE BASIC-E INTERPRETER - VER 1.3

ENTER INITIAL NUMBER OF ITERATIONS? 8
ENTER INITIAL COORDINATES: 0,0 TO END
? 8,10
? 9,10
? 10,10
? 11,10
? 12,10
? 0,0
ENTER PAPER SIZE (IN LINES/PAGE), SET UP PAPER & HIT ENTER? 33
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<table>
<thead>
<tr>
<th>State</th>
<th>Location</th>
<th>Address</th>
<th>Phone</th>
</tr>
</thead>
<tbody>
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<td>Alabama</td>
<td>Huntsville</td>
<td>Computer Store</td>
<td>205-539-000</td>
</tr>
<tr>
<td>Alaska</td>
<td>Anchorage</td>
<td>Computer Store</td>
<td>907-344-4336</td>
</tr>
<tr>
<td>Arizona</td>
<td>Phoenix</td>
<td>Computer Store</td>
<td>602-285-0065</td>
</tr>
<tr>
<td>California</td>
<td>Huntsville</td>
<td>Computer Store</td>
<td>907-344-4336</td>
</tr>
</tbody>
</table>

Text continued from page 76

The Life program in listing 1 was written in BASIC E and run on an IMSAI 8080. Since it is necessary to reference the present generation’s matrix while developing the next generation’s matrix, two arrays, A and B, are used alternately. When an array element represents an occupied square, it is given a value of 10. 1 is added to it for each occupied neighboring square (including itself for a square with three or more neighbors). Consequently a square in the next generation becomes occupied if its corresponding element in the present generation array is equal to 3, 13, or 14 (an empty square with three neighbors or an occupied square with two or three neighbors).

Statements 1 through 13 establish the number of generations to be printed and the initial occupied squares (in the A array). Statements 19 through 25 print the contents of the A array and zero the B array. Statements 27 through 34 generate the B array from the A array. Statements 36 through 42 print the B array and set the A array to zero. Statements 44 through 52 generate the A array from the B array and then loop back to produce the next two generations.
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Chess 4.7 versus David Levy

The Computer Beats a Chess Master

After 29 years, computer chess finally achieved a victory in human competition at the master class tournament level. During the fourth game of a match held at the Canadian National Exhibition from August 26 to September 4, 1978, International Master David Levy resigned to Chess 4.7/CYBER 176 after 56 moves, although he did win the tournament, 3½ to 1½.

David Levy was three years old in 1949, when the American mathematician and computer science pioneer Claude Shannon produced the first paper describing the methodology for producing chess playing computer programs. Not until 1956 did any machine win a game against a human opponent: MANIAC, a system developed at the Los Alamos Scientific Laboratory, won a greatly simplified chess game against a novice player in 23 moves.

12 years later, Levy, expert rated and Scottish National Champion, attended the Fourth Annual Machine Intelligence Workshop. There he took exception to the views of John McCarthy of Stanford University and Prof Donald Michie of Edinburgh University, who agreed that within ten years a computer system would be World Champion of chess. Levy countered that not only would computers fall short of that goal, but they would be unable to defeat him in a tournament style match within that 10 year period. Neither side was able to shake the other's convictions and, as a result, Levy wagered £1250 sterling that he could defend against the computer advances.

The machine intelligence community had expected Levy to be defeated by a large network of computers participating in the game, until 1970, when a Northwestern University program called Chess 3.0, written by Larry Atkin, Keith Gorlen and David Slate, clearly emerged as the leading effort in the first US Computer Chess Championship. David Levy was then 24.

The original feeling of confidence Levy held must have been somewhat shaken as the years 1973 and 1974 saw Chess 4.0 achieve a United States Chess Federation rating higher than that of the average US tournament chess player. [Note: the version number of the program increases along with its skill.] Then, in 1976 and 1977, when Chess 4.5 and 4.6 won the class B championship at the Paul Masson Open Chess Tournament and won outright at the Minnesota Open, Levy conceded that he had begun to think that his match with Chess 4.7, "would not be a formality but could be just a bit of work."

The latter part of 1977 and early 1978 saw a series of 2 game matches between Levy and Chess 4.6, the Duchess program from Duke, Greenblatt's MIT program, and Kaissa from the USSR. Levy handily defeated all the programs in the first game.

Chess 4.7, running on a Control Data Corp (CDC) CYBER 176, had compiled a rating of 2030 after 31 tournament games and a speed chess performance rating of 2450, when the last challenge was given. The issue was to be resolved on the tenth anniversary of the original wager, with play to begin on Saturday, August 26.

Getting a computer to a chess match, which was the duty of this author and Dr Dave Cahlander, is a considerably more difficult task than getting a human to a match. Crossing the Canadian border with microprocessor controlled chessboards, and setting up and testing telephone lines and modems between Toronto and the CYBER 176 in Arden Hills MN consumed most of a week.

The glass box in which the match was held, standing beside three bowling lanes and a fencing exhibition, faced a large demonstration chessboard and seats for onlookers. A square of chess tables used in simultaneous play filled the rest of the room. Opposite the glass box was the stand.
of Josef Smolij, local speed chess king and guru of the all-night, outdoor Yonge Street Chess Association. Josef, we were to learn, would play a large part in the first win ever for a chess machine at the master level.

The relationship between the opponents in the Levy match is difficult to describe. The two Davids, Levy and Slate, and the CDC folks stayed in the same hotel and ate meals, travelled and generally spent the entire time together as friends. Levy even considered the machine to be sort of a friendly foe. Each night the entire group found itself on the sidewalks of Yonge Street playing chess on overturned milk cartons with Joe Smolij until the small hours of the morning. Joe demonstrated his “Smash-Crash” Gambit (also known as the Greco Counter Gambit for those who have not yet met Josef) for 50 cents a lesson.

Levy’s plan for the match was not difficult to anticipate, since he had demonstrated that, while tactical positions favored the computer, strategic positions favored him. He had used close, quiet games to defeat the computers in each defense of the wager, playing a strategic game until a weakness developed in the computer’s position, then winning against that weakness.

The game score of round 1 is presented in the form of a Turing experiment. For those not familiar with him, Alan Turing proposed a method for determining whether a machine should be called “intelligent.” In this test, a human, linked via teletypewriter with a machine, is told that he is communicating with either a machine or another human. If he is unable to determine with which of them he is communicating, the machine can be termed “intelligent.” The question: was Levy White or Black in game 1? Consult table 1 and form an opinion. The answer appears in the text box on page 90.

The first game was a draw. This created a great deal of speculation, as most of the

Table 1: The score (record of moves) of game 1 of the match. The reader is asked to examine this game, and to form an opinion concerning which player had which color of pieces.

About the Author

J R Douglas has 16 years of experience as a microprogrammer, and maintains an interest in artificial intelligence. His hobbies include photography and amateur radio (callsign KA0ACN).

Figure 1: Position occurring in round 1 after White’s 12th move. The player of Black next unleashes an attack which wins material and disrupts White’s Kingside.

Figure 2: The final position reached in game 1. The participants agreed to a draw.
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Figure 3: Position reached in game 4 after Black has made his 47th move. The human chess masters present, including Canadian Master Bruce Amos and 14 year old US National Master Joel Benjamin, were of the opinion that White must lose material. White did have a move they missed, and played it.

Figure 4: The final position of game 4. White's pawns will march irresistibly to the eighth rank and become Queens. Black can find no way to stop them, and resigns.

<table>
<thead>
<tr>
<th>Chess 4.7</th>
<th>Levy</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. P-K4</td>
<td>P-K4</td>
</tr>
<tr>
<td>2. N-KB3</td>
<td>P-KB4</td>
</tr>
<tr>
<td>3. PxP</td>
<td>P-K5</td>
</tr>
<tr>
<td>4. N-K5</td>
<td>N-KB3</td>
</tr>
<tr>
<td>5. N-N4</td>
<td>P-Q4</td>
</tr>
<tr>
<td>6. NxB check</td>
<td>QxN</td>
</tr>
<tr>
<td>7. O-R5 check</td>
<td>O-B2</td>
</tr>
<tr>
<td>8. QxQ check</td>
<td>KxQ</td>
</tr>
<tr>
<td>9. N-B3</td>
<td>P-B3</td>
</tr>
<tr>
<td>10. P-Q3</td>
<td>PxP</td>
</tr>
<tr>
<td>11. BxP</td>
<td></td>
</tr>
</tbody>
</table>

Possessing a one pawn advantage, the computer has forced Black's King to remain in the center of the board.

<table>
<thead>
<tr>
<th>Chess 4.7</th>
<th>Levy</th>
</tr>
</thead>
<tbody>
<tr>
<td>11. ...</td>
<td>N-Q2</td>
</tr>
<tr>
<td>12. B-KB4</td>
<td>N-B4</td>
</tr>
<tr>
<td>13. P-KN4</td>
<td>NxB check</td>
</tr>
<tr>
<td>14. PxN</td>
<td>B-B4</td>
</tr>
<tr>
<td>15. O-O</td>
<td>P-KR4</td>
</tr>
<tr>
<td>16. N-R4</td>
<td>B-Q5</td>
</tr>
<tr>
<td>17. B-K3</td>
<td>B-K4</td>
</tr>
<tr>
<td>18. P-Q4</td>
<td>B-Q3</td>
</tr>
<tr>
<td>19. P-KR3</td>
<td>P-QN3</td>
</tr>
<tr>
<td>20. R/B-K1</td>
<td>B-Q2</td>
</tr>
<tr>
<td>21. N-B3</td>
<td>PxP</td>
</tr>
<tr>
<td>22. PxP</td>
<td>R-R5</td>
</tr>
<tr>
<td>23. P-B3</td>
<td>R-R1</td>
</tr>
</tbody>
</table>

At this point, Levy announced to the spectators that he was playing the "Smash-Crash" Gambit, attributed to Josef Smolij of Toronto.

<table>
<thead>
<tr>
<th>Chess 4.7</th>
<th>Levy</th>
</tr>
</thead>
<tbody>
<tr>
<td>24. K-B1</td>
<td>B-N6</td>
</tr>
<tr>
<td>25. R-K2</td>
<td>B-B1</td>
</tr>
<tr>
<td>26. K-N2</td>
<td>B-Q3</td>
</tr>
<tr>
<td>27. B-N1</td>
<td>R-R6</td>
</tr>
<tr>
<td>28. R/1-K1</td>
<td>R-N6 check</td>
</tr>
<tr>
<td>29. K-B2</td>
<td>R/1-R6</td>
</tr>
</tbody>
</table>

Levy has seized command of the King Rook file. The defense is not at all obvious.

<table>
<thead>
<tr>
<th>Chess 4.7</th>
<th>Levy</th>
</tr>
</thead>
<tbody>
<tr>
<td>30. R-K3</td>
<td>B-R3</td>
</tr>
<tr>
<td>31. N-K2</td>
<td></td>
</tr>
</tbody>
</table>

Chess 4.7 forces the exchange of minor pieces, and thereby defangs Levy's attack.

<table>
<thead>
<tr>
<th>Chess 4.7</th>
<th>Levy</th>
</tr>
</thead>
<tbody>
<tr>
<td>31. ...</td>
<td>BxN</td>
</tr>
<tr>
<td>32. R/1xB</td>
<td>P-B4</td>
</tr>
<tr>
<td>33. P-B4</td>
<td>RxB</td>
</tr>
<tr>
<td>34. RxR</td>
<td>R-R6</td>
</tr>
<tr>
<td>35. K-N3</td>
<td>R-R8</td>
</tr>
<tr>
<td>36. B-B2</td>
<td>R-Q6</td>
</tr>
<tr>
<td>37. R-R3</td>
<td>PxP</td>
</tr>
<tr>
<td>38. Rxp check</td>
<td>K-B1</td>
</tr>
<tr>
<td>39. R-Q7</td>
<td>R-Q6 check</td>
</tr>
<tr>
<td>40. K-N2</td>
<td>B-B4</td>
</tr>
<tr>
<td>41. RxP/5</td>
<td>R-Q7</td>
</tr>
<tr>
<td>42. P-N4</td>
<td>BxP</td>
</tr>
<tr>
<td>43. R-Q8 check</td>
<td>K-B2</td>
</tr>
<tr>
<td>44. R-Q7 check</td>
<td>K-B1</td>
</tr>
<tr>
<td>45. RxP/4</td>
<td>R-N7</td>
</tr>
<tr>
<td>46. K-B3</td>
<td></td>
</tr>
</tbody>
</table>

This move avoids the pin of the Bishop to the King — see why in the next move.

<table>
<thead>
<tr>
<th>Chess 4.7</th>
<th>Levy</th>
</tr>
</thead>
<tbody>
<tr>
<td>46. ...</td>
<td>B-B4</td>
</tr>
<tr>
<td>47. R-Q8 check</td>
<td>K-K2</td>
</tr>
<tr>
<td>48. R-R41 check</td>
<td></td>
</tr>
</tbody>
</table>

The human masters present did not see this move. They thought the computer was certain to lose material.

<table>
<thead>
<tr>
<th>Chess 4.7</th>
<th>Levy</th>
</tr>
</thead>
<tbody>
<tr>
<td>48. ...</td>
<td>K-B2</td>
</tr>
<tr>
<td>49. P-N5</td>
<td>P-N3</td>
</tr>
<tr>
<td>50. R-Q7 check</td>
<td>K-B1</td>
</tr>
<tr>
<td>51. PxP</td>
<td>RxB</td>
</tr>
<tr>
<td>52. P-B5</td>
<td>R-R6 check</td>
</tr>
<tr>
<td>53. K-N4</td>
<td>R-R5 check</td>
</tr>
<tr>
<td>54. K-R5</td>
<td>R-Q5</td>
</tr>
<tr>
<td>55. R-QB7</td>
<td>B-K2</td>
</tr>
<tr>
<td>56. P-B6</td>
<td></td>
</tr>
</tbody>
</table>

Black has no way to prevent the steamroller pawns from advancing to the eighth rank.

<table>
<thead>
<tr>
<th>Chess 4.7</th>
<th>Levy</th>
</tr>
</thead>
<tbody>
<tr>
<td>56. ...</td>
<td>Resigns</td>
</tr>
</tbody>
</table>

Table 2: The score of the fourth round game. The computer had the White pieces and the first move. After Levy lost the game, Joe Smolij complained that the Smash-Crash Gambit was for use against people, not machines.

---

Photo 2: Josef Smolij, the guru of the Yonge Street Chess Association, as he presides over his midnight lessons in the Smash-Crash Gambit.
Photo 3: In game 4, David Levy stolidly ponders the position after his move 51... RxP. The computer's material and positional advantage is large, but tenaciously he seeks the best defense.

Photo 4: Levy forms his plan, and reaches out over the flickering electronic chessboard to put it into effect. He may persuade the computer to trade Rooks. Getting rid of Chess 4.7's troublesome Rook would allow some freedom of movement for Levy's beleaguered King.

Photo 5: The computer decides not to trade Rooks. Levy pulls his Bishop back to act as a shield against the final assault. He smiles as he sees that the steamroller pawns will not stop.
assembled experts had predicted a 3 game conclusion to the 6 game match. The rules required that Levy obtain only three points to win his wager. Now play would be forced to at least four rounds. Levy's concentration during the opening phase of the second game did not falter as he quietly put away the machine without apparent trouble.

Round 3 was not scheduled for six days, so the glass booth, looking much like an abandoned bus stop enclosure, sat empty while various masters played simultaneous exhibitions against spectators, amidst the sounds of three bowling lanes and the clank of sabers from the adjacent fencing matches.

Play resumed on September 2. The third round was another closed and quiet game which Levy won without apparent effort. The score then stood ½ to 2½, with Levy needing only a draw to win the match. However, he chose to confront Chess 4.7 directly in the fourth round by playing the Greco Counter Gambit. His decision was made only hours before, while sitting on a milk carton playing chess against Joe Smolij, the Smash-Crash Gambit expert.

Round 4 commenced with fireworks that never died out during the entire game. The moves of that game are given in table 2.

Though Levy finished the match in the fifth round with another closed game and held his 10 year wager, those on the computer chess side of the contest did demonstrate the ability to produce master level games. The most frequently heard comment after the match was that there were no losers in Toronto.

What happens now? A new version of the program, Chess 5.0, waits in the wings, the CYBER 176 spends most of its waking hours hard at work aiding in the design of its successor, and Levy has offered a prize of $5000 to the developer of a system which is able to defeat him in match play within the next five years. Here we go again.

---

Photo 6: David Slate (left), of Northwestern University, and David Cahlander of Control Data Corp watch the computer terminal as it displays one of Chess 4.7's moves in game 4.
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Circle 302 on inquiry card.
Z-80 Assembler

Patrick A Crowe
22 Ringsbury Close
Purton
Swindon ENGLAND SN5 5DE

A Z-80 assembler that implements all of the Zilog defined mnemonics is available from BYTE. This assembler uses the conventions established by Zilog in the Z-80 Assembly Language Programming Manual. It recognizes uppercase characters for labels, operators and operands. All defined pseudo-operations have been implemented except for macroinstructions and conditional assembly commands.

The assembler can be implemented in read only memory. It assumes that a console display and a paper tape reader and punch are available. However, since the user must supply the input and output routines for the program, this is not necessary, and the required functions can point to locations in memory.

The Nybbles Library is an inexpensive means for BYTE readers to share some interesting but specialized forms of software. These programs are written by readers with small computers and printer facilities, and are therefore designed for particular systems. The algorithms and programming techniques in these programs can be directly used by readers with similar equipment, or can serve as an inspiration for improvisation on computers of different characteristics.

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This month "The Z-80 Assembler" (#101) has been added to the Nybbles Library. To order your personal copy, at $4 postpaid, fill out the coupon below.

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Circle 177 on inquiry card.
Interface Your Computer
to a Printing Calculator

Robert H. Astmann
58A Spring St
Red Bank NJ 07701

There are many microprocessor applications in which it is desirable to produce a hard copy of numeric information being measured or computed, yet even the cheapest of today's low cost printers could easily be the most expensive component of such a system. A solution to this problem is to use one of the thermal printing calculators now available. By means of an interface to a microprocessor, the calculator integrated circuit can be given stimuli identical to those received during the normal pushing of the calculator keys. In this article I describe such an interface which was implemented using an Intel 8080A processor and a Texas Instruments 5050M printing electronic calculator.

Basic Control Procedure

I first describe the method by which data is normally entered on a calculator keypad. Referring to figure 1, each button on the keypad provides a unique connection between a column output line and a row input line. The calculator integrated circuit outputs a scan pulse to each column bus sequentially, and looks for an input pulse from one of the rows. The interpretation given to a detected row signal is therefore dependent on which column is being accessed during the given time period.

The job for the microprocessor in this application is to monitor the column signals until the column containing the desired character key is active and then to drive the correct row bus to a high level so that the calculator circuit senses the input while the given column signal is still active. The microprocessor software controls this procedure by using two stored lookup tables (see table 1): a list of column vector bytes and a list of row vector bytes. The entries in these two tables, together with the code for the

Table 1: Contents of the row vector and column vector tables (RWVCT and CLVCT, respectively) referenced by the program in listing 1.

<table>
<thead>
<tr>
<th>Hexadecimal Row</th>
<th>Hexadecimal Column</th>
<th>Key</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vector (RWVCT)</td>
<td>Vector (CLVCT)</td>
<td></td>
</tr>
<tr>
<td>08</td>
<td>01</td>
<td>&quot;0&quot;</td>
</tr>
<tr>
<td>04</td>
<td>01</td>
<td>&quot;1&quot;</td>
</tr>
<tr>
<td>04</td>
<td>02</td>
<td>&quot;2&quot;</td>
</tr>
<tr>
<td>04</td>
<td>04</td>
<td>&quot;3&quot;</td>
</tr>
<tr>
<td>02</td>
<td>01</td>
<td>&quot;4&quot;</td>
</tr>
<tr>
<td>02</td>
<td>02</td>
<td>&quot;5&quot;</td>
</tr>
<tr>
<td>02</td>
<td>04</td>
<td>&quot;6&quot;</td>
</tr>
<tr>
<td>01</td>
<td>01</td>
<td>&quot;7&quot;</td>
</tr>
<tr>
<td>01</td>
<td>02</td>
<td>&quot;8&quot;</td>
</tr>
<tr>
<td>01</td>
<td>04</td>
<td>&quot;9&quot;</td>
</tr>
<tr>
<td>0F</td>
<td>08</td>
<td>&quot;T&quot;</td>
</tr>
<tr>
<td>0F</td>
<td>04</td>
<td>&quot;=&quot;</td>
</tr>
<tr>
<td>01</td>
<td>08</td>
<td>&quot;=&quot;</td>
</tr>
<tr>
<td>08</td>
<td>08</td>
<td></td>
</tr>
</tbody>
</table>

Figure 1: Keyboard arrangement of the Texas Instruments 5050M printing calculator. Calculator logic outputs a scan pulse to each column bus sequentially and looks for an input pulse from one of the rows. This uniquely identifies the key pressed by the user. Although there are only four row inputs to the calculator circuit, there are five rows of keys. Signals from the upper row of keys appear simultaneously on all four row inputs through the diode network.

Figure 7: Keyboard arrangement of the Texas Instruments 5050M printing calculator. Calculator logic outputs a scan pulse to each column bus sequentially and looks for an input pulse from one of the rows. This uniquely identifies the key pressed by the user. Although there are only four row inputs to the calculator circuit, there are five rows of keys. Signals from the upper row of keys appear simultaneously on all four row inputs through the diode network.
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desired character, determine the mapping of a column input into a row output.

**Hardware Interface**

The signalling between the TI 5050M calculator integrated circuit and keypad is illustrated in figure 2. A 17 V pulse of 40 µs nominal duration is outputted to each column bus with the entire sequence being repeated every 7.3 ms. This signalling continues as long as no button is pushed. When a button is pushed, the column signals are extended to about 150 µs to validate the button push. This pulse width is maintained until the button is released, during which time any other button push is ignored. It is immediately apparent that to interface this calculator to the 8080A processor, level translation circuitry in both directions is required. The circuitry I used in this application is shown in figure 3. An Intel 8255 Programmable Peripheral Interface integrated circuit was chosen because it was already interfaced to the 8080A as a keyboard port. The diodes tied to +5 V ensure that the inputs to the 8255 do not go above +5.7 V when a column signal goes to +17 V. The output lines from the 8255 are connected to open collector drivers which translate a +5 V signal to +17 V.

The necessary connection points within the calculator case were easily accessed since there were large metal strips connecting the printed circuit board to the keypad. A dual trace oscilloscope was used to deduce the identity of each connection. Once the columns were identified by noting the time displacement of the scan pulse on each bus relative to the others, the rows were identified by pressing buttons and looking for responses on the connections that normally did not exhibit any signalling.

**Software Interface**

At the heart of the printer control software is the driver program, INTER. INTER is called when a single decimal digit or control character is to be entered. A 4 bit BCD representation of the digit must first be loaded into the C register of the 8080A. As shown in listing 1, this character code is used to select the correct column and row vectors from the two lookup tables contained in table 1.

In my microcomputer system, which is based on an Altair 8800 computer, this program was executed out of programmable memory which utilizes a processor wait

---

**Figure 2**: The sequence of column scan signals outputted by the calculator circuit.

**Figure 3**: Circuitry for interfacing the 8255 programmable peripheral interface to the Texas Instruments 5050M printing calculator. The diodes prevent the inputs to the 8255 from going above 5.7 V when a column signal goes to 17 V. The output lines from the interface are connected to open collector drivers (IC1) which translate the 5 V signals to 17 V.

<table>
<thead>
<tr>
<th>NUMBER</th>
<th>TYPE</th>
<th>+5</th>
<th>GROUND</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>7407</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC2</td>
<td>8255</td>
<td>26</td>
<td>7</td>
</tr>
</tbody>
</table>
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Thinker Toys™

Circle 255 on inquiry card.
grammable peripheral interface. Row vector and column vector (RWVCT and CLVCT) contents are listed in table 1. The first section in the list is the portion of the main program that calls the routines.

<table>
<thead>
<tr>
<th>Label</th>
<th>Op Code</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>LHLD</td>
<td>POINT</td>
<td>load HL with memory data pointer</td>
<td></td>
</tr>
<tr>
<td>MOV</td>
<td>C,M</td>
<td>load C from memory with 2 low order digits</td>
<td></td>
</tr>
<tr>
<td>INX</td>
<td>H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOV</td>
<td>B,M</td>
<td>load B from memory with 2 high order digits</td>
<td></td>
</tr>
<tr>
<td>INX</td>
<td>H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALL</td>
<td>OUTPR</td>
<td>enter the four digits</td>
<td></td>
</tr>
<tr>
<td>MVIC</td>
<td>D0H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALL</td>
<td>LINE</td>
<td>terminate the line</td>
<td></td>
</tr>
<tr>
<td>CALL</td>
<td>SKIP</td>
<td>skip a line</td>
<td></td>
</tr>
</tbody>
</table>

OUTPR:

<table>
<thead>
<tr>
<th>Label</th>
<th>Op Code</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOV</td>
<td>A,C</td>
<td>get 2 low order decimal digits</td>
<td></td>
</tr>
<tr>
<td>STA</td>
<td>SAVE+1</td>
<td>save</td>
<td></td>
</tr>
<tr>
<td>MOV</td>
<td>A,B</td>
<td>get 2 high order decimal digits</td>
<td></td>
</tr>
<tr>
<td>MVIB</td>
<td>D0H</td>
<td>clear B reg for INTER</td>
<td></td>
</tr>
<tr>
<td>CALL</td>
<td>PR2DI</td>
<td>enter 2 high order digits</td>
<td></td>
</tr>
<tr>
<td>LDA</td>
<td>SAVE+1</td>
<td>retrieve 2 low order digits</td>
<td></td>
</tr>
<tr>
<td>JMP</td>
<td>PR2DI</td>
<td>enter 2 low order digits</td>
<td></td>
</tr>
</tbody>
</table>

PR2DI:

<table>
<thead>
<tr>
<th>Label</th>
<th>Op Code</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>STA</td>
<td>RRC</td>
<td>save low order digit</td>
<td></td>
</tr>
<tr>
<td>RRC</td>
<td>RRC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ANI</td>
<td>0FH</td>
<td>BCD value for digit to be entered now occupies right side of accumulator</td>
<td></td>
</tr>
<tr>
<td>MOV</td>
<td>C,A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALL</td>
<td>INTER</td>
<td>enter the high order digit</td>
<td></td>
</tr>
<tr>
<td>LXi</td>
<td>D0F00H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALL</td>
<td>DELAY</td>
<td>delay for calculator response time</td>
<td></td>
</tr>
<tr>
<td>LDA</td>
<td>SAVE</td>
<td>retrieve low order digit</td>
<td></td>
</tr>
<tr>
<td>ANI</td>
<td>0FH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOV</td>
<td>C,A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALL</td>
<td>INTER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LXi</td>
<td>D0F00H</td>
<td>enter the low order digit</td>
<td></td>
</tr>
<tr>
<td>JMP</td>
<td>DELAY</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SKIP:

<table>
<thead>
<tr>
<th>Label</th>
<th>Op Code</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>MVI</td>
<td>C0H</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALL</td>
<td>INTER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LXi</td>
<td>D0</td>
<td>delay for thermal print head response and paper advance</td>
<td></td>
</tr>
<tr>
<td>JMP</td>
<td>DELAY</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

INTER:

<table>
<thead>
<tr>
<th>Label</th>
<th>Op Code</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>LXi</td>
<td>H,CLVCT</td>
<td>HL points to head of column vector table</td>
<td></td>
</tr>
<tr>
<td>DAD</td>
<td>B</td>
<td>HL points to correct column vector byte</td>
<td></td>
</tr>
<tr>
<td>MOV</td>
<td>D,M</td>
<td>load D reg. with column vector</td>
<td></td>
</tr>
<tr>
<td>LXi</td>
<td>H,RWVCT</td>
<td>HL points to head of row vector table</td>
<td></td>
</tr>
<tr>
<td>DAD</td>
<td>B</td>
<td>HL points to correct row vector byte</td>
<td></td>
</tr>
<tr>
<td>IN</td>
<td>PORTB</td>
<td>read status of column signals</td>
<td></td>
</tr>
<tr>
<td>ANA</td>
<td>D</td>
<td>is desired column active?</td>
<td></td>
</tr>
<tr>
<td>JZ</td>
<td>COL</td>
<td>No, keep looking</td>
<td></td>
</tr>
<tr>
<td>MOV</td>
<td>A,M</td>
<td>Yes, prepare to output row signal</td>
<td></td>
</tr>
<tr>
<td>MVIC</td>
<td>C0FH</td>
<td>initialize first delay counter</td>
<td></td>
</tr>
<tr>
<td>INR</td>
<td>C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>JNZ</td>
<td>WAIT1</td>
<td>time to output row signals</td>
<td></td>
</tr>
<tr>
<td>OUT</td>
<td>PORTC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MVI</td>
<td>C0FH</td>
<td>initialize second delay counter</td>
<td></td>
</tr>
<tr>
<td>INR</td>
<td>C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>JNZ</td>
<td>WAIT2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XRA</td>
<td>A</td>
<td>clear accumulator</td>
<td></td>
</tr>
<tr>
<td>OUT</td>
<td>PORTC</td>
<td>reset row signals</td>
<td></td>
</tr>
<tr>
<td>RET</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Label</th>
<th>Op Code</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>INR</td>
<td>E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>JNZ</td>
<td>DELAY</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INR</td>
<td>D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>JNZ</td>
<td>DELAY</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RET</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Listing 1: Assembly language program for interfacing an Intel 8080A processor to a Texas Instruments 5050M printing calculator using an 8255 programmable peripheral interface. Row vector and column vector (RWVCT and CLVCT) contents are listed in table 1. The first section in the list is the portion of the main program that calls the routines.
user.) Hence, at this point in the application program the code for the #/S key is loaded into the C register and the subroutine LINE is called. LINE proceeds to call INTER and then causes a delay of about 0.5 seconds which enables the calculator to activate the thermal print heads and advance the paper. Finally, the subroutine SKIP is called in order to skip a line before printing the next number.

Conclusions

When using a microprocessor in a control application, it is necessary to be able to "shake hands" with the device to be controlled. This is best accomplished by structuring the software so that a low-level driver routine makes the handshaking transparent to the higher level software.

In this application, the signalling protocol of the printing calculator is utilized as a control mechanism by the processor. The interface between the two devices is easy to implement and the result is low cost numeric printing capability. Whenever the calculator is disconnected from the processor interface, it will operate normally again.

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One of the most fascinating and useful products of recent technology is the read only memory (often abbreviated as ROM) and especially useful for the experimental systems designer is the erasable and electrically programmable read only memory, variously abbreviated EROM or EPROM.

In designing my first microprocessor based system, a read only memory was a must to contain the operating system and the floating point arithmetic firmware. I did extensive research into read only memory systems and after a week or so I was ready to make a specification. I had previously chosen the processor for the system to be the MOS Technology 6502 which requires a memory access time of about 500 ns when running with a 1 MHz clock. It was very desirable to have the read only memory meet this specification for two reasons. First, because of the dynamic nature of the 6502, it does not wait for slow memory very readily. Second, and by far most important, I wanted my arithmetic routines in read only memory to run as fast as possible since I would be using them very often. These considerations ruled out the older 1702 type memories as too slow.

The choice was obvious as soon as I read about the Intel 2708. It had all the requisite features: fast (450 ns) access time, large array (1024 8 bit words) on a single chip, and easy straightforward programming. When I designed this programmer the going price was $100; currently the prices have dropped to about $10, making this chip even more desirable.

The chip is also numbered 8708 to fit into Intel’s 8000 line which includes the 8080. The 2708 and the 8708 are identical as far as I know. They are definitely interchangeable at a pin level. There is also a variation of the design called the 2704/8704 which is arranged as an array of 512 8 bit words. The 2704/8704 is electrically and logically identical to the 2708/8708 but contains only half as much memory. The high order address line is not defined for the 2704/8704. (Rumor has it that 2704/8704 parts are identical to 2708s but wired into the package with the high order address bit unconnected.)

System Design

My design called for 4 K bytes of read only memory resident firmware which could be built up over a period of time as the operating system and arithmetic routines were debugged. My approach to this was to prototype the eventual firmware in normal
programmable memory and then transfer it to read only memory after debugging. I designed a 4 K byte read only memory board (photo 1) which has four 2708 PROM chips plus 1 K bytes of programmable memory. The programmable memory can be jumper selected to occupy any 1 K page on the board. This allows for prototyping a routine in the actual address space that it will eventually occupy. The system has worked out extremely well.

It was my original intention to have the read only memory programmed by professionals offsite. My impression was that 2708 programming was somewhat complex and that a programmer board for a limited number of burns was not very practical. After learning more about the 2708 my attitude changed. A little thought convinced me that a computer driven programmer could be simply constructed at minimum cost. It would be very convenient to be able to program the chips in my own computer and to be able to make changes and corrections with a short turnaround time.

Programming the EROM

When initially received, and after each erasure, all the bits of the 2708 are in the "1" state (output high). The content of the 2708 is programmed by selectively changing state to "0" in the desired bit locations. Programming a given byte requires the address of the byte on the address input pins and the data byte on the data pins, all at TTL levels (+5 V) with the write enable pin held at +12 V, a program pulse of +26 V at 20 mA is applied to the program pin. The 2708 specifications require that the program pulse be between 100 µs and 1000 µs wide. A series of pulses are required to program a particular address. Intel recommends that one pulse be administered to each address location in a loop. The number of times the loop must be repeated is a function of the pulse width. The final accumulated program current time to each address must be greater than 100 ms. Such a scheme is a natural for computer control.

The Zapper programming board shown in photo 2 and figure 1 is designed to have the address and data multiplexed to it through a peripheral interface adapter (PIA) with at least eleven output lines. I use the peripheral interface adapter that is available on my MOS Technology KIM-1 single board computer to drive the Zapper. If you do not have one of these PIAs I recommend either the MOS Technology 6520 or the Motorola 6820. The address and data are passed through the lower eight lines (PA0-PA7) while three of the upper lines (PB0-PB2) control the multiplexing and programming current.

The driving computer is expected to direct the following sequence of events which will program one address location in the 2708:

- PB0 is brought high to enable the upper 8212 (IC1) eight bit latch.
- The lower eight bits of the address are loaded on PA0-PA7 and thus into the 8212.
- PB0 is brought low latching the low address onto the outputs of IC1 which are wired to the address inputs of the 2708.
- PB1 is brought high to enable the lower 8212 (IC2). The upper two bits of the address are loaded on PA0-PA1 and latched when PB1 goes low.
- The data byte is loaded on PA0-PA7 and latched by the PIA.
- PB2 is brought high for the pulse time gating the program current to the EROM.

This sequence is repeated the required number of times to program the EROM.

Photo 2: The Zapper board with the EROM in the upper left corner. Data from the PIA as well as logic power and ground come in via the ribbon cable at the bottom which is connected directly to the computer. Program power comes in on the cable in the upper right corner from an external power supply.
Figure 1: The address and data information for the Zapper is multiplexed through the PIA ports PA0-PA7 while control signals are presented on PB0-PB2. PB0 is connected to the enable pin of the upper 8212 which latches the lower eight bits of the address. The high two bits of the address are loaded and latched on the lower 8212 by PB1. The data byte is latched by the PIA. When PB2 goes high, program power is gated to the program pin of the 2708 by the 3 transistor high current gate in the lower right.
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A burn pulse for each location. The cycle is repeated so that each location receives 255 pulses. The end of the program is signaled by the Teletype bell or terminal signal.

Later it is used in the pulse timing loop simply to cut down the programming pulse time to program the 2708. The start and end plus one addresses of the programmable memory block are loaded in BSL, BSH and BEL, BEH registers respectively before execution is begun. Data is programmed into the same relative addresses in the read only memory as they are found in the programmable memory; ie: the low ten bits of the address are the same.

Notice that the 2708 can be partially programmed. If the memory block to be copied is less than 1024 bytes long, only the appropriate bytes are programmed. The remaining locations are unchanged. The block to be programmed can start and end anywhere in the 1 K page. This is a very useful feature as it allows firmware to be developed over a period of time. The partially programmed read only memory can be used in the meantime. Incidentally, listings 2 and 3 are subroutines only for the sake of modularity and the whim of the author. They are called at only one point each.

It is very important that the +26 V programming power be off at the power supply before the computer has had a chance to latch PB2 low. After this initialization, a pause is implemented by waiting for input from a terminal in subroutine MSG, listing 3. The application of program power before the computer has initialized the Zapper board will usually result in some random location being burned with some random data.

Erasing the EROM

The 2708 is very easily erased using an ultraviolet light source. Intel specifications indicate that an integrated dose of 10 watt-sec/cm² at a wavelength of 2537 angstroms is required to erase the 2708. A quick glance at the CRC Handbook of Chemistry and Physics shows that 2537 angstroms is the most persistent spectral line of mercury (Hg). This means that any mercury vapor lamp will do the trick. I use a nice packaged source from MSC Macalaster (Catalog #3400) which slips over the top of the read only memory. (When using the unit, discard the filters which come with it, and be sure you shield your eyes from the lamp.) The chip

Software

The driving software, as shown in listings 1 to 4, implements the above sequence of events in a double loop. The inside loop, listing 2, works its way through all the addresses to be programmed and gives each location a 600 µs programming pulse. The outer loop, listing 1, repeats the process 255 times giving a total program current time of 153 ms to each bit. This is sufficient time to program the 2708. The start and end plus one addresses of the programmable memory block are loaded in BSL, BSH and BEL, BEH registers respectively before execution is begun. Data is programmed into the same relative addresses in the read only memory as they are found in the programmable memory; ie: the low ten bits of the address are the same.

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Listing 3: The MSG routine effectively causes a pause so that programming power may be turned on after the Zapper board has been initialized. Execution is resumed when any key on the Teletype is pressed.

should be stuck in a piece of conducting foam while erasing. An exposure time of 30 to 40 minutes will yield a fresh chip ready to be programmed again. If you want to make your own eraser, use the GE #G4S11 4 W mercury vapor lamp with a GE #89C504 ballast. Both of these items are usually available at commercial electrical supply houses. The exposure time is about 40 minutes with the 2708 placed 1 cm from the bulb.

My experience shows that each successive time a 2708 is erased the exposure time to completely erase it increases. As the total energy needed to erase it is cumulative, extra short exposures can be given as needed. A little program to check each byte for all ones will assure that the memory is fully erased.

It is also convenient to remember that any 1 bit in the EROM can be changed to 0. Sometimes a single byte needs to be modified and this can occasionally be done without erasing the EROM and reprogramming it. This has been the case for me more often then statistics would dictate. Someone else must not been so lucky.

REFERENCES
1. Intel Data Catalog, Intel Corp, 1975.

Listing 4: External symbol table. The PIA registers (PAD, PADD, PBD, PBDD) are those assigned on the KIM-1 board. OUTCH and GETCH respectively output and input one character each to or from a terminal. They are part of the KIM-1 operating system.

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<tr>
<th>HEX DECIMAL LOCATION</th>
<th>SYMBOL</th>
<th>COMMENTS</th>
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<tr>
<td>0000</td>
<td>BSL</td>
<td>STARTING ADDRESS OF PROGRAMMABLE MEMORY</td>
</tr>
<tr>
<td>0001</td>
<td>BSH</td>
<td>ENDING ADDRESS PLUS ONE OF PROGRAMMABLE MEMORY</td>
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<td>0002</td>
<td>BEL</td>
<td>WAIT REGISTER</td>
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<td>0003</td>
<td>BEH</td>
<td>CYCLE COUNT REGISTER</td>
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<td>0004</td>
<td>LRH</td>
<td>LOCATION REGISTER</td>
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<td>PAD</td>
<td>PA PORT DATA REGISTER</td>
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<td>PADD</td>
<td>PA PORT DIRECTION REGISTER</td>
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<td>1703</td>
<td>PBDD</td>
<td>PB PORT DIRECTION REGISTER</td>
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<td>OUTCH</td>
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<td>GETCH</td>
<td>TTY INPUT ROUTINE</td>
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<tr>
<td>1706</td>
<td>IFPSA</td>
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An Easy Programming System

Joseph Weisbecker
1220 Wayne Av
Cherry Hill NJ 08002

This article describes a hexadecimal interpretive programming system which requires less hardware than high level languages such as BASIC, and which I feel is much easier to use than machine language. In my experience, hexadecimal interpretive programming is ideally suited to real time control, video graphics, games or music synthesis. It can be used with inexpensive computer systems consisting of a hexadecimal keyboard and only 1 K or 2 K of programmable memory. Expensive terminals and large memories aren't required. You can quickly and easily write useful programs that require five to ten times less memory than conventional high level languages without resorting to the tedious complexities of actual machine language.

Interpretive Programming

This programming approach isn't new, but surprisingly few people seem to be using it. The technique consists of designing a high level pseudomachine language that is more powerful for specific applications than conventional machine language. An interpretive program is then written to execute this new set of pseudoinstructions. Each pseudoinstruction is really just a code that specifies a machine language subroutine. This set of subroutines can be designed to perform any functions you might need for your application. By staying with a machine language format, and not using labels or English words for instruction codes, memory requirements are lower. By limiting the addressing range and number of variables, you can limit each pseudoinstruction code length to several bytes for further memory space savings. Interpretive programs for these powerful pseudomachine languages can require as few as 512 bytes of memory. It has seldom taken me more than a week to implement a new hexadecimal interpretive language, and I can then use it for years. The approach can be thought of as vertical microprogramming with the microprocessor machine language used as the microcode representation.

To illustrate the compactness of these types of programs, I wrote a video tic-tac-toe program using the CHIP-8 language described below. Only 500 program bytes were required versus 3000 bytes for an equivalent version written in BASIC. Besides saving memory, this also meant 2000 fewer keystrokes for initial program entry. In addition, the CHIP-8 interpreter was about eight times smaller than the BASIC interpreter. The CHIP-8 program ran on a 1.5 K memory system with a hexadecimal keyboard, while the BASIC program required an 8 K system with an ASCII keyboard and alphanumeric display. The CHIP-8 program took about 12 hours to design, hand code, enter and debug. I suspect that the BASIC version took at least as long on a much more expensive system.

This hexadecimal interpretive programming approach is important for two reasons. First, it reduces the cost of the hardware you need to get started in home computing. Second, it drastically reduces the amount of read only memory required in microprocessor based products such as controllers and video games. Read only memory cost is a significant factor in these types of products.

A detailed example will be used to illustrate the hexadecimal interpretive programming approach. The new RCA COSMAC VIP computer will be used for this example (see August 1977 BYTE, page 30, for a description of this computer). It is a low cost, single card computer containing 2048 bytes of programmable memory, a graphic video display, and a hexadecimal keyboard. I had this type of programming in mind when I incorporated features such as multiple program counters in the COSMAC (1802) microprocessor architecture.

The pseudomachine language used in my example will be one called CHIP-8, designed for use with the COSMAC VIP system. I will
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discuss using this language rather than describing the interpreter for it. Suffice it to say that the interpreter only requires 512 bytes and resides at memory locations 0000 to 01FF (hexadecimal). Programs written in the CHIP-8 language must start at memory location 0200 (hexadecimal). The sample program described will run on a 1024 byte memory system. This includes the CHIP-8 interpreter, the program, work area and video display refresh buffer. The program itself only requires 60 CHIP-8 instructions.

CHIP-8 Language

Table 1 describes the 31 CHIP-8 instructions provided in this pseudomachine language. Each instruction requires only two bytes (four hexadecimal digits). Memory addressing is limited to 4096 bytes so that only three hexadecimal digits are needed to specify a memory address. The number of variables has been limited to 16, labeled V0 to VF in this article. These are 1 byte variables or registers that can be modified or examined by CHIP-8 instructions. There is also a 2 byte memory address register called I, which is used by certain instructions. A real time clock or timer is provided. This timer can be set to any hexadecimal value between 00 and FF by the FX15 instruction. For example, if V2 contained hexadecimal 0A, an F215 instruction would set the timer to 0A. This timer is automatically decremented by one 60 times per second until it reaches 00. If the timer was set to 3C (decimal 60) it would reach 00 exactly 1 second later. This timer can be used to provide delays in game or control programs. A tone clock is also provided which can be set to cause a tone lasting from 1/60 to about 4 seconds.

An important feature of this type of language is that all variables (registers) are contained in memory. This means that debugging is generally limited to examining memory locations, not internal microprocessor hardware registers. Astute readers will be wondering why I maintained a fixed 2 byte instruction length when variable instruction length was possible. Since absolute memory addresses are used, fixed 2 byte instructions avoid addressing confusion that increases programming errors. Also, any instruction can easily be replaced by a branch instruction of the same length for debugging breakpoints or program patching.

Graphic Display Approach

Before proceeding with a detailed programming example, readers will need to understand the video display system. Figure 1 shows the graphic display format used.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1MMM</td>
<td>Go to 0MMM</td>
</tr>
<tr>
<td>BMMM</td>
<td>Go to 0MMM + VO</td>
</tr>
<tr>
<td>2MMM</td>
<td>Do subroutine at 0MMM (must end with 00EE)</td>
</tr>
<tr>
<td>00EE</td>
<td>Return from subroutine</td>
</tr>
<tr>
<td>3XKK</td>
<td>Skip next instruction if VX = KK</td>
</tr>
<tr>
<td>4XKK</td>
<td>Skip next instruction if VX ≠ KK</td>
</tr>
<tr>
<td>5XY0</td>
<td>Skip next instruction if VX = VY</td>
</tr>
<tr>
<td>9X0Y</td>
<td>Skip next instruction if VX ≠ VY</td>
</tr>
<tr>
<td>EX9E</td>
<td>Skip next instruction if VX = hexadecimal key (LSD)</td>
</tr>
<tr>
<td>EXA1</td>
<td>Skip next instruction if VX ≠ hexadecimal key (LSD)</td>
</tr>
<tr>
<td>6XKK</td>
<td>Let VX = KK</td>
</tr>
<tr>
<td>CXKK</td>
<td>Let VX = Random Byte (KK = Mask)</td>
</tr>
<tr>
<td>7XKK</td>
<td>Let VX = VX + KK</td>
</tr>
<tr>
<td>8XY0</td>
<td>Let VX = VY</td>
</tr>
<tr>
<td>8XY1</td>
<td>Let VX = VX/VY (VF changed)</td>
</tr>
<tr>
<td>8XY2</td>
<td>Let VX = VX &amp; VY (VF changed)</td>
</tr>
<tr>
<td>8XY4</td>
<td>Let VX = VX + VY (VF = 00 if VX + VY &lt; FF, VF = 01 if VX + VY &gt; FF)</td>
</tr>
<tr>
<td>8XY5</td>
<td>Let VX = VX - VY (VF = 00 if VX &lt; VY, VF = 01 if VX &gt; VY)</td>
</tr>
<tr>
<td>FX07</td>
<td>Let VX = current timer value</td>
</tr>
<tr>
<td>FXOA</td>
<td>Set timer = VX (01 = 1/60 second)</td>
</tr>
<tr>
<td>FX15</td>
<td>Set tone duration = VX (01 = 1/60 second)</td>
</tr>
<tr>
<td>AMMM</td>
<td>Let I = 0MMM</td>
</tr>
<tr>
<td>FX1E</td>
<td>Let I = I + VX</td>
</tr>
<tr>
<td>FX29</td>
<td>Let I = 5 byte display pattern for LSD of VX</td>
</tr>
<tr>
<td>FX33</td>
<td>Let MI = 3 decimal digit equivalent of VX (I unchanged)</td>
</tr>
<tr>
<td>FX55</td>
<td>Let MI = VO : VX (I = I + X + 1)</td>
</tr>
<tr>
<td>FX65</td>
<td>Let VO : VX = MI (I = I + X + 1)</td>
</tr>
<tr>
<td>000E</td>
<td>Erase display (all 0s)</td>
</tr>
<tr>
<td>DXYN</td>
<td>Show n byte MI pattern at VX-VY coordinates.</td>
</tr>
</tbody>
</table>

Table 1: CHIP-8 instruction set. Note that invalid hexadecimal characters in the hexadecimal instructions listed are replaced by valid hexadecimal codes when a program is written. Thus B1000 might be a valid use of the BMMM instruction.
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Figure 1: A drawing of the video display. The inner dashed square is the playing area. The range of X and Y is shown.

The dotted line indicates the area of the screen used for display. This display area consists of an array of spot positions 64 wide by 32 high. These spot positions represent bits in a 256 byte page of memory. When a memory bit is one, the spot position is on (white). The CHIP-8 language specifies spot positions on the screen by an XY coordinate system as shown in figure 1. The values of the X coordinate (horizontal spot position) can run from 00 to 3F (0 to 63 decimal). The values of the Y coordinate (vertical spot position) run from 00 to 1F (0 to 31 decimal). Any two variables (V0 to VF) can be used to specify the X and Y coordinates of a spot position on the screen.

The display instruction (DXYN) lets you show a pattern of spots on the screen. This pattern of spots can form a picture, letter, number, etc. Patterns are represented in memory by a list of one to 15 bytes. Suppose you want to display a rocket ship. You must first construct a rocket ship pattern on grid paper as illustrated in figure 2. The hexadecimal codes for this pattern can then be derived directly from the bit pattern.

To show this rocket ship on the screen with a DXYN instruction, you must first set I to the address of the rocket ship pattern byte list in memory. You must then set two variables to the X and Y coordinates at which you want the rocket ship pattern to appear on the screen. The X and Y coordinates specify the position of bit 7 of the first pattern byte on the screen. For example, the following short program would show the rocket pattern of figure 2 at the top left corner of the screen:

<table>
<thead>
<tr>
<th>Memory Address (Hexadecimal)</th>
<th>Instruction Code</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0200</td>
<td>6200</td>
<td>Set V2 = rocket X coordinate = 00</td>
</tr>
<tr>
<td>0202</td>
<td>6300</td>
<td>Set V3 = rocket Y coordinate = 00</td>
</tr>
<tr>
<td>0204</td>
<td>A20A</td>
<td>Set I = rocket pattern address = 020A</td>
</tr>
<tr>
<td>0206</td>
<td>D236</td>
<td>Display 6 byte rocket pattern</td>
</tr>
<tr>
<td>0208</td>
<td>1208</td>
<td>End loop</td>
</tr>
<tr>
<td>020A</td>
<td>2070</td>
<td>Rocket pattern byte list</td>
</tr>
<tr>
<td>020C</td>
<td>70F8</td>
<td></td>
</tr>
<tr>
<td>020E</td>
<td>D888</td>
<td></td>
</tr>
</tbody>
</table>

The last hexadecimal digit of the display instruction (DXYN) must always specify the number of bytes in the pattern to be shown on the screen. The DXYN instruction compares each bit of the new pattern to be displayed with whatever is already displayed on the screen at the same spot positions. If a 1 bit is already displayed at the same position as a 1 bit in the new pattern to be displayed, a 0 will be shown on the screen at this spot position, and VF will be set to 01. In other words, the new pattern to be shown is combined with the pattern already showing on the screen via an EXCLUSIVE OR function. This means that after a pattern is shown on the screen it can be erased by showing the same pattern again with the same X and Y coordinates. Incrementing the X or Y coordinate and showing the pattern a third time would cause the illusion of motion. If the value of VF is 01 after showing the pattern on the screen, it means that the pattern touched or hit a previously displayed pattern.

The DXYN instruction permits displaying, erasing and moving individual patterns on the video screen. The ability to detect when one pattern meets another permits you to program chase, paddle and target games.

Decimal Digits and Random Bytes

Several instructions are provided to permit displaying decimal numbers on the video screen. These are useful for game scorekeeping, etc. An FX33 instruction converts the value of any variable (VX) to decimal form. Suppose I=0442 and V9=A7 (hexadecimal). An F933 would cause 01 to be stored in memory location 0422 (hexadecimal), 06 in 0423, and 07 in location 0424.

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Photo 1: The actual video display of the game showing the rocket, UFO and score.

Since A7 in hexadecimal equals 167 in decimal, we see that the three bytes addressed by I represent the decimal equivalent of the value of V9. If I=0422, an F265 instruction could then be used to set V0, V1 and V2 to the values of the three bytes addressed by I above (01, 06 and 07). An FX29 instruction can then be used to set I to a 5 byte pattern representing any one of the three decimal digits. An F229 instruction would leave I addressing a 5 byte pattern for displaying the least significant decimal digit (7 in this example). A DXY5 instruction can then be used to display the decimal digit on the video screen at any desired position.

The above example illustrates the use of an FX65 instruction to transfer three memory bytes to three variables (V0 to V2). The FX55 instruction will store any number of variables in memory locations starting at the I address. These two instructions can be used to increase the number of variables by swapping sets of variables and memory bytes. Just remember that variables are always copied to or from memory in groups starting with V0 and ending with VX, inclusive.

It is often useful to generate random byte values. The CXKK instruction sets any variable (VX) to a random byte value. This random byte will have any bits matching 0 bit positions in KK (a 2 digit hexadecimal number) set to 0. For example, a C407 instruction would set V4 equal to a random byte value between hexadecimal values 00 and 07.

The remainder of the CHIP-8 instructions should be self-explanatory. The 2MMM instruction will transfer control to a subroutine which must be terminated by

Figure 3: The range of rocket X values is from hexadecimal 0F to 2E. Rocket Y is decremented from hexadecimal 1A to 00. The UFO Y remains a constant hexadecimal 08, while the UFO X is incremented from hexadecimal 00 to 39.
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<tr>
<td>32-63 chips</td>
<td>7</td>
</tr>
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Designing a Video Game Program

A detailed example will illustrate how easily the CHIP-8 language can be used to program a real-time video game. The first step always involves specifying the video display and the functions to be programmed. Figure 3 shows the display format chosen for this game. An enemy UFO will be constantly moving from left to right across the top of the screen. A single digit score will be displayed at the lower right. A rocket ship will appear at a random horizontal position along the bottom edge of the display area. You can launch this rocket by pressing key F on the hexadecimal keyboard. The rocket will then move vertically toward the top of the screen. When it reaches the top or hits the target UFO it will be erased and a new rocket will appear at the bottom of the screen. After nine rockets have been launched the game ends and no new rockets will appear. If you hit the UFO with a rocket the score is incremented by 1.

After specifying the positions of the various game patterns on the video screen as shown in figure 3, you must decide on how the 16 variables will be used in the program. Table 2 illustrates how we will use the variables in this example. Six variables (V3, V4, V5, V6, V7, V8) are needed to specify the X and Y coordinates of the three types of patterns involved (score, target UFO and rocket). We need two more variables (V1, V2) to keep track of the current score and number of rockets launched. V9 will be used as a flag that shows whether or not the current rocket has been launched. VA will be set to 01 if the rocket hits the UFO (i.e., point scored) and V0 will be used for a working register in the program. VF is the hit flag and is automatically set to 01 when a hit occurs.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>V0</td>
<td>Temporary variable</td>
</tr>
<tr>
<td>V1</td>
<td>Score (00 at start)</td>
</tr>
<tr>
<td>V2</td>
<td>Rocket counter (00 at start)</td>
</tr>
<tr>
<td>V3</td>
<td>Score X (38)</td>
</tr>
<tr>
<td>V4</td>
<td>Score Y (18)</td>
</tr>
<tr>
<td>V5</td>
<td>UFO X (00 at start)</td>
</tr>
<tr>
<td>V6</td>
<td>UFO Y (08)</td>
</tr>
<tr>
<td>V7</td>
<td>Rocket X (random, 0F to 2E)</td>
</tr>
<tr>
<td>V8</td>
<td>Rocket Y (1A at start)</td>
</tr>
<tr>
<td>V9</td>
<td>Rocket fired flag (00=no, 01=yes)</td>
</tr>
<tr>
<td>VA</td>
<td>Score increment (00 or 01)</td>
</tr>
<tr>
<td>VF</td>
<td>Hit flag (00 or 01)</td>
</tr>
</tbody>
</table>

Table 2: Rocket program variables. VB, VC, VD and VE are not used in this program.

Flowcharting the Game

I believe you should always construct a detailed flowchart, such as the one shown in figure 4. Proper flowcharting will save hours of debugging and will simplify making future changes to your program. A flowchart also lets you see the major and minor loops in your program, allowing you to avoid timing bugs that can occur in real-time situations such as video games.

Step 1 involves initializing the score and rocket counters, as well as the X and Y coordinates for the target UFO and on-screen score digit. The UFO pattern is shown on the screen so that it can subsequently be moved. In step 2 the latest score is shown on the screen, and V2 is checked to see if the game should end because nine rockets have been fired.

Step 4 performs the operations required to show a new rocket at the bottom of the screen. The rocket count is incremented by 1 for each new rocket. The rocket pattern Y coordinate is set to hexadecimal 1A so that the rocket will appear at the bottom of the screen. The rocket X coordinate is set to a random value between hexadecimal 0F and 2E so that it will appear at a random horizontal position without interfering with the score digit. The flag V9 is set to 00 to indicate that the rocket has not yet been fired. The rocket is then shown on the screen and the program proceeds to the loop containing steps 5, 6 and 7.

This loop causes the target UFO to continuously move across the top of the screen while waiting for key F to be pressed. The UFO is randomly moved zero, one, two or three spot positions to the right each time the loop is executed. This gives it a rather fast, randomly varying rate of motion, making it harder to hit. The movement of the UFO merely involves incrementing its X coordinate (V5). When V5 is incremented past the right edge of the display area, wrap around automatically occurs so that the UFO reappears at the left edge of the display area. This wrap around automatically occurs when any X or Y coordinate of any display pattern is incremented or decremented past any edge of the 64 by 32 bit display area.

When key F is pressed to launch the rocket, step 6 causes V9 to be set to 01. Step 7 then causes step 8 to be included in the loop. Step 8 checks the value of the system real-time clock (or timer) to see if it has reached 00 yet. When the timer reaches 00 the rocket is moved up one spot position, and the timer is reset to a value of 03 (1/20
Most features of ALTAIR Extended BASIC are included PLUS these added features:
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Price is $100 on CP/M diskette with documentation. (CP/M is a product of Digital Research.)

SPOOLER

This 8080 program will save many hours of computing time. It intercepts all output to the list device, spools the output to a high-speed disk file, and directs the spooled data to a low-speed printer during unused cycle time while the CPU waits for transfer of data to and from the console. System throughput is greatly increased with the aid of SPOOLER. Output is never lost due to insufficient memory allocation. Fully compatible with the CP/M file system, SPOOLER permits parallel processing without hardware interrupt, and with minimal impact on other processes.
Price: $70.00 (Copyright K.L.H. Systems.)

BASIC-E Compiler

Designed to work with CP/M Disk Operating System this software requires a total of 20K bytes of memory. Included are 26 compiler error messages and 23 run-time error messages. Disk files may be read, written or updated by using both sequential and random access. Included are blocked and unblocked files. Price for compiler and run-time monitor on diskette is $10.00. Manual is available separately for $5.00. (Public domain software by Gordon E. Eubanks, Jr.).

CP/M 1.4 Update Package

A TARBEELL Update Package for those now using CP/M 1.3 is now available on diskette. The Update Package adds new commands and the ability to access four disk drives, as well as 21 new CP/M manuals, TARBELL CP/M User’s Guide and a new BIOS listing.
Price: $50.00.

CBASIC Programming System

Upward compatible from BASIC-E, CBASIC is similar but expanded to include several business oriented facilities, allowing decimal computations to 14 digits of precision, data formatting and PRINT USING statements. Statements allow access to disk files and disk file maintenance. Strings of characters may be read from the console to permit correct input line format to be checked before reading data. General programming features include variable names up to 31 characters, optional line numbers, dynamic debugging tracers, and optional data output to printer. CBASIC on diskette and manual priced at $100. (Copyright Software Systems.)

EMPL-an 8080 APL

Especially suited to educational applications, EMPL is an adaptation of APL, using the ASCII character set. Only one-dimension arrays are allowed. This 8K version occupies the first 5376 bytes of memory and operates in two modes. The Execution Mode permits all instructions to be executed immediately. The Definition Mode permits the user to enter functions. EMPL on Tarbell Cassette with manual is $15. (Copyright 1977 Erik Mueller).

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Figure 4: Flowchart for rocket game.
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Coding and Debugging the Final Program

The final program is shown in figure 5. To translate the flowchart into CHIP-8 instructions, start by listing even numbered hexadecimal memory addresses in the first column, as shown in figure 5. Fill in the third column with an abbreviated description of the function to be performed by each instruction. It is usually most convenient to locate subroutines and pattern byte lists at the end of the program. Labeling the appropriate program addresses with the flowchart step numbers will also prove helpful. The actual hexadecimal codes for the CHIP-8 instructions can then be written in column 2 and entered into the COSMAC VIP memory using the hexadecimal keyboard.

To debug the program, replace the 4209 instruction at memory location 0212 with a 1212 branch instruction. When the program runs, it will stop at location 0212 since the 1212 branch loops on itself. If the UFO and a 0 digit initial score show on the video screen, you know execution was proper up to location 0212. Replace the

Figure 5: The rocket program code in CHIP-8 hexadecimal interpretive language instructions. The steps specified relate directly to the flowchart given for the game in figure 4.
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1212 branch with the original 4209 instruction and put a similar idle loop branch further down in the program for the next test run. In this way you can identify which program steps are causing a problem. If you need to change any portion of the program, just insert a branch instruction to a patch added at the end. Designing, coding and debugging this simple game program required about eight hours. Actual coding and loading the program into memory required less than an hour of this time.

The sample program was kept simple for ease of understanding. Even in this simplified form it is a challenging game to play. The speeds of the rocket and UFO can be easily adjusted to make scoring more or less difficult. Adding multiple targets and 2 digit scoring is possible. Multiple rocket launch angles or after-launch steering could be incorporated. Exploding UFO patterns could be shown when one is hit.

Conclusions

Hexadecimal interpretive programming provides an easy way to program small computers. This approach requires fewer instructions and is much easier than machine language programming. On the other hand, hexadecimal interpretive programming requires much less hardware overhead cost than do high level languages such as BASIC.

A detailed example was provided to illustrate this interpretive approach for a real time video game. The RCA COSMAC VIP and CHIP-8 language were used in this example, although other hexadecimal interpretive languages are possible, and a similar approach can be used with other microcomputers. The steps required in programming with a language such as CHIP-8 are the same as required when using any language: you must specify the functions required, decide on variable and memory utilization, prepare a flowchart, check the flowchart, do the detailed coding, load the code, and debug to the extent required to get the program running properly. Only the last two steps involve using the hardware. Skipping any of the earlier steps will invariably lead to excessive machine debugging time no matter what language is used.

If you’ve never tried a language such as CHIP-8, you may be surprised at how easy it is to use. If you have a limited budget you will certainly appreciate the savings in hardware over conventional high level languages. Last but not least, you might even discover that designing your own hexadecimal interpretive language is also fun.■
6800 Debug Package

The TSC 6800 Debug Package provides a better way to trap program bugs. It is an extremely powerful and complete assembler language program debugging tool which is capable of simulating all functions of the 6800 microprocessor, including interrupts and I/O operations. It is an ideal substitute for hardware logic analyzers or CPU emulators at only a fraction of the cost.

Any number of breakpoints may be user defined. Each breakpoint may invoke any one or combination of eight different actions. These actions may be dependent on a user defined condition such as register A=$FF or memory location $1B55=0. The actions may also be delayed or limited by a pass count. Histogram breakpoints may be set to enable profiling of the executed program. Breakpoints may be set in RAM or ROM!

Complete simulation control allows trace mode to be enabled at anytime. During trace, registers and opcode mnemonics are displayed after each instruction is executed. Single or multiple instruction stepping is permitted as well as simulation speed control. The trace back feature allows the past 256 executed instructions to be viewed. Program execution may be halted at anytime by operator command.

Memory protection and traps are another key feature. Any section(s) of memory may be write, execute, memory, or simulate protected. Execution traps allow program exit on general conditions such as interrupt instruction, transfer instruction, subroutine nest count, and instruction count timeout.

General features include a line at a time assembler, disassembler, memory interrogation commands, hex calculator, machine states counter, stack protection, register modifier, and mode control. In all, there are over 50 commands available. The manual includes detailed operating instructions as well as the complete commented source listing. Requires 9K at $3000.

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Send 25¢ for a complete catalog of TSC’s assembler language software for the 6800, 8080, and 6502.
Who doesn't want a tutor who is infinitely patient, expert on almost any subject under the sun, available at your beck and call, adapted to your learning speed and style, and cheap? This has attracted the attention of a number of the manufacturers of personal computers, and several of them make prominent reference to educational applications in their advertising. But the customer who uses educational applications to justify raiding the family budget for a computer will have some explaining to do, for good teaching software on microcomputers is not available, nor is it easy to write. Why?

If you examine the 20 years of development of computer assisted instruction (CAI) on mainframe computers, you'll see that the computer can be an effective teaching tool when used properly. Students taught with a computer perform as well or better than comparison groups; they may learn two or three times faster. Their failure rate is lower and they express satisfaction with the technique. Why then is the technique not more widely used? There are three main reasons.

First, teachers are conservative. In fairness we also must realize that teachers have heard too many extravagant claims for the miracle that this or that piece of educational technology will produce; their cynicism is understandable. Proponents of computer assisted instruction have not always been conservative (nor have they always been accurate). The cost of hardware is also seen to be prohibitive. Exceptions exist, but the most visible (ie: highly funded) systems are costly to purchase or lease. Third, the creation of high quality software is a difficult and time consuming task which to this point has provided little compensation beyond personal satisfaction.

The personal computer will eliminate two of the reasons. Teachers are discovering computers through their own efforts and through stimulation provided by students and parents who have computers in their homes. The major price breaks in the cost of hardware have resulted from the introduction of smaller machines. Minicomputer systems will possibly cost less than 10 percent of minicomputer systems (using in all cases initial capital outlay, the most relevant number for individuals or small institutions). What remains is to create appropriate software for teaching with a microcomputer.

Before we attempt to write good teaching software, there are some rather fundamental questions to be answered. First, what do we mean by good teaching? A more useful question might be, "What is good teaching not?" One relevant answer for computer teaching is, "Good teaching is not just testing."

Most programs described as teaching programs are programmed tests; the format is exclusively question, accept answer, one message for right, and a second for wrong. Random selection of messages from a list may defer boredom a bit, but that feature alone does not change a test into teaching.

Good teaching is not repetitious to the point of boredom. That's an obvious statement, but it poses a dilemma for those who would teach with the computer, because the efficient use of a computer usually involves repeated use of sections of code. The resolution of the dilemma is to write long and varied course software which can be used by a large number of students.

Good teaching does not force each student to proceed by the same path. Addition of hints or partial solutions for every question on a programmed test does not make that program a good teaching program. If each wrong answer is diagnosed, and a hint or partial solution which builds on the correct portions of that particular wrong answer is given, then we may have a good teaching tool.

Good teaching does not consist of a random collection of available bits and pieces. This implies that we should think in terms of sizable units which can become significant components of a course or subject.

Finally, we should not forget that good teachers are most often experienced teachers and that any occasional lack of enthusiasm on their part about the teaching efforts of well-meaning parents is not invariably misguided.

Another important question is, "What are we trying to teach?" This question is especially important for the personal computer user because the output devices commonly used cannot provide the notation which the students use elsewhere. Books are not written in uppercase only; exponents are not usually written with arrows or double
asterisks; yes and 1 are not synonymous, nor are no and 0; the answer to every question is not a, or b, or c, or d — none of the above. If we attempt to teach using devices which impose notation limitations, we ask ourselves repeatedly, “Are we teaching what we want to teach, or are we teaching how to use and cope with the limitations of the software?”

With these points in mind let us now consider computer languages for teaching. Some teaching languages are based on a teaching strategy; others are based on software functions. Our experience is that the latter types are far superior to the former, for they allow implementation of a variety of teaching strategies. Examination of a large variety of good computer assisted instruction materials shows that they are built from a small number of operations.

For example, one must be able to send text to and accept text from the terminal. Call these functions type and accept (or T and A). (The notation herein is the PILOT notation; for a more complete description of the language see “Computer Assisted Instruction on a Microcomputer,” November 1978 BYTE, page 90.)

Having accepted text, one must be able to analyze it. This is usually done with some type of a match (M) algorithm. One also needs some kind of jump (J) instruction, instructions for subroutine calls and returns (U and E), and some kind of compute (C) instruction so that one can use the full range of numerical and string operations normally associated with computers. Finally one needs some way to make execution of at least some of these instructions (at a minimum, the jump) dependent on the values of various variables or on the success or failure of certain matches.

The obvious question for the microcomputer fan is, “Can I use BASIC?” Unfortunately, the answer is, “Only with extreme difficulty.” Typing text is no problem, and accepting input from the terminal can be handled. Accepting an input of two when you programmed INPUT X and expected the answer 2 will take some extra code, but we’ve already learned that these are going to be long programs by usual computer standards. The difficulties with accepting data pale in significance when compared to the difficulties with match.

Consider an extremely simple case: a question that can be answered yes. Write BASIC code which will match any of the following:

yes, Yes, YES, O.K., OK, Of course, Sure, Always.

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The text of The Computer Book is presented in such a clear, down-to-earth style that it makes an ideal introductory reference for anyone, student and non-technician alike, who wishes to improve his/her understanding of the digital world. Contents include:

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but which will not match any of these:

yesterday, yes and no, yes or no, Alyeska, eyes.

In a good teaching language it can be done in a single line. It could be done in BASIC, at least in a BASIC with a full range of string operators, but in practice no one bothers because it's so much easier to tell the student to answer 1 for yes. One could program the match algorithm of a good teaching language in BASIC as a subroutine, but the resulting code is too slow. It seems then that BASIC (and other computational languages, such as FORTRAN and APL) are not suitable for this purpose.

Fortunately one of the best teaching languages, PILOT, is well suited for microcomputers. The original form of PILOT is too limited for production of top quality teaching materials. Several extended forms of PILOT have been developed, and the National Library of Medicine is supporting an effort to achieve a national standard for the extended language. At Western Washington University we have implemented what promises to be essentially this standard on a SwTPC 6800, and we are currently working on 8080, Z-80 and Pascal implementations. By doing so we have shown that it is possible to implement a language that includes all the operations necessary for teaching, including the full range of numeric and string operators, full floating point, and numeric and string arrays, all in a 20 K byte microcomputer. Moreover, the response time is excellent. We maintain that there is no reason to settle for less in an instructional language.

Now that you're convinced that you'll have to get better systems software, what about hardware? It appears that any of the standard microcomputers will be suitable for this application if they can accept sufficient memory (16 K to 20 K bytes). The length of instructional programs and the distance and complexity of branching within the program requires the use of floppy disks or other forms of mass storage.

A typical instructional dialogue program occupies about 8 K bytes for every 5 minutes of instruction. Any individual student might leapfrog an entire section in a few seconds if the program were written to move with a well-prepared student. Thus the system must be interpretative, with the programs stored on disks.

Good terminals for teaching should have good graphics capabilities. At this time such terminals are too expensive ($4000 to $6700), several times the cost of the rest of the system. What is needed is a video terminal with at least a 256 by 256 dot matrix that can be superimposed on a 24 line by 80 character display (upper and lower case). Until such a unit is available, we must make do with less. However, a 40 character line is rather short for this purpose.

Finally, after all these cautions and discouragements, what can or should the owner of a microcomputer who wants to use the thing to teach do? One possibility is to search for or create games which provide practice in topics which your children have already learned in school. An obvious example is a version of Spacewar that demands fractional inputs as an exercise in fractions. A second possibility is the purchase of suitable systems software and course material. Such material is beginning to come onto the market. The third and most exciting possibility is to become involved in creating teaching material. Get suitable systems software and find an interested teacher. The teacher provides the material and the approach, and you provide the programming. If you take this route, remember that the teacher knows how to teach, that students are more varied than your imagination, and that good materials require testing and editing and retesting and reediting.
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BYTE December 1978 127
Digital integrated circuits that multiply binary numbers without the use of clock pulses have been available for several years. One such 4 bit by 4 bit multiplier is illustrated in figure 1. The 8 bit product appears on the output lines about 40 ns (the propagation delay) after the input lines are set. Larger numbers may be multiplied by first sectioning the inputs into 4 bit words, forming the products of each word of one input with every word of the other input, and summing these products in the appropriate manner. The propagation delay increases approximately linearly with the number of input bits. The number of integrated circuits required increases roughly as the number of bits in the multiplier times the number of bits in the multiplicand.

Multipliers are readily constructed from simpler integrated circuits. A 4 by 4 multiplier is illustrated in figure 2. The four bits of the multiplicand are gated into the adder M places from the right if the Mth bit of the multiplier is 1. If this bit is 0, only 0 is added in. The parts count is minimized by bringing the carry output of the last adder back to a previous adder input. This system costs less than the circuit in figure 1. Its disadvantages are a higher components count and a 60 percent increase in power requirements. The two systems have comparable propagation delays.

**Clockless Multiplication**

**and Division Circuits**

*Figure 1: Commercially available 4 by 4 multiplier.*
Figure 2: Inexpensive 4 by 4 multiplier that has a higher number of integrated circuits and uses more power than the circuit in figure 1.
The circuit in figure 3 shows one of many possible variations along these lines. This 4 by 5 multiplier uses inverters and NOR gates on the inputs instead of the AND gates of figure 2. Desirable input buffering is thus provided at about the same dollar cost, but requires more packages and power.

Clockless division circuits are more complicated than multiplication circuits. One way to obtain a 4 bit quotient from a 7 bit dividend and a left-adjusted 4 bit divisor is shown in figure 4. A subtraction is performed at each stage by complementing the divisor and adding, while forcing a carry input to the adder. If the difference is negative, as indicated by a 0 carry output, a 4 bit 1 out of 2 multiplexer is set to transmit the minuend to the next stage. If the difference

Figure 3: 4 by 5 multiplier with buffered inputs.
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Figure 4: Simple but slow clockless division circuit.
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A hypothetical assembly language called MIX was developed by the author to illustrate programming examples throughout the series. MIX is easily convertible to other assembly languages.

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is positive, the multiplexer transmits this difference. The quotient bits are the same as the bits that set the multiplexers. This method is straightforward and provides a remainder, but has the disadvantage of being relatively slow.

A more elegant clockless divider makes use of the relation $1/(1-r) \approx 1+r$ provided the absolute value of $r$ is much less than 1. The error in this estimate is $r^2$, as can be seen by multiplying each side of the approximate equality by $(1-r)$. Suppose an 8 bit dividend ($A = a_7a_6a_5a_4a_3a_2a_1a_0$) is to be divided by an 8 bit left-adjusted divisor ($D = d_7d_6d_5d_4d_3d_2d_1d_0$) to yield an 8 bit integer quotient $Q$. Let:

$$r = (2^3-d_2d_1d_0)/(2^3(d_7d_6d_5d_4d_3+1)).$$

This means that:

$$D = (d_7d_6d_5d_4d_3+1)(2^3)(1-r)$$

$$Q = 27(A)/[(d_7d_6d_5d_4d_3+1)(2^3)(1-r)],$$

$$Q \approx 2^4(A)(1-r)/(d_7d_6d_5d_4d_3+1).$$

Since $d_7$ equals 1, $r$ is less than $2^3/(2^3 \times 2^4)$ or $2^{-4}$, and $r^2$ is less than $2^{-8}$. $Q$ in this approximation is accurate to at least eight bits. Let:

$$I = 2^{12}/(d_7d_6d_5d_4d_3+1)$$

and

$$J = 2^{12}/(d_7d_6d_5d_4d_3+1)^2$$

each rounded to the nearest integer. Then $Q$ is approximately equal to $2^{-8}(A)[1+(2^3-d_2d_1d_0)(2^3)(J)]$ and the division problem has been reduced to addition and multiplication once $I$, $J$ and $(2^3-d_2d_1d_0)$ have been determined.

This last quantity is easily derived from four simple gates, as illustrated in the complete divider of figure 5. The quantities $I$ and $J$ are listed in table 1 for all possible values of $d_7d_6d_5d_4d_3$. These are found to 9 bit and 5 bit accuracy, respectively, to insure 8 bit accuracy in $Q$ after the intermediate

---

**Table 1: List of I and J values for 8 bit divider circuit of figure 5.**

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**Table 2: Power connections for integrated circuits used in figures 7 thru 5.**

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Figure 5: Faster 8 bit clockless divider. The 4 by 5 multiplier is the circuit of figure 3. The I and J values are obtained from a set of gates or a lookup table. The results being looked for are the values given in table 1. The 8 by 8 multiplier is the only device not previously discussed. The multiplier is composed of bit slices; the theory behind the multiplication circuits can be found in the TTL Data Book for Design Engineers, published by Texas Instruments Inc. The device number is SN54LS275, found on page 7-391 of the 1976 edition.
steps. I and J may be determined for a given divisor by a lookup process or by a suitable arrangement of gates. Of course, the entire division may be performed by looking up the inverse of the 8 bit divisor and then multiplying, but the method described here uses one eighth the memory space and only slightly more circuitry.

This process uses the inverse of a small number to find the inverse of a larger number, and so suggests a procedure for handling the division of numbers of arbitrary size. Such multiple-precision calculations could be performed by expanding the kind of hardware described here, or by an iterative software routine. Remainders are not directly available from this circuit, and must be obtained by subtracting the product of the quotient and divisor from the dividend.

The requirement that the divisor be left-adjusted is something of a nuisance; dividers generally need a restriction of this sort to keep the calculation in range of the hardware capability. Methods exist to make this adjustment and the subsequent adjustment required in the quotient without the use of clock pulses. These cumbersome circuits will not be described here.

Is any of this useful to the small systems owner? Most microprocessors do not have multiplication or division instructions. Products and quotients are obtained through time-consuming subroutines. Computer generated music or animated video displays may not permit sufficient computation time. Such real time outputs would be feasible if the fast circuits described here were incorporated into an external arithmetic unit and accessed through the input/output (IO) ports of the microcomputer. Then a division would be performed by the following:

- Output the divisor to the external arithmetic unit divider.
- Output the dividend to the external arithmetic unit divider.
- Input the quotient from the external arithmetic unit divider.
- Input the remainder (if desired) from the arithmetic unit divider.

Holding registers are required for the divisor and dividend. If 8 bit arithmetic is used, the entire calculation can be performed easily in the time taken by the input and output instructions.

**Editor's Note:**

*These circuits are theoretical. They have been designed but not implemented by the author.*

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**Z80 Programming for Logic Design** by Adam Osborne, Jerry Kane, Russell Rector, and Susanna Jacobson. Here's the book we've all been waiting for! This is the first in the Z80 family of books, which are programming for logic design books (the 8080 and 6800 books). Written for both programmers and logic designers, it explains how an assembly language program can replace non-programmable logic devices—with direct reference to the Z80 microcomputer. 352 pp. $8.50.

**8080A/8085 Assembly Language Programming** by Lance A. Leventhal. This book provides an introduction to assembly language programming for the 8080A and the 8085 processors. Included are sections on the instruction sets for the two processors, assemblers, simple program examples, code conversion, tables and lists, subroutines, IO, interrupts, program design, and debugging. Many examples and illustrations are included to cover critical points. 467 pp. $8.50.

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**SARGON** by D. and K. Spracklen. A complete computer chess program that won the 1978 West Coast Computer Faire Chess Tournament. Highly praised in the 9/78 issue of *Personal Computing*. Available early November. 120 pp. $14.95. (No photo)

**Microcomputer Primer** by Mitchell Waite and Michael Pardee. Here's a microprocessor tutorial for readers having some electronics background. *Microcomputer Primer* concentrates on the hardware of microcomputers (although there are sections dealing with software) with chapters on basic computer concepts, hardware, programming, memories, and number systems. A full complement of photos and schematics accompanies the text. 224 pp. $7.95.

**Programming a Microcomputer: 6502**. This informal, well-written book may just be what you need to enter the world of microcomputers. Caxton C. Foster uses the 6502 as a basis for discussing the techniques of writing programs. The chapters include simple, practical example programs for creating a Morse Code oscillator, combination lock, tune player, digital clock, and more. The emphasis is on clarity, and the many illustrations and flowcharts help get the author's points across. 231 pp. $9.95.

**Programmable Calculators** by Charles J. Sippl and Roger J. Sippl. This large (526 pages) book is an exhaustive survey of the programmable calculator field covering its history and present status. Chapters deal with the basic calculator, advanced hand-held products, RPN (Reverse Polish Notation) versus algebraic notation, desktop calculators, and programming the programmable calculator. Examples and illustrations abound in this useful reference work. $14.95.

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*BYTE* December 1978 139
Creating a Chess Player Part 3:

Chess 0.5 (continued)

Listing 1: The second half of Chess 0.5, written in Pascal. This portion of the program covers evaluation of terminal nodes, the look-ahead procedure and user commands (listing 1 continued on page 146).

This month we conclude the listing and commentary of Chess 0.5 begun last issue. The program was written by Larry Atkin, who is coauthor with David Slate of the world championship chess program, Chess 4.6. The program is readily adaptable to personal computers having Pascal systems such as the UCSD Pascal project software. Part 4 concludes the series with a discussion of chess strategy and tactics.

Evaluating Terminal Positions

Another important aspect of any chess program is the function which provides a static evaluation of terminal positions in the look-ahead tree. In the present program, this routine also doubles as a preliminary scoring function for sorting moves at the first ply, at the beginning of the look-ahead search. Since the evaluation function is used repetitively in the search, efficiency demands that it be carefully engineered. We have left this task as an exercise for the reader. Our function presently includes only a few basic essentials.

The most important feature is material. We employ essentially the same function for this that is used by Chess 4.5. A trade-down bonus is also incorporated, ie: trade pieces but not pawns when ahead in material. A second feature which is considered is piece mobility. The mobility of Knights and Bishops is weighted more heavily than that for Rooks and Queens. Special credit is given to a King which is located in one of the four corner squares in each corner of the board, ie: 16 squares total. This encourages early castling. Pawn structure is considered by providing a bonus for advancing the pawns in the four center files, for having a pawn near the King, and for having a pawn adjacent to or defended by another pawn. This indirectly penalizes isolated or backward pawns. There is a direct penalty...
if the square in front of a pawn is occupied. The position of the Rooks is considered by providing a bonus for placing a Rook on the seventh rank and for attacking another Rook of the same color (i.e., doubled Rooks). The executive routine for these assessments is EVALU8.

The Look-Ahead Procedure

The look-ahead procedure is controlled by an executive routine called SEARCH. Several subprocedures are also defined which handle specific tasks. NEWBST keeps track of the move which is currently thought to be best, and dynamically reorders the moves at the first ply level each time a new best-move is selected. MINMAX determines whether the move under consideration will produce an α-β cutoff. SCOREM is called into action when the program can find no legal moves at a node. It determines whether the position should be scored as a checkmate or as a stalemate. SELECT is responsible for move ordering at each node. It determines whether there are any more moves to be searched and if so, makes sure that they are generated in the correct order (i.e., captures, killers, castling moves, and then the remaining moves).

SEARCH incorporates a number of important features which make the look-ahead search more efficient. These include staged move generation, preliminary ordering scores, setting a narrow α-β window at the beginning of the search, conducting the search in an iterative fashion, and dynamically recording moves at the first ply as the search proceeds. Because of these features, the full-width search takes a long time instead of taking forever.

User Commands

For the user's convenience, the program should be able to respond to a few simple commands. Inputs to the program are processed by a lengthy routine, READER, which has many component subroutines. The translation of the input string is handled by a group of routines: RDRERR, RDRGNST, RDRSFT, RDRCMP, RDLINE, RDRMOV and RDRNUM. Each of the commands is executed by a separate routine.

When the human player wishes to terminate the game before it has reached its conclusion (e.g., when he is hopelessly lost and does not want to stay around to be crushed), he can simply type an END command and the ENDCMD routine will terminate the program. If the user simply wishes to start a new game, he can type INIT and the INICMD routine will set up for a new game.
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(eg: side to move, move number, en passant, castling), this can be done by activating STACMD.

Notes on Notation

The program also processes standard chess notation. This is not strictly necessary. Many programs use their own convention for entering and reporting moves. A common procedure is to denote the squares using a number (1 through 8) for each row and a letter (A through H) for each column. A move is defined by listing the present square of the piece and then the destination square. For example, the common opening move, P-K4, would be E2E4. Moving the White Knight on the kingside from its original square to KB3 would be G1 F3. This convention works nicely but it forces an experienced chess player to learn a new system. Most would prefer standard chess notation.

Because there are multiple ways to express the same move in standard notation, the translation routine needs to be fairly sophisticated. Consider a position in which the White Queen’s Rook is on its original square and the neighboring Knight and Bishop have been moved. A move which places the Rook on the Queen Bishop file can be designated as R-B1, R-QB1, R/1-B1, R/1-QB1, R/R1-B1, or R/R1-QB1. It is important that the program recognize that each of these character strings represents the same move. How is this done?

One way is to have the machine generate a list of all legal moves and then compare each of these with the move entered by the player. If his move matches one on the list, that move is noted. The rest of the list is then checked and if no more matches are found, the noted move is assumed to be the correct one. If no match is found, the machine prints “illegal move.” If a second match is found (eg: P-B3 matches both P-KB3 and P-QB3), the machine prints “ambiguous move.” The process of translating the opponent’s move into machine compatible form and checking its legality or ambiguity is done by YRMOVE. The process of translating the machine’s move into standard notation is handled by MYMOVE. Both of these procedures call MINENG, which is responsible for constructing the appropriate character strings.

Final Thoughts

This completes our listing of our demonstration chess program. Despite the program’s length, there are many desirable features which have been omitted. The reader with an interest in chess and programming should use this listing as a starting point for developing a program. The time required for move calculation can be reduced by writing machine dependent code for some of the frequently used routines. There are also features which can be added to improve the level of play.

One useful addition would be an opening library. An effective technique for this is described by Slate and Atkin in their chapter in Chess Skill in Man and Machine (P W Frey, editor, Springer-Verlag, New York, 1977). An opening library provides the user with a challenging set of opening moves and directs the game into situations which are familiar to the experienced chess player. By including various options at the early choice points and using a random selection procedure, the programmer can insure that the machine will not always select the same move sequence. The programmer can also give the user the option of specifying a particular opening against which he would like to practice. For important matches, the programmer can prepare surprise openings for the machine in order to gain a psychological edge on the opponent.

Text continued on page 157
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Listing 1, continued from page 140:

```

FUNCTION EVROOK (* EVALUATE ROOK *)
VALUE = (+ ROOK LOCATIONS +)
BEGIN
  INTV = TVI (* SCRATCH *)
  INTH = THI (* SCRATCH *)
  INTS = TS (* SEVENTH RANK *)
BEGIN
  INTV = INTV + 1 (* INITIALIZE *)
  THMS = THM (* AT FIRST PLY *)
  IF NOT TVS(THM,INTV) THEN
    BEGIN
      ANDS(INTH,THMS,THMSTV(THM,INTV));
      If NOT NULRS(INTH) THEN
        BEGIN
          INTV = INTV + 1 (* GIVE DOUBLE ROOE CREDIT *)
          THMS = THMS + 1;
        END;
      END;
    END;
  END;
  EVROOK = INTV + INTH*INTV**INTV; (* CREDIT ROOKS ON SEVENTH *)
END (* EVROOK *)

BEGIN
  IF TVS(JNTK-1) = HBV1(JNTK) AND XPS = BSTVL(JNTK-2) THEN
    (* MOVE WILL PRUNE ANYWAY *)
    INTV = XTHV(JNTK-1) = HBV1(JNTK);
  ELSE
    BEGIN
      INTV = (FLOOP(THMSTV(TV)),21,22),ELOOP(TV),SH,VR);
      IF THMSTV(TV) THEN
        BEGIN
          INTV = INTH - TVI (* LOCATE FIRST ROOK *)
          THMS = INTV;
        END;
      END;
      BEGIN
        ANDS(INTH,THMS,THMSTV(INTH,THMS));
        If NOT NULRS(INTH) THEN
          BEGIN
            INTV = INTV + 1 (* GIVE DOUBLE ROOE CREDIT *)
            THMS = THMS + 1;
          END;
        END;
        EVROOK = INTV + INTH*INTV**INTV; (* CREDIT ROOKS ON SEVENTH *)
      END (* EVROOK *)
    END;
  END;
  IF TVS THEN
    BEGIN
      WRITE("VALUE",JNTK,JNTK,INDEX(JNTK),INTV);
      PRINTMOV(MOVES(INDEX(JNTK)-1));
    END;
  END;
  (* RETURN SCORE *)
END (* FUNCTION SELECT *)

FUNCTION SEARCH (* SEARCH LOOK-AHEAD TREE *)
BEGIN
  INTV = TVI (* RETURNS THE BEST MOVE *)
  LABEL 11, 12, 13, 14, 15, 16; (* TRY DIFFERENT FIRST MOVE *)
  IF INTV THEN
    BEGIN
      MOVES = 0; (* FLOAT VALUE BACK UP *)
      IF INTV THEN
        BEGIN
          IF MOVES THEN
            (* FIND ANOTHER MOVE *)
            MOVES = 1; (* BACK UP A PLY *)
          END;
        END;
      END;
      IF INTV THEN
        BEGIN
          EXIT SEARCH (* GET MOVES *)
        END;
      END;
    END;
  END;
  (* RETURN MOVE INFORMATION *)
  (* PLY OF BEST MOVE *)
END (* FUNCTION SELECT *)

BEGIN
  INTV = TVI (* MOVES INDEX *)
  THMS = THM (* SCRATCH *)
BEGIN
  BSTVLA = INDEX(A+1); (* SAVE BEST MOVE *)
  IF A = AK THEN (* AT FIRST PLY *)
    BEGIN
      BRM = MOVES(BSTVLA); (* SAVE BEST MOVE *)
      FOR INTV = BSTMVLA = MOVES(BSTVLA) DO
        BEGIN
          MOVES(INTH) = MOVES(INTH) + 1 (* MOVE OTHER MOVES DOWN *)
          MOVES(INTH) = MOVES(INTH) + 1 (* PUT BEST AT BEGINNING *)
          BSTVLA = BSTVLA + 1 (* POINTS TO BEST MOVE *)
        END;
      END;
    END;
  ELSE
    BEGIN
      If NOT MOVES(BSTVLA) = NHC THEN
        BEGIN
          KILLJNTK = MOVES(BSTVLA); (* SAVE KILLER MOVE *)
        END;
      END;
    END;
  END (* BEST MOVE *)
END (* FUNCTION SEARCH *)

BEGIN
  MOVES(INDEX(JNTK)-1) = TRUE (* INDEED MOVE*)
  IF MOVES(INDEX(JNTK)-1) THEN (* CLEAR MOVES SEARCHED *)
    BEGIN
      BSTVL(JNTK-2) = BSTVL(JNTK-2) (* SAVE ALPHAB *)
      INTV = INTV + 1 (* INHIBIT PRUNING IN EVALUATE *)
      MOVES = 0 (* INITIALIZE MAXIMUM POSITIONAL SCORE *)
      GEMALL = 0 (* GENERATE ALL MOVES *)
      FOR INTV = A1 TO JNTK-1 DO
        BEGIN
          IF UPDATE(MOVES(INTH)) THEN (* CLEAR MOVES SEARCHED *)
            BEGIN
              INDEX(JNTK) = INTH (* POINT TO CURRENT MOVE *)
            END;
          EVALUATE (* SCORE POSITION *)
        END;
      END;
      GONODATE(MOVES(INTH));
      END;
    END;
  END (* SELECT EXIT - DOW *)
  IF INTV THEN
    BEGIN
      MOVES(INTH) = A1 (* SELECT EXIT *)
      SPRINTMOV(MOVES(A1));
      IF NOT MOVES(INTH) THEN
        BEGIN
          SELECT MOVES(INTH); (* SELECT EXIT *)
        END;
    END;
  END (* SELECT EXIT *)
END (* SELECT EXIT *)

BEGIN
  MOVES(ININDEX(JNTK)-1) = TRUE (* INDEED MOVE *)
  If MOVES(ININDEX(JNTK)-1) THEN (* CLEAR MOVES SEARCHED *)
  BEGIN
    SOLVE(JNTK),INDEX(JNTK),INDEX(JNTK),INDEX(JNTK); (* INITIALIZE *)
  ELSE
    VALUE(INDEX(JNTK)) = 0 (* STALEMATE *)
  BEGIN
    VALUE(INDEX(JNTK)) = 1 (* IF SMT THEN *)
    WRITE("SCORE",JNTK,JNTK,INDEX(JNTK),INDEX(JNTK),VALUE(INDEX(JNTK)));
    END (* IF SMT THEN *)
  END (* BEGIN *)
END (* FUNCTION SELECT *)

BEGIN
  MOVES(ININDEX(JNTK)-1) = 1 (* CLEAR MOVES SEARCHED *)
  If MOVES(ININDEX(JNTK)-1) THEN (* CLEAR MOVES SEARCHED *)
  BEGIN
    BSTVL(JNTK-2) = BSTVL(JNTK-2) (* INHIBIT PRUNING IN EVALUATE *)
    MOVES = 0 (* INITIALIZE MAXIMUM POSITIONAL SCORE *)
    GEMALL = 0 (* GENERATE ALL MOVES *)
    FOR INTV = A1 TO JNTK-1 DO
      BEGIN
        If UPDATE(MOVES(INTH)) THEN (* CLEAR MOVES SEARCHED *)
          Begin
            INDEX(JNTK) = INTH (* POINT TO CURRENT MOVE *)
          END;
        EVALUATE (* SCORE POSITION *)
      END;
    END;
    GONODATE(MOVES(INTH));
    END (* SELECT EXIT *)
  END (* IF SMT THEN *)
  IF INTV THEN
    BEGIN
      MOVES(ININDEX(JNTK)-1) = 1 (* RESTORE ALPHA *)
      SORTMOV(MOVES(INTH-1)); (* SORT PRELIMINARY SCORES *)
      For INTV = A1 TO JTH DO
        BEGIN
          KILLJNTK = NULRY (* CLEAR KILLER TABLE *)
        END;
    END;
  END (* SELECT EXIT *)
END (* SELECT EXIT *)

BEGIN
  MOVES(ININDEX(JNTK)-1) = 0 (* INITIALIZE FOR NEW MOVES *)
  BEGIN
    MOVES(ININDEX(JNTK)-1) = A1 (* CLEAR MOVES SEARCHED *)
    BSTVL(JNTK-2) = BSTVL(JNTK-2) (* INHIBIT PRUNING IN EVALUATE *)
    MOVES = 0 (* INITIALIZE MAXIMUM POSITIONAL SCORE *)
    GEMALL = 0 (* GENERATE ALL MOVES *)
    For INTV = A1 TO JNTK-1 DO
      BEGIN
        If UPDATE(MOVES(INTH)) Then (* CLEAR MOVES SEARCHED *)
          BEGIN
            INDEX(JNTK) = INTH (* POINT TO CURRENT MOVE *)
            EVALUATE (* SCORE POSITION *)
          END;
      END;
    END;
    GONODATE(MOVES(INTH));
    END (* SELECT EXIT *)
  END (* SELECT EXIT *)
END (* SELECT EXIT *)

BEGIN
  MOVES(ININDEX(JNTK)-1) = 1 (* CLEAR MOVES SEARCHED *)
  If MOVES(ININDEX(JNTK)-1) THEN (* CLEAR MOVES SEARCHED *)
  BEGIN
    BSTVL(JNTK-2) = BSTVL(JNTK-2) (* INHIBIT PRUNING IN EVALUATE *)
    MOVES = 0 (* INITIALIZE MAXIMUM POSITIONAL SCORE *)
    GEMALL = 0 (* GENERATE ALL MOVES *)
    For INTV = A1 TO JNTK-1 DO
      Begin
        If UPDATE(MOVES(INTH)) Then (* CLEAR MOVES SEARCHED *)
          BEGIN
            INDEX(JNTK) = INTH (* POINT TO CURRENT MOVE *)
            EVALUATE (* SCORE POSITION *)
          END;
      END;
    END;
    GONODATE(MOVES(INTH));
    END (* SELECT EXIT *)
  END (* IF SMT THEN *)
  IF INTV THEN
    BEGIN
      MOVES(ININDEX(JNTK)-1) = A1 (* RESTORE ALPHA *)
      SORTMOV(MOVES(INTH-1)); (* SORT PRELIMINARY SCORES *)
      For INTV = A1 TO JTH DO
        BEGIN
          KILLJNTK = NULRY (* CLEAR KILLER TABLE *)
        END;
    END;
  END (* SELECT EXIT *)
END (* SELECT EXIT *)

BEGIN
  MOVES(ININDEX(JNTK)-1) = 0 (* INITIALIZE FOR NEW MOVES *)
  BEGIN
    MOVES(ININDEX(JNTK)-1) = A1 (* CLEAR MOVES SEARCHED *)
    BSTVL(JNTK-2) = BSTVL(JNTK-2) (* INHIBIT PRUNING IN EVALUATE *)
    MOVES = 0 (* INITIALIZE MAXIMUM POSITIONAL SCORE *)
    GEMALL = 0 (* GENERATE ALL MOVES *)
    For INTV = A1 TO JNTK-1 DO
      Begin
        If UPDATE(MOVES(INTH)) Then (* CLEAR MOVES SEARCHED *)
          BEGIN
            INDEX(JNTK) = INTH (* POINT TO CURRENT MOVE *)
            EVALUATE (* SCORE POSITION *)
          END;
      END;
    END;
    GONODATE(MOVES(INTH));
    END (* SELECT EXIT *)
  END (* SELECT EXIT *)
END (* SELECT EXIT *)
```

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Evaluation copy $500 in USA, 2 weeks delivery, payment by cheque, American Express or Visa.

Micro Focus offers a CIS COBOL licensing package to OEM's including access to internal documentation and program source plus an Interfacing Kit to enable CIS COBOL to be implemented quickly in the OEM's own hardware and software environment. The CIS COBOL compiler is itself written in COBOL making it self compiling and thereby extremely portable.

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* CP/M is a trademark of Digital Research and ISIS is a trademark of Intel Corporation.

Circle 216 on inquiry card.
Listing 1, continued:

IF SMTR OR SWPS THEN
  FOR INTW = AW:1 TO JNTW-1 DO
    BEGIN
      WRITE("PRELIM-INTW,VALUE(INTW)\nPREMOVING(VALINTW)\n(* PRINT PRELIMINARY SCORES \nIF INTW/2-1 = INTW DIV 2 THEN PAUSER\nELSE\n  SELWHT(WITY) \n  (* SEARCH ALL MOVES \nENDI

M11 (* INITIALIZE AT NEW DEPTH *)
BEGIN
  VSSELJNXT1 = $1
  IF JNTK = $JNT THEN
    BEGIN
      EVALUATE \n        (* EVALUATE CURRENT POSITION *)
      INDEX(JNTK+1) = $AN\n      BSTVL(JNTK+1) = VALUE(INDEX(JNTK+1))
      IF REMNAX(JNTK+1) OR JNTK = $JKT THEN
        SELDOM; \n        (* THIS MOVE PRUNES *)
      SCHR(JNXT) = $2; \n        (* capture search *)
    ENDI
ELSE
  SCHR(JNXT) = $3; \n    (* captures in full search *)
  GENCAP; \n    (* GENERATE CAPTURES *)
  SELWHT((SCHR(JNXT)\n    (* change search mode *)
ENDI

M21 (* capture search *)
BEGIN
  INTW = $AW\n    (* best move pointer *)
  INTV = $AV\n    (* best value *)
  FOR INTV = LINDX(JNXT) TO JNTW-1 DO
    WITH MOVEVINTW DO
      IF NOT DSMW THEN
        IF ABS(STPNV(RCPM)) = INTW THEN
          INTV = ABS(STPNV(RCPM)); \n            (* set new move *)
        INTW = INTV; \n      (* best move to INTV *)
      IF INTW = AW THEN \n        (* MOVE FOUND *)
        SELMOV(INTW) \n       (* SELECT BIGGEST CAPTURE *)
      ELSE \n        SELDOM; \n          (* quit *)
ENDI

M31 (* full width search - captures *)
BEGIN
  INTW = $AW\n    (* best move pointer *)
  INTV = $AV\n    (* best value *)
  FOR INTV = LINDX(JNXT) TO JNTW-1 DO
    WITH MOVEVINTW DO
      IF NOT DSMW THEN
        IF ABS(STPNV(RCPM)) = INTV THEN
          INTW = INTV; \n            (* best move to INTW *)
      INTV = INTW; \n          (* best move to INTV *)
      IF INTW = AW THEN \n        (* MOVE FOUND *)
        SELMOV(INTW) \n       (* SELECT BIGGEST CAPTURE *)
      ELSE \n        IF NOT NULMV(KILLR(JNXT)) THEN
          BEGIN
            INTW = JNXT; \n              (* save current moves index *)
            GENFLKS(KILLR(JNXT),RMP1) \n              (* generate move by killer *)
            SCHR(JNXT) = $W1; \n                (* set next search mode *)
            FOR JNTW = INTW TO JNTW+1 DO
              IF KILLR(JNXT),RMP1 = MOVEVCONT(JNXT) THEN \n                (* look at moves by killer *)
              SELMOV(RWT); \n                  (* select killer move *)
            ENDI
          ENDI
        SELWHT(MHT) \n          (* go to next state *)
      ENDI

H11 (* initialize scan of castle moves and other moves by killer piece *)
BEGIN
  GENCAI; \n    (* generate castle moves *)
  SELWXHTH1; \n      (* go to next state *)
ENDI

H51 (* full width search - castles and other moves by killer piece *)
BEGIN
  SELWHTH1; \n    (* select any move *)
  GENFLKSLALOC(JNXT),RMP1 \n    (* generate remaining moves *)
  SELWXHTH1; \n    (* next search mode *)
ENDI

H61 (* full width search - remaining moves *)
BEGIN
  SELWHTH1; \n    (* select anything on list *)
  IF HSVELJNXT1 = 0 THEN \n    (* score mate *)
  SELDOM; \n      (* exit select *)
ENDI

H71 (* research first ply *)
BEGIN
  JNXT = LINDX(AW+1) \n  (* point to already generated moves *)
  HSVELJNXT1 = 0; \n  (* reset moves searched *)
  FOR INTW = AW+1 TO JNTW+1 DO
    MOVEVINTW,RSW = FALSE; \n      (* clear searched bit *)
  IF SMTR THEN \n    (* write "-", INTK, BSTVL=2-1, BSTVL=1-1*)
    SELWHTH1 \n      (* search all moves *)
ENDI

221 (* select exit *)
SELECT = INTBI \nENDI (* select *)

BEGIN (* search *)
BSTVL(NXK) = AW \n  (* initialize move *)
INDEX(JNXT1) = $AN \n  (* initialize tree *)
ENDI (* initialize move *)
ENMI (* initial guess at score *)
BSTVL=2-1 = VALUE(JNXT) \n  (* initialize alpha-beta window *)
JNKT = $KST \n  (* initialize iteration number *)
WHILE (MOVES < NODEL) AND (JNKT < MAXIZE DIV 2, ZE-BI) DO\nBEGIN

111 (* start new ply *)
BSTVL=1-1 = VALUE(JNKT) \n  (* initialize alpha-beta *)

121 (* different first move *)
BEGIN
  IF BSTVL(JNXT) = VALUE(INDEX(JNKT+1)) \n    (*) newbst(JNKT1) *)
  ENDI (* find another move *)
ELSE
  BEGIN
    IF UPDATE(MOVEVINDEX(JNKT+1)) THEN \n      GOTO 111 \n      (* start new ply *)
    ELSE
      GOTO 121 \n      (* find another move *)
  ENDI

131 (* float value back *)
IF REMNAX(JNKT) THEN \n  GOTO 151 \n  (* prune *)
ELSE
  BEGIN
    IF UPDATE(MOVEVINDEX(JNKT+1)) THEN \n      GOTO 111 \n      (* start new ply *)
    ELSE
      GOTO 141 \n      (* find another move *)
  ENDI
ENDI (* end *)

151 (* back up a ply *)
IF JNKT = $KST THEN \n  BEGIN (* not done with iteration *)
    DNMATE(MOVEVINDEX(JNKT+1)) \n    (* retract move *)
  ENDI (* end *)

161 (* done with iteration *)
IF BSTVL(AW) = BSTVL(AW-2) OR BSTVL(AW) = BSTVL(AW-1) THEN \n  BEGIN (* no move found *)
    IF HSVELJNXT1 = 0 THEN \n      BSTVL(AW) = 0 \n      BEGIN (* no legal moves *)
        GOTO 161 \n        (* give up *)
      ENDI (* end *)
    BSTVL(AW-2) = -ZFI \n      (* set alpha-beta window large *)
    BSTVL(AW-1) = -ZFI \n      (* set alpha-beta window *)
    SCHRJNXT1 = $HST \n      (* try again *)
  ENDI (* end *)
ENDI (* end *)

171 (* exit search *)
SEARCH = BSTVL(AW) \n  (* return best move *)
ENDI (* search *)

PROCEDURE READER;
  (* read input from user *)
LABEL 111 \n  (* command finished exit *)
VAR \n  IMRA = RA; \n    (* scratch token *)
  INTJ = TJ; \n    (* echo command index *)
PROCEDURE RODERR(ARMH) \n  (* print diagnostic and exit *)
VAR \n  INTJ = TJ; \n    (* string index *)
  INTN = TN; \n    (* message index *)
BEGIN
  IF NOT SHED THEN \n    (* echo line if not already done *)
    BEGIN
      WRITE ""; \n        (* write intj to zj-1 do *)
      WRITE(INI;(*write(intj!))
        (* write input line *)
      ENDI (* end *)
    ENDI (* end *)
    (* leading blakens before arrow *)
    ENDI (* end *)
    (* pointer to error *)
    ENDI (* command error *)
  ENDI (* end *)
NEW!

9600 BAUD CASSETTE RECORDER

An ASYNCHRONOUS NRZ type Recorder with remote motor start/stop. Error rate 10⁻⁸ at 4800 BAUD. Can be used from 110 to 9600 BAUD into a UART — no clocking required. This is not an audio recorder. It takes RS232 or TTL signals from the terminal or computer and gives back the same signals. No audio interface is used. Motor start/stop is manual or through TTL or RS232 signals.

Tape speeds are 1.6" / 3.0" and 6.0" per second. 110 volt, 60 Hz, 5 watts. (220 Volts on special order). Can use high quality audio cassettes (Philips Type) or certified data cassettes. Recommended for DATA LOGGING, WORD PROCESSING, COMPUTER PROGRAM RELOADING and DATA STORAGE. Manual control except for motor start/stop. 6800, 8080 or Z80 software for file or record searching available on request with order. Used by major computer manufacturers, Bell Telephone and U.S. Government for program reloading and field servicing.

AVAILABILITY — Off the shelf.

MODEL CC-9
$200.00 (4800 Baud)
$220.00 (9600 Baud and 220V/50 Hz)

PROVIDES MONITOR AND TAPE SOFTWARE in ROM. TERMINAL and TAPE PORTS on SAME BOARD. CONTROLS ONE or TWO TAPE UNITS (CC-8 or 3M3B).

This is a complete 8080, 8085, or Z80 system controller. It provides the terminal I/O (RS232, 20 mA or TTL) and the data cartridge I/O, plus the motor controlling parallel I/O latches. Two kilobytes of on board ROM provide turn on and go control of your Altair or IMSAI. NO MORE BOOTSTRAPPING. Loads and Dumps memory in hex on the terminal, formats tape cartridge files, has word processing and paper tape routines. Best of all, it has the search routines to locate files and records by means of six, five, and four letter strings. Just type in the file name and the recorder and software do the rest. Can be used in the BISync (IBM), BiPhase (Phase encoded) or NRZ modes with suitable recorders, interfaces and software.

This is Revision 8 of this controller. This version features 2708 type EPROM's so that you can write your own software or relocate it as desired. One 2708 preprogrammed is supplied with the board. A socket is available for the second ROM allowing up to a full 2K of monitor programs.

Fits all $100 bus computers using 8080 or Z80 MPU's. Requires 2 MHz clock from bus. Cannot be used with audio cassettes without an interface. Cassette or cartridge inputs are TTL or RS232 level.

AVAILABILITY — Off the shelf.

DOUBLE DENSITY FLOPPY DISK CONTROLLER

A new floppy controller for 5" and 8" drives utilizing the new 1791 chip to provide single or double density recording. Flip the switch to use one or the other mode. Can load memory from single density and re-record it double density on the same drive so you can transfer or re-record your programs and files. Comes with new format program for double density on disk to replace your old single density format program. (Soft Sector IBM format). $295. Assembled and tested.

SHIPPING STARTED OCTOBER '78.

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$190.00, Tested & Assmb.

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The LATEST in Tape Systems

2SIO (R) CONTROLLER
$190.00, Tested & Assmb.
Listing 1, continued:

FUNCTION RDSGTN(VAR $IRA) : # GET NEXT TOKEN FROM COMMAND
RETURNS TOKEN IN A.
RETURNS TRUE IF NON-EMPTY
TOKEN.
A TOKEN IS ANY CONSECUTIVE
COLLECTION OF ALPHANUMERIC
CHARACTERS, LEADING SPECIAL CHARACTERS
IGNORED. *)

VAR
INTJ : TJI
(* STRING INDEX *)
BEGIN
WHILE (INTJ < 2) AND ( Ord (IN LNE [INTJ]) < Ord ("=")) DO
A := ""
INTJ := INTJ + 1
END;
RDSGTN := INTJ := AA:
(* RETURN TRUE IF ANYTHING
MOVED *)
WHILE (INTJ < 2) AND (IN LNE [INTJ] = "=" OR INTJ = 1) DO
(* SKIP REST OF TOKEN *)
END; (* RDSGTN *)

PROCEDURE RDSFTI (* SKIP FIRST TOKEN IN COMMAND
LINE *)
VAR
INRA := RAI:
INTB := TBI:
(* SCRATCH *)
BEGIN
INTJ := AJI
INTB := RDSGTN(INRA):
(* THROW AWAY FIRST TOKEN *)
END; (* RDSFTI *)

PROCEDURE RDSRCHO (* TEST FOR AND EXECUTE COMMAND
EXITS TO COMMAND EXIT IF
COMMAND IS PROCESSED. *)

FUNCTION RMPHTBI (* EXTRACT NEXT COMMAND
FROM INPUT LINE,
RETURNS TRUE IF NON-EMPTY
COMMAND. *)
VAR
INTC := TC:
INTJ := TJI:
(* SCRATCH *)
(* STRING INDEX *)
BEGIN
READLN;
INTJ := AJI
WHILE NOT (EOLN AND (INTJ < 2)) DO  (* COPY INPUT LINE *)
BEGIN
READCARD(INJ):
INTJ := INTJ + 1
END;
WHILE NOT (EOLN) DO
(* SKIP REST OF INPUT LINE *)
BEGIN
READCARD(INJ):
INTJ := INTJ + 1
END;
(* BLANK REST OF LINE *)
END;
READCARD(INJ):
INTJ := INTJ + 1
(* SET END OF COMMAND *)
JN T J := AJI
(* RESET INPUT LINE POINTER *)
END; (* RMPHTBI *)

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YOUR COMPUTALKER!

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Circle 53 on inquiry card.
Listing 1, continued:

PROCEDURE BOARDV(AJT1): (* ADVANCE N FILES *)
BEGIN
  IF INTS + 6 < 25 THEN
    INTS := INTS + 6
  ELSE
    INTS := 25;
  END (* BOARV *)

PROCEDURE BOASTOC (AJP1): (* STORE PIECE ON BOARD *)
BEGIN
  BOARD.RBSI[INTS] := AI;
  IF INTS <= 25 THEN
    INTS := INTS + 1;
  END (* BOASTOC *)

BEGIN (* BOACH *)
CLST1 := (* CLEAR STATUS FLAGS *)
LSTMV := NULMV; (* CLEAR PREVIOUS MOVE *)
FOR INTS := 26 TO 29 DO
  BOARD.RBSI[INTS] := AT; (* CLEAR BOARD *)
  INTH := LITE;
  INTH := 81;
REPEAT
    CASE CLST1[JNT1] OF
      'P': BOASTOITUPMER(INTH);
      'B': BOASTOITUMER(INTH);
      'N': BOASTOITUMER(INTH);
      'K': BOASTOITUMER(INTH);
      'Q': BOASTOITUMER(INTH);
      'H': INTH := LITE;
      'G': INTH := DARE;
      'O': INTH := DARE;
      'D': BOASTOITUPMER(INTH);
      'L': BOASTOITUPMER(INTH);
      'G': BOASTOITUPMER(INTH);
      'O': BOASTOITUPMER(INTH);
      'D': BOASTOITUPMER(INTH);
      'L': BOARD[ORD(INTH)] := 0;
    END (* CASE *)
  ELSE
    IF CLST1[L] IN ('A', 'H') THEN
      BEGIN
        FOR INTS := 26 TO 29 DO
          BOARD.RBSI[INTS] := AT;
        CLST1 := (* CLEAR STATUS *)
        RORERR := "ILLEGAL BOARD OPTION " ||
        JNT1 := JNT1 + 1;
        UNTIL JNT1 = 29;
      END (* BEGIN *)
    END (* ELSE *)
  END (* IF-ELSE *)
END (* BEGIN *)

PROCEDURE ENDCMD(): (* COMMAND - END PROGRAM *)
BEGIN
  GOTO 91; (* END PROGRAM *)
END (* ENDCMD *)

PROCEDURE GOMCMD(): (* COMMAND - GO N MOVES *)
BEGIN
  GOING := RORNUM;
  IF GOING = 0 THEN
    BEGIN
      GOING := 1;
    END (* IF-THEN *)
END (* GOMCMD *)

PROCEDURE INITCMD(): (* COMMAND - INITIALIZE FOR A NEW GAME *)
BEGIN
  GOTO 11; (* INITIALIZE FOR A NEW GAME *)
END (* INITCMD *)

PROCEDURE LETCMD(): (* COMMAND - CHANGE VARIABLE *)
LABEL Z11:
  (* LET COMMAND EXIT *)
PROCEDURE LETONE(): (* COMMAND - SET ONE VARIABLE *)
A111 := 11111111;
VAR BIT111 := (*) VARIABLE *)
BEGIN
  IF A111 = L THEN
    BEGIN
      R := RORNUM;
    GOTO Z11;
    END (* IF-THEN *)
END (* BEGIN *)

PROCEDURE PAMCMD(): (* COMMAND - PRINT ATTACK MAP *)
BEGIN
  WHILE RORNUM > 0
  IF INRAAI = "T" THEN
    PRINT(KA1AIET());
  ELSE
    PRINT(KA1AIET());
    END (* IF-ELSE *)
  ELSE
    RORERR := "ATTACK MAP NOT 'TO' OR 'FROM'");
  END (* PAMCMD *)

PROCEDURE POPCMD(): (* COMMAND - PRINT OTHER STUFF *)
VAR
  SPORT := 11;
  CASTLE := 11;
BEGIN
  If BOARD[SPORT] THEN
    BEGIN
      PRINT("WHITE MUST ATTACK", TO MOVE.");
      END (* PRINT *)
END (* PPOCM *)

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Listing 1, continued:

PROCEDURE PHNCHWO
(* COMMAND - PRINT MOVE LIST *)
VAR
INT: * TH:
(* MOVES LIST INDEX *)
BEGIN
LISTMOV:
FOR INT := 1 TO INTW DO
BEGIN
WRITE(INTW, " ");
PRIMMOVMOV(INTHW, INTW);
IF INTW/2 + INTW DIV 2 THEN
PAUSE;
END;
END (* PHNCHWO *);

PROCEDURE SWCHWO
(* COMMAND - FLIP SWITCH *)
LABEL
Z11
(* SWITCH OPTION EXIT *)
PROCEDURE SWCHNE
(INHA:
(* PROCESS ONE SWITCH *)
VAR STY:
(* SWITCH NAME *)
BEGIN
INT := TJ:
(* SAVE COMMAND INDEX *)
BEGIN
IF INRA = A THEN
BEGIN
INT := JTJ:
IF RORGNT(INRAN) THEN
BEGIN
IF INRA = "ON " THEN
BEGIN
SWCHNE("EC", "OLVE");
SWCHNE("PA", "SWPA");
SWCHNE("PS", "SWPS");
SWCHNE("U", "SWU");
SWCHNE("FR", "SWIF");
END;
ELSE
BEGIN
EXIT STATUS OPTION (*);
END;
END;
ELSE
IF INRA = "OFF " THEN
BEGIN
SWCHNE("EC", "OLVE");
SWCHNE("PA", "SWPA");
SWCHNE("PS", "SWPS");
SWCHNE("U", "SWU");
SWCHNE("FR", "SWIF");
END;
BEGIN
SWCHNE("EC", "OLVE");
SWCHNE("PA", "SWPA");
SWCHNE("PS", "SWPS");
SWCHNE("U", "SWU");
SWCHNE("FR", "SWIF");
PROCEDURE STACWI
(* COMMAND - STATUS CHANGES *)
LABEL
Z11
(* STATUS COMMAND OPTION EXIT *)
VAR
INRA = RA;
(* CURRENT TOKEN *)
INTH = THI;
(* SIDE BEING PROCESSED *)
PROCEDURE STACPI
(INRA:
(* PROCESS EP FILE *)
BAYF:
(* TEST TOKEN *)
(* EQUIVALENT FILE *)
BEGIN
IF A = INRA THEN
BEGIN
IF INT = LITE THEN
BEGIN
BOARD.RBS = XTRFSRI,B1;
END
ELSE
BOARD.RBS = XTRFSRI,B1;
GOTO Z11;
(* EXIT STATUS OPTION *)
END;
END (* STACPI *);
PROCEDURE STACGO
(* ALLOW CASTLE KING SIDE *)
BEGIN
IF INT = LITE THEN
BOARD.RBS = BOARD.RBS + ELS;
ELSE
BEGIN
(* READER *)
IF NOT RORGNT(INRAN) THEN
BEGIN
CLST:
PROCEDURE STAEO:
(* TEST STATUS OPTION *)
BEGIN
IF ODRERR THEN
BEGIN
PROCEDURE STAAT:
(* PROCEDURE TO EXECUTE IF EQUAL *)
BEGIN
IF INRA = A THEN
BEGIN
BEGIN
(* STACWI *)
(* CLEAR STATUS *)
INT := LITE;
(* DEFAULT SIDE WHITE *)
Z11 (* STATUS OPTION EXIT *)
WHILE RORGNT(INRAN) DO
BEGIN
STACWI():
(* CLEAR STATUS *)
PROCEDURE WHAIC:
(* COMMAND - WHAT? *)
BEGIN
(* READER *)
WHILE NOT RORGNT DO
RLOGIN;
(* COMMAND EXITS *)
BOARD.RBS := BOARD.RBS + ELS;
PROCEDURE STAEO:
(* SET SIDE TO MOVE *)
BEGIN
BOARD.RBS := INT;
(* STM *)
END (* STAEO *);
PROCEDURE STAAG:
(* SET BLACK OPTIONS *)
BEGIN
INT := DARK;
(* STM *)
END (* STAAG *);
PROCEDURE STAEPE:
(* SET ENPASSANT FILE *)
BEGIN
IF NOT RORGNT(INRAN) THEN
BEGIN
RDRERR;
PROCEDURE STACAR:
(* ALLOW CASTLE QUEEN SIDE *)
BEGIN
IF INT = LITE THEN
BEGIN
BOARD.RBS := BOARD.RBS + (ELS);
ELSE
BOARD.RBS := BOARD.RBS + (ELS);
END (* STACAR *);
PROCEDURE STAK:
(* ALLOW CASTLE QUEEN SIDE *)
BEGIN
(* STACGO *)
(* CLEAR STATUS *)
INT := LITE;
(* DEFAULT SIDE WHITE *)
Z11 (* STATUS OPTION EXIT *)
WHILE RORGNT(INRAN) DO
BEGIN
STACGO():
(* CLEAR STATUS *)
PROCEDURE STAAT:
(* COMMAND - LAST MESSAGE *)
BEGIN
WHILE RLOGIN DO
RLOGIN;
Listing 1, continued:

IF NOT THEN
BEGIN
  WRITE("*");
  FOR INTJ = A1 TO J2 DO
    WRITE(IMAGE(INTJ));
  WRITE("\n");
END:

PROCEDURE ADDCHR
  (* ADD CHARACTER TO MESSAGE *)
_BEGIN
  MOVEMS(INTM) = A;
  IF INTM = F4 THEN
    INTM = INTM + 1;
_END:

PROCEDURE ADDSQP
  (* ADD SQUARE TO MESSAGE *)
_EXTERN
  (AIRM:
    BIT1);
Listing 1, continued:

IF RMD THEN         (* CASTLE *)
  BEGIN
    ADDRD1"-D-0 "; 31
    IF RMD THEN
      ADDRD1"-D-1 "; 21
    END
  ELSE
    IF RMD THEN
      HINGE4(A,FMC,FMCL)
      ELSE
      SIMPLE MOVE *)
    IF RMD THEN
      PROMOTION *)
  BEGIN
    ADDCR1("=")
    ADDCR1(16CRPPII)
    END
    ADDRD1"-D- "; 31
    IF RMD THEN
      (* CHECK *)
    BEGIN
      ADDRD1("CHECK "; 151
      IF RMD THEN
        (* CHECKMATE *)
      ADDCR1("=")
      END
    ELSE
      (* STALEMATE *)
      ADDRD1("STALEMATE; ",10 l
      END
    END      (* NINGE *)

PROCEDURE HMOVIE:     (* MAKE MACHINES MOVE *)
  VAR
    INNM: RNI
    (* THE MOVE *)
  BEGIN
    CREATE
    (* INITIALIZE DATA BASE *)
    INNM "HOMESSEARCHI
    (* FIND THE BEST MOVE *)
    IF INNM, RNI THEN
      (* NO MOVE FOUND *)
      BEGIN
        GOING = 81
        IF LITE.RNIC THEN
          (* CONGRATULATIONS *)
        ELSE
          WRITEL "DRAWN, "
        END
      END
    ELSE
      (* STALEMATE *)
      BEGIN
        WRITEL "GAME OVER, "
        (* TRANSLATE MOVE TO ENGLISH *)
        WRITECNI(HOMES)
        (* TELL THE PLAYER *)
        THEN
        IF SWU THEN
          WRITEL "BISHOP, "
          (* MAKE THE MOVE *)
        END
      END
      (* NINGE *)
    END

PROCEDURE YMHOVE:     (* MAKE PLAYERS MOVE *)
  LABEL
    1, 2, 7, 16, 15:
    (* SYNTAX MICES *)
    16:
    (* AMBIGUOUS MOVE *)
    17:
    (* NORMAL EXIT *)
  VAR
    IF: TBI
    (* VALU MOVES FOUND *)
    INTC1 TCI
    (* CURRENT CHARACTER *)
    INTM: TJI
    (* MOVES INDEX *)
    INTP: TPI
    (* MOVING PIECE *)
    INCP: TPI
    (* CAPTURED PIECE *)
    INCF: TBI
    (* CASTLE *)
    INFCPS: TBI
    (* QUEEN SIDE CASTLE *)
    INTP1 TGI
    (* PROMOTION TYPE *)
    IFP: TBI
    (* MOVE FOUND *)
    IFD1 TBI
    (* R, N, B OR Q ON LEFT *)
    IFL1 TBI
    (* K OR Q ON RIGHT *)
    IFP: TBI
    (* K OR Q ON RIGHT *)
    ILNF: SFI
    (* FILES ON LEFT *)
    INLF: SFI
    (* FILES ON RIGHT *)
    INFS: SFI
    (* BISHOP FILE *)
    INRM: RH
    (* THE MOVE *)
  FUNCTION HOMIC
  (* DETERMINE IF NEXT INPUT CHARACTER IS NOT IN A GIVEN SET *)
  (* SET OF CHARACTERS TO CHECK *)
  (* SEMANTICS ROUTINE TO CALL *)
  IF NEXT CHARACTER IS IN SET *)
  (* TRUE IF CHARACTER IS NOT IN SET *)
  VAR
    INTB: TBI
    (* SCRATCH *)
BEGIN
  INTB = 0 (INTC IN A):
  IF NOT INTD THEN
  BEGIN
    YMHOVE:
    (* EXECUTE SEMANTICS ROUTINE *)
    IF JNTJ = INTC1 THEN
      (* ADVANCE PASS CHARACTER *)
      BEGIN
        JNTJ = JNTJelligent
        IF INTC1 = "-" OR INTC1 = "1" THEN
          (* EXIT SCAN *)
          END
        HOMIC := INTB1
        (* RETURN TRUE IF CHARACTER IS NOT IN STRING *)
        END
    END
    ELSE
      (* NOMIC *)
      BEGIN
        (* FOUND A MOVE, EXITS TO AMBIGUS MOVE IF THIS IS THE SECOND POSSIBLE MOVE, SAVES THE MOVE IN INRM OTHERWISE *)
        IF IFW THEN GOTO 171
        IF IFW THEN "HOMESSEARCHI
        IF IFW THEN MOVESININT1I
        END
        (* YMM )
      END
    PROCEDURE YRCM:
    (* COMPARE SQUARES, CALLS YMM HOMESSEARCHI MOVE THE RIGHT TYPE OF PIECE, CAPTURES THE RIGHT TYPE OF PIECE, AND MOVES TO AND FROM POSSIBLE SQUARES *)
BEGIN
  IF IFL1 = "-" THEN
    (* SEMANTICS - CAPTURE *)
    IF IFL1 THEN
      (* SEMANTICS - CASTLE *)
      BEGIN
        IF IFL1 THEN
          (* SEMANTICS - CAPTURE PIECE *)
          BEGIN
            CASE INTC1 OF
              "F": INCP1 XTUMEP[OMEREMJNTJ]
              "W": INCP1 XTUMEF[OMEREMJNTJ]
              "B": INCP1 XTUMP[OMEREMJNTJ]
              "Q": INCP1 XTUMP[OMEREMJNTJ]
            END
            END
          END
        END
      END
    END
    (* SEMANTICS - CASTLE LONG *)
    BEGIN
      IF IFL1 THEN
        (* SEMANTICS - K OR Q ON LEFT *)
        BEGIN
          CASE INTC1 OF
            "K": INLF = [F1,F2] = INLF1
            "Q": INLF = [F1,F2] = INLF1
            (* KING SIDE *)
            IF IFL1 THEN
              END
              (* YMM *)
            END
          END
        END
      END
    END
    (* SEMANTICS - R, N, B OR Q ON LEFT *)
    BEGIN
      CASE INTC1 OF
        "K": INLF = [F2,F3] = INLF1
        "W": INLF = [F2,F3] = INLF1
        "B": INLF = [F2,F3] = INLF1
        "Q": INLF = [F2,F3] = INLF1
      END
      END
    END
    (* SEMANTICS - R, N, OR B ON RIGHT *)
    BEGIN
      CASE INTC1 OF
        "N": INLF = [F2,F3] = INLF1
        "K": INLF = [F2,F3] = INLF1
        "B": INLF = [F2,F3] = INLF1
      END
      IFL1 = "-" THEN
        END
        (* YMM *)
      END
    END
    (* SEMANTICS - RANK OR LEF *)
    BEGIN
      CASE INTC1 OF
        "K": INLF = [F2,F3] = INLF1
        "W": INLF = [F2,F3] = INLF1
        "B": INLF = [F2,F3] = INLF1
      END
      IF IFL1 THEN
        END
        (* YMM *)
      END
    END
  IF JNTJ = "-" THEN
  BEGIN
    IF JNTJ = "LITE THEN

CHESS SKILL IN MAN AND MACHINE edited by Peter W Frey.
A game of endless variations, chess has challenged our skill for centuries. This book surveys our current understanding of human chess skill and covers the subtleties of coaxing a machine to play chess. The initial chapter and appendix present a brief history of the computer chess tournaments. The next two chapters describe the essentials of how humans and computers play chess. The fourth chapter provides a detailed description of the Northwestern Chess Program, currently the national champion. The following three chapters discuss several alternative approaches to chess programming. In the final chapter, a former captain of the U.S. Olympic chess team assesses the present status of chess skill in human and machine. 217 pp. $14.80 hardcover.

The sixth annual U.S. Computer Chess Championship, held in October 1975, was a tournament in which twelve computer programs competed against each other. This book includes a detailed analysis and description of all the games, presented by David Levy, the tournament director. 86 pp. $5.95.

AN EDITOR/ASSEMBLER SYSTEM FOR 8080/8085 BASED COMPUTERS by W J Weller and WT Powers.
This 148-page book contains complete information for initializing and using a powerful new editor/assembler and debugging monitor system, and the full SOURCE text of both. The assembler fully supports all Intel instruction mnemonics as well as the entire language used in PRACTICAL MICROCOMPUTER PROGRAMMING™: THE INTEL 8080. The editor/assembler is resident in less than 8K RAM and will run on any 8080, 8085 or 280 based computer with peripherals which transfer on a character by character basis or can be made to do so by buffering. The user supplies his own I/O drivers. The text editor is extremely simple to use and does not require irrelevant line numbers. Also included is a program to convert Processor Technology™ format tapes to a format usable by the editor/assembler.

This system is not the usual “quickie” software, riddled with errors and limitations, but a professionally created, thoroughly tested and debugged system. At $14.95 it is the best software bargain you are ever likely to see. AND BY THE WAY... paper tape object copies of all of this software are sent FREE to book purchasers when the coupon at the back of the book is returned to Northern Technology Books. 8½ x 11 format. $14.95.

STANDARD DICTIONARY OF COMPUTERS AND INFORMATION PROCESSING 2nd Edition by Martin H Weik.
This is a very complete, fully cross-referenced dictionary. It goes a step farther in that it includes full explanations, practical examples, many pertinent illustrations, and supplementary information for over 12,500 hardware and software terms. It cross-references the terms to other closely related concepts, and appended to each definition, as the need arises, are explanations, tutorial information, examples, usage areas, and cross-references for further clarification of concepts and meanings. 390 pp. $16.95 hardcover. (No photo)
BEGIN
(• YR MOVE •I
INTB 1::1 FALSE;
MHllE NOT INT B 00
BEGIN
READER I
lSTNOVI
trCA I • F Al SE I
If PR 1 • F Al SE I
IFOO u FIL SE;
IFQS
FALSE;
If LO Is F Al SE:
lflf I• FALSCI
1r•o •• FALSE I
1r11r • • FAlSEI
lNTP I• NTI
INCP I• NTI
IHLr I• IFl •• Fll I
tfrdtr I • [Fl • • Flll
INLR I • IRl •• Rlll
IHRR I• l Rl •• Alli

Listing l , continued:

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ELSE
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·1·1 INLR
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"J"I INLR
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lNLR
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lNlR
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C• YA:MUtK •
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INTC

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,YRMLRICJ
111
c• LEFT SIDE DONE •t
IF NOT NCHINl["·"I
, YRMMUl t
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,YRMCAltl
Jr
NCHINC(•p•,•11t·.·N·,·B·.·Q·1
, YRMCPC I
, 'fRMNUll
IF
NCHINll "/"I
121
c• RI,HT SIDE SQUARE •1
, Yl:MRCQI
tr
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, 'fRM•R:ll
IF
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, YRMRRCI
lll
c• PROMOflON •t
If
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, YRMNULI
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NCHIN((-~-.-..-.-.-.-Q-1
,YRMPl:OJ
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C• SE"ANTICS •

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PROCEDURE YANPCNI

I• SEMANTICS •

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BEGIN
CASE !HTC OF
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INTP
INTP I •
INTP
•1(•1 lNTP
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ENOI
YR:MPCN

XTUMPfEP • .INT"J1
ITUMP([R:,JNTMJ;

XTUMPIEN,JNTMJ;

ITU"PI El!lt JNTM It

XTU"PlEQ,JNTNJ;
ITU"P([l(,JNTNJ;

PIECE MOVED • 1

....•••• .,
,••.

PAWN •1
ROOK
l(HICNT •J
BISHOP •J
QUEEN • 1
KING • J

l~I

trrfCHIN(( .. 0•,•0•1
NCHINfl•-•1
HCHINIC•o•,•0•1
NCHIN(( · - · 1
NCHINC(·o·.-a-1
SYHTAX CORRECT •J

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,YRMNULI
,Yf(MNULl
, YftMCASI
,YRHCQSl
, Y'RMNULJ

IF

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PROCEDURE

IFRF ANO HOT IFRO THEN
lNA:F I • IHRF • (F ... F"SJ;
IFLF ANO HOT IFLO THEN
lNLF I • INLF • (Flt,F51;
IF"V I • FALSE:
INTll 11• IN ;
NHilE INTN c JNTN 00
MITH "OVESl IHTMJ 00
BEGIN
IF lt"PA: • IFPR fHEN
If R"PR THEN
IF R"PP a INTG THEN
YRl'ICO"
El SE
El SE
IF A:"OO s IFOO THEN
tr RMOO THEN
IF li.MQS a IFQS THEN
YA:MHIT
ElSE
El SE
YRNCON:
INTll I • INTIHl;
[MO;
IF IFNV THEM
BEt;IN
NINENGCINIUl,"YOUlt MOVE "IJ
MRITElNCNOVNSI I
TH[NOV 1 INRNl I
INT8 I• TA:U£1
ENO
ELSE
•RITElNI" lllEGAl HOVE,"11
GOTO 11:
IF

PRO"OflON •J

t• R001( •J
(• l(HICHT •1
(• BISHOP •J
t• QUEEN •J

P5l&
PN;

PBS
PQ;
.,

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YRNRICQ;

SE"IHTICS •

I( OR Q OH IUCHT •1

BEGIN
CASE lNTC OF

•1(•1 INltF I• lf5 •• fl1 • 1Nttf1
•a•• JNltf •• 1 r1 •• ,,, • uutr1
ENOJ
IFRF
ENO;

I•

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1 • QU[[M SIO[ •I

TA:UU
YlltNLICQ •J

I• SE"ANT ICS •
ltJGHT •J

PROCEDURE YRNRllB J

BEGIN
CASE

1• KING SIDE •1

R, H, OR I ON

lNTC OF

•1t•1
•..-1
•9•1

Ullt:F I• (Fl,F'll •

INA.F'S

lNlltf I• (f2,F7J •
INA:f I• 1Fl,f61 •

INA:f1
INA.F:

I• ROOI( rtLE •1
1• KNIGHT rILE •1

c•

161

BISHOP rtLE . ,

ENO;

tFRO I• TRUE;
ENO;

c•

TM[N GOTO 1a.1
TH[M COTO 11;
TM[N'
TM[Nt
THEM•
TH[M
THEM
THEN
THEN

lZl
1'1

GOTO
GOTO
GOTO
GOTO

161
131

THEMI
TH[MJ
TH[NI
THEM GOTO 151
THEN t;OTO 161

t• CASTLING •t
If
IF
If
IF
If

lSI

1• SE"ANTICS BEGIN
CASE lNTC OF
A:""1 INTG
00
H 00 1 INTG I •
1•1 HUG t•
•g•1 INTC. I •
ENOJ
If PR I• TRUE;
END:
(• YA.MPR:O

LEGAL MOVES • 1

If
IF
tr
IF
tr

PROCEDURE YA:"NUL;
BEGIN
[NO:

l a

1• READ NEXT MOVE •1
1• LIST

(• SYNTAX ERROR. •1
111111.ITELN(• SYNTAX ERROR.•t 1
GOTO 111

THEN
THEN
THEN
THEN
THEN

GOTO
GOTO
GOTO
GOTO
GOTO

161
16 .:

16;

is;

16;

....
..

SELECT K OR Q FILE • l

••••

CORRECT PROMOTION TYPE •1
COMPARE SOUA•ES ANO PIECES •1

SELECT K OR Q r ILE •I
NO HOV[ FOUND Y'Ef •J
1 • lNITUllZE !HOE<

.,

c•

NOT PROMOTION •1

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CASTLING ·~
CASTl ING SANE MAY

c.

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••••

NOT CASTLING •I
COMPARE SOUARES ANO PIECES • 1
ADVANCE NOV[S INO[X • 1

c•
c•
c•
c•

OM[ NOYI FOUND •1

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..••

COMV[RT TO OUR STYL[
PRINT llOV( •I
NU[ TH[ llOVE •1
UIT YRNOVf • 1

•1

NO MOVES fOUlllO •t

EXIT •1

t• Ertf •t

YA:NLRB . ,
171
111
1• SE"AHTICS •

PROCEDURE YRNRIU I

lt&NK ON ltICMT

•1

( • AMBIGUOUS MOYE •)
MIUTELN(• AMBIGUOUS MOVE.•J l
f• EXIT •1

ENO I
ENO :

c•

Y'RMOVE •1

BEGIN

If JNTN a LITE THEN
CASE !HTC OF
•1•1 INRA. I•
•z•1 INIUt r •
•3•1 IHIUt I•
.. ,,. ... IHRA: I,.
•5•1 INRR I•
•&•1 IHRR 1 :
-1-1 INRR 1 •
•a-1 INRR I :
ENO
El SE
CASE INTC OF
•1 ""1 INRR I•
1 INRR 1z
•1•1 INRR
.. ,,. .. , INRR I a
•5•1 INRR I•
•&•1 INRR I a
•7•1 IHRR
•1•1 IHRR 1 a
ENO:
c• Y'R"LRK •1
ENO;

·z ..

156

lRl II
I RZ 11
!Al J:

IR• I I

l Q5"
I 06 J:

BEGIN
C• THE PROGRAM •I
WA:lf[LN(• HI,
THIS IS CHESS
lNICOH:
1 1

l R7 J:
I RI 1;

IR8ll

(R7J:
l Rf> J;
(R5 J;
CR .. I;
(Rl 1:
I RZ It
I Rl I;

December 1978 © BYTE Publicuions Inc

21

c•

.s•q

INITIALIZE FOA A NEiii GAME •J
INITIL CBOAA:OI:
REPEAT
REPEAT
'fRMOVE:
UNTIL SMR[ I

(• EXECUTE "ACHilrillES MOVE •t
REPEAT
NY HOVE I
IF GOING > 0 THEN
GOING 1• GOING•ll
UNTIL GOING a 0;
UNTIL FALSE:

9 I
C•
ENO.

ENO Of PROCtU M •I

t• INITIALIZE COtillSTINTS •t

c•

INitlALlZC 'OR A NEiii GAME

c•

EXECUTE PLIYEl:S MOVE

•J

•t


A second and somewhat more challenging project would be to develop a transposition table for the program. This requires the availability of unused memory (at least 8 K bytes and preferably 16 K or 32 K bytes), an efficient hashing scheme, and a set of decision rules to select among positions when a collision occurs (i.e., two positions hash to the same address in the table). Another problem is that the use of a staged evaluation process and the α-β algorithm often provides an imprecise evaluation score (i.e., the machine has determined that a position was not optimal but has not invested the time to find out exactly how bad it was). If the programmer succeeds with the transposition table, however, move calculation will take 30 to 50 per cent less time in most middle game positions and 60 to 90 per cent less time in many end game positions.

A third area for improvement is the evaluation function. Our program presently has only a rudimentary function. The reader should compare it with the one used by Chess 4.5 which is described in detail by Slate and Atkin. Their evaluation function provides an excellent starting point for revising our present function. In part 4 we will discuss the advantages of using a conditional evaluation function, i.e., one that changes depending on the stage of the game and on the presence of special features. One implementation of this strategy is the special end game program described by Monroe Newborn in Chess Skill in Man and Machine.

It is appropriate for us to add two important disclaimers at this juncture. Although we have carefully tested each of the routines in the program and played several chess games, it is still possible that there are a few minor bugs in the program. If you find one, a letter to one of us or to BYTE would be appreciated. Secondly, our chess program was written primarily for pedagogical purposes. For this reason it is not a production program and does not run very efficiently. If you are the competitive type, our program should provide many useful ideas, but you should not expect it to compete successfully in tournament play unless you make extensive modifications and additions.

A chess program has a tendency to grow and change its personality as the programmer becomes more familiar with each of its many limitations. It provides a constant challenge for those of us who are too compulsive to tolerate obvious weaknesses. In fact one must be careful not to become totally obsessed with this project. We do not wish any of you to lose your job or your spouse because of a chess program.
recovery from transmission errors. Add to this the fact that the protocol has been in service a number of years, and I am sure readers will find the literature worth reviewing.

Carroll Perkins
POB 333
Pilot Mountain NC 27041

SIZING UP MODULAR PROGRAMMING

I enjoyed the “Top-Down Modular Programming” by Albert D Hearn in the July 1978 BYTE, page 32. I thought he did a good job of explaining the subject. While I realize that he was purposely trying to simplify matters, I do take exception to his comment that a module should be no more than 50 lines long.

The concepts of structured programming are intended as guidelines, not as dogma for a programmer’s religion. All of the better known proponents of the methodology stress this point, along with the idea that you must approach the study of structured programming with your eyes open, making your own evaluation. In this light let us explore the 50 line limit.

One of the bases for breaking a program up into modules is so that a complex problem can be handled with small, easy to understand pieces of code. One of the thoughts about module size is, therefore, that a module ought to be able to fit on one printed page. This is so that all the information about the module is in one place and the programmer won’t have to thumb through several pages to read the code for a single module. Having experienced “modules” running as long as 10 to 15 pages, I heartily agree with this philosophy.

In professional programming installations, this idea has frequently been translated into a local standard of about 50 lines of code, since this is the number of lines which are printed on an 8.5 by 11 inch (21.59 by 27.94 cm) page coming out of a line printer (allowing for headers, footers, etc). For the personal computer enthusiast, however, this limit might be more conveniently set at 24, 32 or 40 lines—the size of the video display.

For many more complex problems, it is possible that a significant module cannot be constructed in 24 lines. This is no problem—just make the modules longer. The point is to try to restrict the module size to a length which enhances the programmer’s ability to understand the code.

James Fleming
2220 Sims Dr
Columbus IN 47201

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A Sidney Alpert
University Patents Inc
2777 Summer St
Stamford CT 06905

Steve Ciarcia replies:

While I am personally aware of
journalistic freedoms with regard to
patents, many readers may not be. Your
statement is well taken. It should be
further noted that the University of
Illinois patents appear to cover the
scanning principle and not the design
circuitry.

PLATO AND THE TOUCH PANEL

I lead a double life: during the night
I make up little things for my own
Apple, but during the day I become a
rising young training executive of the
CDC Plato terminal.

And that’s why Steve Ciarcia’s article
on touch input units brought me up with
a start — because his touch panel is
nearly identical to the touch panels
put on the first Plato terminals! I’m
taking about the original Magnavox
terminals that brought Plato out of the
lab in Illinois and into the world. Those
terminals, just like Steve’s monitor,
had a picture frame around them with
32 LEDs and 32 phototransistors. In
fact, there are only minor differences
between them and Steve’s design except
for the aspect ratio — Plato terminals
have square screens. The Plato panels
even had a built-in circuit that triggered
the 0.1 second beep Steve mentioned
in his article.

One minor difference was that Plato
panels had the LEDs on the top and
the phototransistors on the bottom.
Steve’s method is better — the old touch
panels would fall regularly whenever the
sun shone on them at the wrong angle.

Those old panels are obsolete now.
Both CDC and the other Plato terminal
maker are using different designs, under
direct control from an internal micro-
processor. But there are still plenty of
the old Magnavox boxes out there, in
schools and colleges across the country.
In fact, three microprocessor systems
that I know of display output through
a gat ed and rewired Magnavox box,
bo unched on the “orange and black
market.” (named for the color of the
old plasma screens, you know.)

Silas S Warner
8 Charles Plaza
Baltimore MD 21201

Steve Ciarcia replies:

Thank you for the vote of confi-
dence. It may interest you to know that
I worked for Control Data Corporation
for three years as a process control
engineering consultant. During that time
I became familiar with Plato, but never
have, to this day, used the touch input
feature. I just liked to go in after work
and play Star Trek or Empire against
other people on the system throughout
the country.

The design illustrated in BYTE was
done from scratch and any resemblance
to Plato is purely coincidental. I just
got an idea for it one Friday afternoon
and brought the completed unit into
the office Monday morning.

VOICING AN OPINION

Congratulations to Bill Georgiou for
his excellent primer on speech recog-
nition in June 1978 BYTE (“Give an Ear
to Your Computer,” page 56). This
wide-ranging and complex topic was
presented in a most understandable
form, yet did not sacrifice excessive
detail.

As Mr Georgiou stated, voice recogni-
tion has a rather long history, and has
intrigued avid experimenters such as
myself for some time. Back in 1965, I
designed and built a demonstration unit
capable of differentiating ten different
words or short phrases, and activating
one of ten relays upon completion of
analysis. The project was awarded a first
prize at the Canada-Wide Science Fair
that year.

The implementation was not unlike
figure 12 in the article, an automatic
gain control stage followed by multiple
bandpass filters, except that all pro-
cessing was done in analog. A degree of
differential comparison was incor-
porated, to provide for the variableness
of fundamental pitch in each speaker.
Template matching was used, with a
great deal of “cut-and-try” programming
effort. And if Mr Georgiou thinks the
Bell Labs version of 1952 was “gro-
tesque,” he should have seen this one,
built from old television sets and record
players.

Although the machine displayed
about a 90 percent recognition rate for
my voice (it had obviously been pro-
grammed that way), I was constantly
surprised during public demonstrations
how often it would react correctly to a
“stranger’s” voice. With a little practice,
even a feminine voice could speak the
word “open” and see my little solenoid
lock snap back.

The article has rekindled my interest
in the field, and I shall be looking for-
ward to implementation with my micro-
processor now.

F Wallace
Burroughs Business Machines Ltd
POB 861
Winnipeg, Manitoba
CANADA R3C 2P7

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Newcomb’s letter on the evils of radio
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☐ Send me more information on AIM 65.
☐ Have someone phone me at ____________________________

Name__________________________ Address__________________________

__________________________ ____________________________

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communications between computers, having just read the DOC’s (the Canadian FCC) proposals on the “Packet Radio Service.” Welcome to the 19th century, Mr. Newcomb!

The DOC is proposing not 1 MHz, but the entire amateur radio 220 MHz band and very likely will finalize at 220-221 MHz, leaving room for a communicator class or GRS (CB) service in the remaining 4 MHz. Our FCC, which works very closely with the DOC, is thinking along the same lines.

Unquestionably, we’ll have radio communications between computers within the next year or two. I, for one, am extremely excited by the fantastic possibilities, and am already working on suitable equipment. I’d appreciate hearing from others working along the same lines.

Donad L Stoner W6TNS/7
John Hancock Blvd
Mercer Island WA 98040

IDEAS NEEDED FOR PROJECT TO AID DISABLED

The Spain Rehabilitation Center at the University of Alabama Medical Center has a project underway to demonstrate both the utility and economic feasibility of the new generation of personal computers for use by the severely disabled. The programmability of the computer will allow it to serve as a general purpose appliance to be used as an aid to communication and education as well as for environmental control and entertainment.

This system, as currently envisioned, will consist of a microcomputer; an on line storage device for programs and data; two television monitors for user feedback and information display; a printing device for typed output; a speech recognition device for vocal input of commands, data, and text; a power line controller for environmental control; and a telephone dialing and answering device. We are attempting to select components which are widely distributed and serviced as well as being plug compatible and economically priced.

Programs will be written or purchased to perform specific functions in each of the four general areas mentioned above. However, we would be very interested in receiving ideas from your readers, particularly those who are disabled, those who have disabled friends or relatives, and those who have personal computers and would like to develop hardware or software for the system on their own, regarding specific functions which they would like to see developed and which could be accommodated by the proposed microcomputer system.

We are looking forward to receiving input from anyone who may be interested in this project.

Charles Healey
Spain Rehabilitation Center
UAB University Sta
Birmingham AL 35294

Circle 313 on inquiry card.
Pascal for Computer Club Members

The UCSD Pascal Project has announced a special offer for bona fide computer clubs. The UCSD Pascal software, which normally sells for $200, will be made available to club members at a substantial discount if the club assists in the copying and production costs for disseminating the software. For more information, computer clubs should contact Tracy Barrett, CO 21, UCSD, La Jolla CA 92039.

Some BOMB Reflections

Occasionally we like to share some of the unfettered comments, pro and con, that arrive monthly on the BOMB cards, our system for reader response through a postcard at the back of the magazine.

The following BOMB card came from an anonymous Pascal enthusiast:

```
We have been suitably chastened. This is the first time we have been accused of not being subjective enough, and we will attempt to examine the problem as subjectively as possible...CM
```

Other BOMB comments about the August issue include:

**Best BYTE I have read in a long time. Please devote more discussion to Pascal. The language in its beauty, compactness and readability is worth talking about. Would like to know more about the extensions being discussed for the language.**

The article by Weems ("Designing Structured Programs") was easy to comprehend and delivered a valuable message.

This was one of your best issues, I like having related articles in one issue.

To be fair, not all the comments were as positive as the last three. The following BOMB card was also received for the month of August:

```
BOMB: BYTE's Ongoing Monitor Box 418

Some BOMB Reflections

Attention: HAL 9000 Owners

We have just received word of an important new book: Programming Instructions for the HAL 9000 Computer, revised edition. The new edition of the HAL 9000 handbook has been updated to incorporate improvements suggested by this versatile machine's surviving users. In particular, the manufacturers suggest that priority be given to the retrofitting of small explosive charges at strategic points in the central memory unit.

Authorized by Arthur C Clarke
Chief Semantic Controls Engineer
Colombo SRI LANKA

Best BYTE I have read in a long time. Please devote more discussion to Pascal. The language in its beauty, compactness and readability is worth talking about. Would like to know more about the extensions being discussed for the language.

The article by Weems ("Designing Structured Programs") was easy to comprehend and delivered a valuable message.

This was one of your best issues, I like having related articles in one issue.

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BOMB: BYTE's Ongoing Monitor Box 418

Incremental Motion Control Symposium
Issues a Call for Papers

The Eighth Annual Symposium on Incremental Motion Control Systems and Devices will be held at the Ramada Inn, Urbana IL, May 21 thru 24 1979. A call for papers has been issued by Prof B C Kuo, director of the symposium, which is sponsored by the Incremental Motion Control Systems Society, in cooperation with the University of Illinois, Dept of Mechanical Engineering, and Warner Electric Brake and Clutch Company of Beloit WI.

The symposium will encompass a broad area with sessions devoted to tutorial papers as well as original contributions, covering step motors,
Circle 33 on inquiry card.

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Machine tool control systems, computer controls, linear and AC/DC motors, clutch-brake devices and systems, and related incremental motion control applications. Exhibit space will be available.

The call for papers, both theoretical and practical, related to incremental motion control systems and devices, requests authors to submit a summary of about 500 words by January 1. Final manuscripts will be due around mid March. Send all summaries and inquiries to Dr B C Kuo, POB 2772, Station A, Champaign IL 61820, phone (217) 333-4341.

A Call for Papers

The Instrument Society of America has issued a call for papers for its 1979 conference and exhibit, ISA/79. The conference will take place at the O'Hare Exposition Center in Chicago IL, from October 22 through 25 1979. The conference theme, Instrumentation for Energy Alternatives, will emphasize current practices in instrumentation design and implementation. Papers are being sought in the following areas: analysis, automatic control, chemicals and petroleum, cryogenics, data handling and computation, education and training, food, glass and ceramics, maintenance, management, marine sciences, metals, mining and metallurgy, power, process measurement and control, standards and practices, telemetry, test measurement, water and wastewater, pulp and paper, and biomedical instrumentation. Paper topics should introduce or explain techniques or innovations in instrumentation and control system design, testing, operation and maintenance. The papers may be either theoretical in nature or application oriented. The deadline for unsolicited abstracts is February 5 1979. The appropriate forms should be requested from: ISA/79, Instrument Society of America, 400 Stanwix St, Pittsburgh PA 15222.

American Management Association Offers Courses for EDP and NonEDP Professionals

The American Management Association's Information Systems and Technology Division is offering courses for both the electronic data processing (EDP) and nonEDP professional managers. A sampling of the courses offered include: systems analysis and design computer security, minicomputers, distributed data processing, fundamentals of EDP, office automation, EDP applications to human resources and much more. The courses run through March 1979. A brochure...
Chess Bug

Due to an oversight on our part, a number of errors appeared in the October 1978 "In This BYTE" entry (page 4) for "Creating a Chessplayer" by Peter W Frey and Larry Atkin. The introduction implies that Peter Frey is one of the creators of Chess 4.6. This is not true. The program was written by Larry Atkin and David Slate. Peter Frey was also erroneously referred to as "David" Frey, and Larry Atkin as Larry "Atkins." We sincerely apologize to all concerned for these errors.

Address Change

In the "What's New?" section of November 1978 BYTE we reported on a new product from TSA Software (page 216). This company has notified us of a change of address. Their new address is: 39 Williams Dr, Monroe CT 06468.

Tilt!

Some errors crept into the Pinball Wizard program that appeared in my article "The HP-67 and HP-97: Hewlett-Packard's Personal Computers" (June 1978 BYTE, page 112). The code in step 69 of listing 1 (page 114) should read "35 00", not "36 00"; the key entry is correct, however. Also, step 189 (page 115) should read "RCL B 36 12", not "RCL B 36 06," and step 139 should read LBL 0 21 00 instead of LBL 0 21 16. My apologies to any readers who might have experienced difficulties in using the program.

Craig A Pierce
2529 S Home Av
Brewyn IL 60402

Circle 280 on inquiry card.

Dec 1978 © BYTE Publications Inc
In order to gain optimum coverage of your organization's computer conferences, seminars, workshops, courses, etc, notice should reach our office at least three months in advance of the date of the event. Entries should be sent to: Event Queue, BYTE Publications, 70 Main St, Peterborough NH 03458.

December 3-5, Ninth North American Computer Chess Championship, Sheraton Park Hotel, Washington DC. The 1978 annual meeting of the Association for Computing Machinery will be the site of this chess championship. This will be a 4 round Swiss style tournament with participants restricted to computers. Two rounds will be played on December 3 (1 PM and 7:30 PM), one on Monday (7:30 PM) and the last round on Tuesday (7:30 PM). Deadline for entries is October 20. Contact Prof M M Newborn, School of Computer Science, McGill University, Montreal Quebec H3A 2K6, CANADA.

December 4-6, 1978 Annual Conference of the Association for Computing Machinery, Sheraton Park Hotel, Washington DC. Contact Dr Richard Austing, Dept of Computer Science, University of Maryland, College Park MD 20742, (301) 454-2004.

December 4-6, Minicomputers and Distributed Processing, Atlanta GA. This 3 day seminar will examine the uses, economics, programming and implementation of minicomputers. Contact Phillip M Kowlen, director, Center for Continuing Education, The University of Chicago, 1307 E 60th St, Chicago IL 60637.

December 4-8, Microcomputer Software Design, Virginia Polytechnic Institute and State University, Blacksburg VA. This workshop will develop assembly language programming skill for 8080 and 8085 based microcomputers. Topics to be discussed include floating point mathematics, lookup tables, number base conversion, interrupt programming, searching and sorting. Contact Dr Linda Leffel, Donaldson Brown Center for Continuing Education, Virginia Polytechnic Institute and State University, Blacksburg VA 24061, (703) 951-5421.

December 6-8, Data Processing Operations Management, Washington DC. This 3 day seminar will emphasize the management skill and techniques applicable to the data processing operations function. Contact Dr Linda Leffel, Donaldson Brown Center for Continuing Education, The University of Chicago, 1307 E 60th St, Chicago IL 60637.

December 12-14, Midcon/78, Dallas Convention Center, High Technology electronics show and convention. Contact Electronic Conventions Inc, El Segundo CA, (800) 421-6816 (toll free).

December 13, Computer Networking Symposium. Sponsored by the IEEE Computer Society's Technical Committee on Computer Communications and the Institute for Computer Sciences and Technology of the National Bureau of Standards. This symposium will highlight papers of practical and research experiences concerning both computer and communication networks. Contact Dr George Cowan, Computer Sciences Corp, 6565 Arlington Blvd, Falls Church VA 22046.

December 13-15, Distributed Mini-computer Networks, Executive Tower Inn, Denver CO. This seminar will address the minicomputer from the viewpoint of the distributed network user. The structure and management of a large data base and software problems with the trade-offs of languages utilized, hardware types, input and output options, device controllers, system failure and recovery, sample application case studies and the economics of minicomputer applications will be covered in depth. Contact The Institute for Professional Education, Suite 601, 1901 N Fort Myer Dr, Arlington VA 22209, (703) 527-8700.

December 18-21, Microcomputer Data Acquisition, Instrumentation and Measurement Systems, Virginia Polytechnic Institute and State University. Course to be given by the authors of the Bugbooks. Contact Dr Linda Leffel, Donaldson Brown Center for Continuing Education, Virginia Polytechnic Institute and State University, Blacksburg VA 24061, (703) 951-5421.

January 8-12, Structured Programming and Software Engineering, George Washington University, Washington DC. This course is designed for experienced program architects, designers and managers. It will provide up to date technical knowledge of logical expressions, analysis and invention for performing and managing software archi-
tecture, design and production. Presentations will cover principles and applications in structured programming and software engineering. Design workshops with analysis and review sessions will provide actual practice in problem solving. Contact George Washington University, Continuing Engineering Education, Washington DC 20052.

January 15-17, Minicomputers and Distributed Processing, San Francisco. For details, see December 4-6, Atlanta.

January 17-19, Distributed Minicomputer Networks, Ramada Inn, Arlington VA. For details, see December 13-15, Denver.

January 24-27, International Microcomputers/Microprocessors 79/Japan, Harumi Exhibition Center, Tokyo. Contact ISCM, 222 W Adams St, Chicago IL 60606, (312) 263-4866.

January 30-February 1, Communication Networks and Exposition, Sheraton Park Hotel, Washington DC. Designed to bring together communication network users, consultants, vendors and regulatory officials so that issues can be discussed and analyzed. It is particularly aimed at executives and managers who purchase communication products and services. Contact The Conference Company, 60 Austin St, Newton MA 02160.

February 1-3, Microprocessor Programming Workshop with a Take-Home Microprocessor, Jefferson Plaza Building, Arlington VA. Sponsored by the IEEE, this 3 day workshop is intended for the practicing engineer, engineering manager and programmer. The course objective is to provide state of the art information in order to acquire an understanding of the place of microprocessors as replacements for wired logic and as controllers; to provide the capability of understanding the design of systems involving microprocessors; and the ability to program the Motorola M6800 microprocessor in machine language. All students will have their own microprocessor and laboratory equipment. Contact IEEE Service Center, 2145 Hoes Ln, Piscataway NJ 08854.

February 13-15, The National Office Exhibition and Conference, Harbour Castle Hilton Convention Center, Toronto Ontario. This 3 day exhibition will provide a showplace for approximately 100 exhibitors in the areas of word processing, office computers, office equipment and furniture. Contact Canadian Office magazine, 2 Bloor St W, Suite 2504, Toronto Ontario, CANADA M4W 3E2, (416) 967-6200.


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Micro-Ap
8939 San Ramon Road
Dublin, CA 94566

Circle 218 on inquiry card.
Attention: Robot Enthusiasts

The Robotics Newsletter is a monthly periodical for robot enthusiasts on both the hobby and professional level. It presents timely articles on micro-computers, batteries, motors, automata theory, sensory devices, manipulators, biophysical analogs, robot history, etc. Yearly subscriptions are $8. Contact the International Institute for Robotics, POB 615, Pelahatchie MS 39145.

Northern New England Computer Society

Albert Brunelli has written us that a new computer club has been formed "up here in the north woods." It is located in Berlin NH and is called the Northern New England Computer Society. They meet the second Thursday of each month at 7 PM at the New Hampshire Vocational Technical College, Milan Rd, Berlin. Their aim is to set up an area that is accessible to local people where they can learn about and use small computers. The membership fee is $10 per year. For more information, write to Albert Brunelli at POB 69, Berlin NH 03570.

Denver Amateur Computer Society

The Denver Amateur Computer Society now has permanent club quarters and office at 1380 S Santa Fe Dr, Denver CO 80223. The club meets the third Wednesday of every month at 7:30 PM. For further information, write to the society's president, Mike Dymtrasz, at the above address or call (303) 979-6441.

The Okaloosa Computer Hobbyist Club

We have been notified that the Okaloosa Computer Hobbyist Club has been formed in Ft Walton Beach FL. The meetings are held on the second and fourth Tuesday of each month and all interested persons and newcomers are welcome. For more details, write to Loretta R Gubko, P.O. Box 72, 32 Denton Blvd NW, Fort Walton Beach FL, (904) 242-5938.

Computers in Mental Health Newsletter

Micro-Psych is a newsletter for professionals interested in the use of computers in mental health. Each bimonthly edition contains reviews of current work in the field, a forum for the exchange of information, an ongoing bibliography, and news about pertinent hardware and software. Membership and a subscription to Micro-Psych costs $10 per year. For more information about this newsletter, contact Marc D Schwartz, MD, 26 Trumbull St, New Haven CT 06511.

Connecticut Computer Club Welcomes All Level Hobbyists

The Connecticut Computer Club, which is a few years old, consists of an informal group of software and hardware people who meet on a monthly basis to exchange ideas. Speakers and demonstrations are of general group interest. The club meets the first Thursday of each month at either the Suffield Library or The Computer Store of Windsor Locks. A newsletter is available to members at a yearly cost of $5. Contact Leo Taylor, 18 Ridge Ct W, W Haven CT 06516, (203) 933-3518.

Quad City Computer Club

We have heard from John E Greve, president of the Quad City Computer Club (QC3). The club, devoted to all phases of hobbyist computing, meets on the first Sunday of each month at 7 PM at the Rock Island Arsenal classroom #5, Rock Island IL. The dues are $6 per year, which includes a newsletter. For more information concerning this club, contact John E Greve, 4211 7th Av, Rock Island IL 61201.

Apple II Users Group in Portland OR

The Apple Portland Program Library Exchange, or APPLE for short, has been formed as a users group for owners of the Apple II. They are interested in exchanging programs and ideas with other clubs. Send a self-addressed stamped envelope for an application form to Ken Hoggatt, 9195 SW Elrose Ct, Tigard OR 97223.

Canadian PET Owners Start Users Group

The Vancouver PET Users Group recently held their second meeting. Attendees included 40 owners and 15 PETs. The club format includes a short presentation by a PET owner on programming, or PET hardware news from Commodore and other sources. This is followed by PET patter and program swapping. For more information about this club, write to Richard Leon, Vancouver PET Users Group, POB 35353, Station E, Vancouver British Columbia, CANADA.

TRS-80 Computing

A complimentary copy of TRS-80 Computing has been sent our way. This 32 page first edition is packed with TRS-80 news including articles by a TRS-80 designer, a Radio Shack repairman, and a couple of programmers; an article on how to install your own 16 K
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byte integrated circuits and save; a 10 page schematic, and considerably more. The price for 12 issues is $10 and is available from Computer Information Exchange Inc, POB 158, San Luis Rey CA 92068.

Chicago Area Computer Hobbyist Exchange Forms User Groups

In keeping with the club's philosophy of dedication to investigating the roles and uses of microcomputers and related small size computing devices in the hobbyist field, the Chicago Area Computer Hobbyist Exchange (CACHE) has recently announced the formation of user groups. According to the club's newsletter CACHE Register, the North Star, SOL and Digital Group user groups are active and going strong. The CP/M, H-11/LSI-11 and computer aided instruction user groups have formed but are not meeting regularly. There are other groups in the formative stages. CACHE members meet on the third Sunday of each month at 1 PM in the Northern Illinois Gas Building, Golf and Shermer Rds, Glenview IL. Contact Bill Precht, president, POB 52, S Holland IL 60473.

Attention Minneapolis/St Paul Apple II Users

We have been notified by Dan Buchler, 13516 Grand Av S, Burnsville MN 55337, that an Apple II users group has been formed in the Minneapolis and St Paul area. The purpose of the group is to promote the exchange of user developed programs and technical information among Apple II users. Help in documenting programs will be offered. Contact Dan Buchler for further information.

Newsletter for Users of Digital Group Equipment

BRIDGE (Bidirectional Reflections for the Illumination of Digital Group Enthusiasts) is an impressive newsletter devoted to helping fellow Digital Group owners over the voids. The cost of membership is $6, which entitles you to six issues of the newsletter. The most recent newsletter contains a couple of articles, items for sale, random bits of information of interest to Digital Group equipment owners and much more, including a letter from BYTE's Steve Ciarcia, an occasional contributor. If this newsletter is of interest to you, it can be obtained by writing to the Digital Group Independent Users Group, POB 316, Woodmere NY 11598.

Rockwell's AIM 65 Users Group

An AIM 65 users group is being formed for Rockwell's computer-on-a-board. A bimonthly newsletter will be available in January 1979 for $5 per year. Article contributions are welcome. For more information about this group, contact Don Clem, RR 2, Spencerville OH 43587.

*CP/M is a trademark of Digital Research
**Add $100 if CBASIC is also needed

Circle 328 on inquiry card.
Partitioned Data Sets

Figure 1: Information arrangement for a small partitioned data set.

If you have a floppy disk and are having trouble keeping track of where your programs and data are written on it, this simple file organization technique may provide the automated management of disk space you need.

A partitioned data set (PDS) is a file divided (or partitioned) into areas, each area containing data not related to data in other areas. For example, a system library might contain a source editor, assembler and linkage editor. Each of these programs could be stored in a separate partition in a partitioned data set. The partitioned areas in which these programs would be stored are called members of the data set, so the partitioned data set just described would contain three members, as in figure 1.

Designing the Partitioned Data Set

Four things are required for definition of a partitioned data set. First, a map for defining those areas on the disk that are in use (allocated). For this we create a track map that defines each track on the disk with one bit. If the bit is set to 1, the corresponding track is free. If the bit is set to 0, the track is in use. For a disk with 77 tracks, a 10 byte track map is sufficient. The position of each bit in the map defines the address of its associated track. The first bit in the map defines track 0, the second bit defines track 1, etc. The track map is referenced whenever a data set is allocated or scratched, so the smallest data set possible would be 1 track in length.

Second, we need a sector map to keep track of which sectors are in use and which are free. As in the track map, we assign 1 bit in the map to each sector. If our disk has 10 sectors per track, the sector map must be 770 bits in length, so we assign 97 bytes to it. As in the track map, the position of each bit defines the address of the associated sector. The sector map, table 1, is used when a member is created in or deleted from a data set.

Third, a control block for defining the name and location of the partitioned data sets is needed. These blocks can immediately follow the maps, and should contain space for the data set name, starting track address of the data set, length of directory in tracks, and the ending track address of the data set. Following this control block are similar

Table 1: Possible arrangement for the label record (1a) and data set control block (1b) for a partitioned data set.
control blocks for other data sets and unused (free) control blocks. A free control block is indicated by the name field being filled with binary 0s.

The maps and the control blocks can all fit on a single track. This track is called the volume table of contents (VTOC) and begins with the volume label, also known as the volume serial number (VSN). If we want a multitrack volume table of contents, we need to define how many tracks are in the table for use by the access method software. A byte for a count of the tracks in the volume itself should be included. If our system is to handle different formats and densities it would be wise to include the format information in the table of contents. The access method software could then read the count of the number of tracks on the disk and the number of sectors per track directly from the table and be able to handle several formats without modification.

In order to avoid wasting disk space, 16 byte logical records can be blocked 8 to a 128 byte sector. A single track volume table of contents blocked in this way could handle 136 partitioned data sets. The fourth item required for a partitioned data set is a directory for the members in the data set. The directory, table 2, begins at the first sector of the first track of the actual data storage area. The directory entries are 16 bytes long and packed 8 to a 128 byte sector. Each entry contains the name of the member, the starting and ending track and sector addresses of the member, the count of the number of sectors actually used by the member, and the data type of the member. The data type may be:

0 : Source data.
1 : Core image object data.
2 : Relocatable object data.

Both source and BASIC programs may be stored in a member of data type 0, while data type 2 is used as input to a relocating loader, linking loader or linkage editor. Data type 1 is used for storing nonrelocatable programs.

Now that the design of the file structure is complete, we can design software that will create, manipulate and delete members and data sets.

Table 2: Format for the directory entry information.

<table>
<thead>
<tr>
<th>Member name</th>
<th>Start of data area address for member</th>
<th>End of data area address for member</th>
<th>Number of logical records in use</th>
<th>Data type of member</th>
<th>Unused</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>6 bytes</td>
<td>2 bytes</td>
<td>2 bytes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 bytes</td>
<td>2 bytes</td>
<td>1 byte</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3 bytes</td>
<td></td>
</tr>
</tbody>
</table>

Figure 2: Disk initialization program.

Implementation

The first program we need is a disk initialization routine such as the one in figure 2. The initialization routine creates and empties the volume table of contents track and clears the data storage area by setting it to 0. The user is required to enter the volume serial number and the beginning and ending track numbers of the data storage area. The track and sector maps are created so that the bits corresponding to the data storage area are set to 1 (free space) and all other bits
Figure 3: The ALLOCATE routine, used to put a new file onto the disk and update all pointers to indicate that the file is present.
are set to 0 (space used). The volume label, a count of the tracks used by the volume table of contents (permanently set to 1) and the maps are then written on the first sector of the first track of the disk. All other sectors of the table of contents track are set to binary 0. Every sector of the data storage area is also set to 0. Initialization of the disk is now complete.

Once the disk has been initialized, we can allocate data sets on it by using the allocate routine. The allocate routine shown in figure 3 actually consists of two routines: one to allocate data sets, and one to allocate members in a data set. To allocate a data set, the user enters the volume serial number of the disk, the name of the data set to be allocated (six characters maximum), the number of sectors to be used for directory, and the number of tracks to be devoted to the data area. Note that the space used for the directory is included in the amount of space entered for the data area definition.

The allocator routine then reads the volume table of contents track and verifies that the volume serial number on the disk matches that entered by the operator and that the data set name to be used does not already exist. If neither test fails, the track map is scanned for contiguous free space equal to the amount requested by the user. If the free space is found, the necessary bits are reset to 0 in the track map. The data set control block is now built by moving the required data into an empty block in the table of contents. The sector map is also updated to reflect the sectors used by the directory and the updated volume table of contents is rewritten on the disk, completing the allocation of a data set.

To allocate a member, the user must provide the volume serial number of the disk as well as the name of the data set of which the member will be a part, the member's name (six characters maximum), member data type, and the number of sectors to allocate to the member. The allocator program again verifies that the proper disk is on line and that the data set exists. Obtaining the address of the partitioned data set's directory from the control block for the data set, the allocator verifies that a member with the same name as that being allocated does not already exist. If all is well, the sector map is scanned for contiguous free space in the data set's data storage area sufficient to satisfy the user's request. If space is available, an empty directory record is used to create a directory entry for the member. The sector map is then updated and the directory and table of contents are rewritten on the disk.

We now have a partitioned data set with...
In order to free space on the floppy disk, deletion programs are required. Scratching a data set would deallocate the space used by the members in the data storage area (recorded in the sector map) and clear the track map bits used for the overall space allocation for the data set. The data set control block is then filled with binary 0s, freeing all space previously allocated.

Scratching a member requires that the sector map be updated and the directory entry for that member be rewritten as binary 0s. The deletion programs should be written to be as forgiving as possible of operator errors. After the operator has finished giving the delete command, the program should echo the command and wait for operator verification. All this is needed in order to avoid accidentally destroying irreplaceable data.

Another useful program is the volume table of contents lister. The list program reads the data set control blocks from disk, formats and displays the information contained in them, and indicates how much space is allocated to each data set and how much free space remains. As an added feature, the lister could be made smart enough to use the data in the data set control blocks to find and display the contents of the member’s directory entries, thereby providing a powerful tool for controlling the data on the disk.

As with all good things, the free space on the disk will soon come to an end. The obvious solution is to delete a few members or data sets to make room for new things, but this has the disadvantage of destroying....
programs and data that may be important.

A better solution would be to place these programs into cheap archival storage in a format that simplifies their restoration onto the disk. Thus, the members or data sets to be saved would be written to magnetic tape by an unload program and written back on the disk later with a load program. The unload program reads the data set control block of the data set to be unloaded and writes it on tape. It then reads the directory entries for the members of the data set and writes the one selected to tape, followed by the data for the member from the data storage area. It continues to write directory entries followed by member data until the request entered by the user is completed.

The load program reads the data from the tape and if necessary allocates data sets and members before writing the data into them from the tape.

The partitioned data set file organization technique has been used successfully on many large systems and can be easily adapted for use by the hobbyist. In order to avoid a situation similar to that encountered with audio cassettes, standards should be formulated now so that disks can be interchanged from user to user.
Tic-Tac-Toe in BASIC

Tic-Tac-Toe is a game that has been turned into a computer program thousands of times. Although it is fun to play with a computer, the best a human opponent can hope for is a draw game. After a short time the player loses interest because he or she never has any chance of winning. My version plays a regular game except that there are a few logic errors which put the player on a more even level with the computer. There is a fighting chance against the now imperfect opponent. The program logic that scans the rows, columns and diagonals has been altered to produce counter-moves much like those of a person just learning the game. After playing dozens of games with the machine, if the player is lucky, the pattern of moves that fool the machine will emerge and allow the player to beat the machine every game. One such pattern is shown by the sample game of figure 1.

To change the program logic back to playing a perfect game every time, change the value of Z at line 1140 from 1 to 2. This hint should allow any good hacker to figure out how the program works internally. You can have fun playing the computer and showing your friends you are, indeed, smarter than the computer!
Listing 1: BASIC source code listing for Tic-Tac-Toe game.

100 REM "TA" === TIC-TAC-TOE WITH A TWIST
110 REM 02-05-77 WRITTEN BY MIKE STODDARD
120 REM
130 DIM K(I:3),L(I:9),A(I:12)
140 PRINT "(D) THE GAME OF TIC-TAC-TOE. THERE ARE A POSSIBLE GAMES"
150 PRINT "WHICH YOU CAN WIN. THE BOX SQUARES ARE NUMBERED."
160 PRINT "1 2 3 4 5 6 7 8 9"
170 FOR I=1 TO 3
180 FOR J=1 TO 3
190 LET K(I,J)=9
200 NEXT J
210 NEXT I
220 LET N=0
230 LET M=0
240 LET J=1
250 LET I=1
260 LET N1=0
270 LET N2=0
280 PRINT TAB(7);"A SYSTEM WITH SOCK!"
290 PRINT TAB(7);"OUR SPECIAL MOTOROLA MICROPROCESSOR EVALUATION KIT II"
300 PRINT TAB(7);"CHRISTMAS "PACKAGE" INCLUDES THE HARDWARE YOU NEED"
310 PRINT TAB(7);"TO EXPAND YOUR D2 KIT TO FULL SYSTEM CAPABILITIES!
320 PRINT TAB(7);"FULLY TESTED AND ASSEMBLED!
330 PRINT TAB(7);"SEND US YOUR CHECK OR MONEY ORDER NOW!
340 PRINT TAB(7);"WE CAN ALSO BILL TO YOUR MASTER CHARGE OR VISA"
350 PRINT TAB(7);"IF YOU INCLUDE THE NUMBER AND EXPIRATION DATE.
360 PRINT TAB(7);"ENCLOSE TOTAL FOR ENTIRE PACKAGE OR ANY TAXES (INCLUDE AN ADDITIONAL $5.00 FOR SHIPING"
370 PRINT TAB(7);"AND HANDLING). BE SURE TO INCLUDE YOUR NAME"
380 PRINT TAB(7);"ADDRESS AND PRINT CLEARLY. MAKING CHECKS"
390 PRINT TAB(7);"PAYABLE TO MOTOROLA INC.
400 PRINT TAB(7);"MALL TO:
410 PRINT TAB(7);"MOTOROLA MAIL ORDER SALES"
420 PRINT TAB(7);"P.O. BOX 27605, TEMPE, AZ 85282.
430 PRINT TAB(7);"A SYSTEM WITH SOCK!"
440 PRINT TAB(7);"MOTOROLA MICROPROCESSOR EVALUATION KIT II"
450 PRINT TAB(7);"IT INCLUDES:
460 PRINT TAB(7);"MEK6800AB ... $199.95"
470 PRINT TAB(7);"ACCESSORY BOARD FOR COMPLETE INTERFACE BETWEEN D2 KIT. ASCII"
480 PRINT TAB(7);"KEYBOARD AND VIDEO MONITOR OR TV SET. HAS CUSTOM ROM WITH"
490 PRINT TAB(7);"VIDEO DRIVER.
500 PRINT TAB(7);"SOFTWARE PROGRAMMABLE LINE AND CHARACTER FORMAT:
510 PRINT TAB(7);"16 X 32, 16 X 64, 24 X 80—UP TO 24 LINES BY 165 CHARACTERS.
520 PRINT TAB(7);"5 X 7 CHARACTER FORMAT WITH UPPER AND LOWER CASE.
530 PRINT TAB(7);"MEK6800D2 ... $235.00"
540 PRINT TAB(7);"THE EVER POPULAR D2 (IN KIT FORM ONLY) TO DEVELOP AND EVALUATE"
550 PRINT TAB(7);"M6800 MICROPROCESSORS.
560 PRINT TAB(7);"FREQUENCY SYNTHESIZER ... $395.00"
570 PRINT TAB(7);"MEMORY BOARD WITH 16K X 8 BYTES OF RAM.
580 PRINT TAB(7);"POWER SUPPLY ... $99.50"
590 PRINT TAB(7);"FULLY-REGULATED +12 VOLTS AT 1 AMP AND +5 VOLTS AT 6 AMPS..."
600 PRINT TAB(7);"CAPABLE OF POWERING COMPLETE SYSTEM WITH POSSIBLE EXPANSION.
610 PRINT TAB(7);"MOTOROLA MICROPROCESSOR EVALUATION KIT II"
620 PRINT TAB(7);"FREQUENCY SYNTHESIZER ... $395.00"
630 PRINT TAB(7);"MEMORY BOARD WITH 16K X 8 BYTES OF RAM.
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980 PRINT TAB(7);"FREQUENCY SYNTHESIZER ... $395.00"
990 PRINT TAB(7);"MEMORY BOARD WITH 16K X 8 BYTES OF RAM.
1000 PRINT TAB(7);"POWER SUPPLY ... $99.50"
1010 PRINT TAB(7);"FULLY-REGULATED +12 VOLTS AT 1 AMP AND +5 VOLTS AT 6 AMPS..."
1020 PRINT TAB(7);"CAPABLE OF POWERING COMPLETE SYSTEM WITH POSSIBLE EXPANSION."
Listing 7 continued:

2060 LET N4 = 0
2070 FOR I = J TO 10
2080 LET J = I
2090 LET N4 = N4 + K(I, I)
2100 IF N4 ≥ M GOTO 2230
2110 NEXT I
2120 LET K(I, I) = 0
2130 LET N4 = 0
2140 FOR I = 1 TO 10
2150 LET J = I
2160 LET N4 = N4 + K(I, J)
2170 IF N4 ≥ M GOTO 2230
2180 NEXT I
2190 IF K(I, J) = 5 GOTO 2210
2200 ON N1 GOTO 1370, 1590, 1790, 1220
2210 PRINT TAB(7), "THE GAME IS A DRAW."
2220 GOTO 2700
2230 IF M = J GOTO 2260
2240 IF K(I, J) >... ? GOTO 2500
2250 ON K2 GOTO 2290, 2310, 2330, 2350
2260 PRINT TAB(7), "CONGRATULATIONS. YOU WIN THIS GAME."
2270 GOTO 2700
2280 REM COEFFICIENT EVALUATION SUBROUTINE
2290 LET J = J - I
2300 LET J = 10
2310 LET J = J
2320 LET J = 1
2330 GOTO 2210
2340 LET J = J
2350 GOTO 2210
2360 LET J = J + 1
2370 GOTO 2211
2380 REM CONVERT 1-9 SUBSCRIPT TO I-J VALUE
2400 LET N4 = 0
2410 FOR I = 1 TO 10
2420 FOR J = 1 TO 10
2430 LET N4 = N4 + K(I, J)
2440 NEXT J
2450 NEXT I
2460 GOTO 2700
2470 LET K(I, J) = 1
2480 IF NZ GOTO 2500
2490 REM CONVERT 1-9 VALUE TO 1-J SUBSCRIPT
2500 IF NZC>1 GOTO 2550
2510 IF NZC<1 GOTO 2550
2520 GOTO 2700
2530 LET N4 = 0
2540 FOR I = 1 TO 10
2550 LET N4 = N4 + K(I, J)
2560 NEXT I
2570 PRINT TAB(7), "EVERYTHING YOU ALWAYS WANTED TO PLUG INTO YOUR PET, APPLE OR TRS-80."

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Hansford, John
603 N Hazelton Av
Wheaton IL 60187

Having been interested and active in computer programming for some 10 years, I have watched with great anticipation the advent of the personal computer. In my own hobby and professional programming, I have used a rather large number of languages and have discovered through many painful experiences and uncounted hours of debugging that, in general, regardless of the language being used, a modular top-down approach to developing new programs is by far the easiest to understand and use. Unfortunately, my first experiences with programming consisted of occasional use of a Teletype terminal on a timesharing BASIC system. I still use BASIC for some of my hobby programs, but I find that unless some skill in program organization is used, a BASIC program can very easily become a

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rat's nest of inserted problem bypasses and altogether impossible to read. I recently obtained a copy of a primer on Pascal in the hopes that it would provide some knowledge and insight into providing a proper means of improving program structure through language format and syntax rather than relying on my own experience in this area. I can now see why this language has become much more popular as a first language in many universities and I hope that it will continue to grow in popularity and wide usage.

At various times in the past I have tried my own hand at designing a source language which would provide a much more meaningful approach to program structure which must be at least as important as function. I have no new language to propose in the cause of this interest, having never tried to implement one of the languages I have designed, but I do have some comments which may be of interest to those who are also involved in the search for the "perfect language."

In various languages, to my knowledge including BASIC, Pascal and COBOL, there is at least one statement which tests a condition and will or will not perform a specified function depending on the outcome of the test. This is, of course, the IF statement in the languages mentioned above. ELSE we forget, these languages also contain a statement which allows the testing of a variable state and the optional performance of one of several alternative functions depending on the state encountered. In BASIC, this is the "ON . . . GOTO . . ." statement; in Pascal it is the "case . . . of . . ." statement, and in COBOL it is the "GO TO . . . DEPENDING ON . . ." statement. FORTRAN also has this capability in a limited way through the use of the numeric IF rather than the logical IF. In my humble opinion, Pascal's implementation of this feature is far more meaningful not only to program structure but also to understanding the condition which is actually being tested. Many times when this structure is used in BASIC or COBOL, it is the powerful feature which justifies the use of that "hairy" computation to adjust the conditions which are actually present to be an integer between 1 and 10. Pascal's implementation of this structure is still not perfect because it takes some extra effort in defining data types to assure that one of the alternatives will indeed be picked. Correct me if I'm wrong, but there is no explicit way to specify what should be done if none of the states for which there are alternatives is actually

Figure 1.

```
IF
  condition 1 statement 1
  condition 2 statement 2
  condition 3 statement 3
  .
  condition n statement n
END
ELSE statement
```
found. I believe it would also be somewhat tricky to use this single Pascal statement to perform one function if the variable being tested is less than 50, to perform another if the variable equals 50, or to perform a third if the value is greater than 50, for example.

These are obviously closely related conditions and would ideally be resolved with a simple statement structure. Note that these types of tests are possible in most any language: however, my suggestion is that there should be an alternative to this sometimes confusing structure.

Rather than having one statement to test a single condition and another to resolve multiple conditions, why not make the single condition test a simple subset of the multiple condition test? A loosely defined statement structure which would satisfy this requirement is shown in figure 1. As this statement is parsed, the statement becomes a multiple condition test when it contains multiple conditions. When additional conditions are encountered, each is concatenated to the first condition to form a new conditional expression which is then evaluated to determine if the statement associated with the new condition should be executed or not. The one restriction I would like to see on this type of a structure would entail not evaluating the original condition if statement 1 is omitted. This means that only the concatenated expressions which are formed will actually be evaluated. Simple examples of possible forms of this type of a statement are shown in figure 2.

I believe that this statement structure provides an excellent aid to properly organizing program structure. It has the capability of directly relating associated states in an easy to understand manner and provides the flexibility which a multiple condition test should have, without having to go through any complex manipulations to resolve the conditions present to any particular restrictive form.

I would welcome any and all comments on this proposal and am always interested in finding more about the "perfect language" if you have any suggestions.

Perhaps a reader with language design experience would care to comment on the various examples and suggestions proposed. Readers should note that none of the examples of figure 2 follow the prototype of figure 1 completely. But the examples of figure 2 might provide interesting variations on the multiple condition suggestion if they prove unambiguous to a language translator or interpreter. . . .CH1

---

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For those who have not yet stepped up to Pascal, the programs above also available in BASIC
Pascal Critique and a Comment

I have just finished reading your August 1978 issue and would like to comment. I am more than a little disappointed with the volume of coverage given to Pascal. Whatever the relative merits of the language that amount of discussion isn't merited in my opinion. There currently is no affordable implementation of the language available to the typical computer enthusiast. If and when Pascal is available I believe it will have a very rough battle trying to compete with both the pricing and heavy usage that BASIC enjoys today.

Another problem I think you have failed to address is the effect of the huge investment in time and money many have made in BASIC. Just what is to become of that? Conversion? An unlikely prospect given the historical example of the COBOL and PL/I controversy. Use both languages? Again an unlikely prospect. Most people have all they can handle without the demands a second language would require.

It should also be pointed out that Pascal has little or no following outside the academic community. It wouldn't be the first time that a language enjoying a great deal of admiration at the academic level has failed to gain acceptance as a viable tool in the real world of data processing. Languages are used and live only on the basis of perceived usefulness, the availability of experienced practitioners, and widespread implementation of the language. Pascal now has none of those attributes.

In my opinion the number of users of any language speak many silent volumes that by weight of numbers signal acceptance of a language more than any theoretical proposals or arguments about the relative advantages of competitive languages.

But there is an affordable implementation of Pascal — the UCSD system is available separately, or bundled with various manufacturers' products. As a means of learning a new language, conversion of one or two programs as tutorial experiments is just fine. Pascal should only be thought of as an avenue to more effective creation of new programs.

As for "no following outside the academic..."
community,” Pascal has a very strong following as witnessed by the representatives of both industry and academia present at the UCSD Pascal Workshop last summer. BASIC was once the only logical and effective choice of languages to use.

The virtue of Pascal and similar languages is the fact that the very expression of the program is so much closer to the way people think. I, for example, think in terms of “I want to do thus and so”; in Pascal, I might have to map out in advance exactly what it is he will ask the machine to do.

At the root of the matter is the consideration that there is no clean distinction between “implementing a program” and simply “invoking a system utility.” Suppose, for example, we wish to check on the value of some variable, for example $J$, during an APL terminal session. We simply type:

$$J$$

Now suppose that the value of $J$ is lower than we expected, so that we become interested in the first $J$ elements of the array $A$. We type:

$$A[1..J]$$

Continuing Comments on APL

John Howland’s “Comments on APL’s Characteristics” in the May 1978 BYTE Languages Forum, page 143, are for the most part well thought out. However, it seems to me that he is missing something when he states that an APL programmer who composes programs on line is “similar to the person who opens his mouth and begins to speak before engaging his brain.” The whole point of having an interactive language facility is based on the fact that the programmer does not always want to reference a procedure with the name thusandso. In BASIC I would have to reference it in the program with a number artificially created for that purpose. I might say GOSUB 10000, for example, when I really mean to call and execute a thusandso procedure. Pascal can be used as any other programming language — for the underlying computers are identical. It is a matter of making the expression of a program easier for the user.

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But now perhaps we realize that J is actually the number of pairs of quantities in A and so in order to examine the set consisting of the first element of each pair we type:

\[ A[-1+2:X 1 J] \]

I could go on, but I think the point is clear: at what level of complexity have we stopped merely using the facilities of the environment and started writing a program?

My own view is that the above distinction is immaterial and that what matters is simply that the environment be structured to maximize the programmer's capability to accomplish the job at hand expediently. When the job at hand is large and complicated, there is no question but that at present hardware costs the most expedient recourse involves writing out the bulk of what is to be typed in beforehand. Likewise when the job at hand is trivial and transparent (eg: inspecting \( A[-1 J] \)), it is undeniably the case that writing it down before typing it in is a waste of time. In between these two extremes, things are not so clear, and the point at which paper and pencil become necessary will depend both on the individual programmer involved and on the system. However, what is clear is that the more complex the programmer finds himself able to get, on line, while still maintaining cogency of thought, the more productive he will be.

Mr Howland justly defends APL's right to left order of evaluation from those who would make it left to right: \( 3 ÷ 6 \) equals 2 is not a pleasant prospect. However, a valuable property for any language/environment to possess is one which allows short, transparent programs to be entered quickly and easily, without any need for pencil and paper in the process. My suggestion to the APL terminal manufacturers, if they haven't done so already, is to implement an option whereby each line could be entered from right to left (in much the way one frequently finds oneself writing out lines of APL on paper, that is, starting at the righthand edge and working leftwards). In this way, the objective of simplified online program creation could be achieved at no cost in the way of incompatibility with existing APL processing precedence.

Reacting just slightly to the last paragraph of your letter, a question comes to mind: is it the terminal manufacturer's responsibility or the APL interpreter-writer's responsibility to make the input sequence run from right to left? With a fast enough terminal, it is possible to rewrite the last
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In response to the discussions of high level languages I have been following in BYTE, I would like to call your attention to an existing language as implemented on the Hewlett-Packard 9825A.

HPL, as Hewlett-Packard calls it, is implemented on the basic machine similarly to BASIC. Extensions are available by stages in read only memory. String capabilities are enhanced by a string ROM. IO handling by the general IO ROM is enhanced to be similar to FORTRAN. The advanced programming ROM extends the capabilities to cover, in large part, the characteristics of PIAO ALGOL as described in The Design and Analysis of Computer Algorithms by Aho, Hopcroft and Ullman (Addison Wesley). A couple of features should be noted. An assignment operator is used, allowing the equal sign to be only a relational operator. While the list of variable names is limited to single letters, the flexibility of substrings, local variables in subprograms and functions, and r variables provide for few problems in practical use.

I have been working with this system for a year and a half developing and implementing programs for an agricultural consulting firm. While the firmware, fully implemented, is probably close to 70 K, this is an excellent example of what can be done on a small system, and might just be a good system to emulate.
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A Proposal for a Kitchen Inventory System, or Don’t Byte the Wand That Feeds You

A practical and natural application for your home computer is an inventory system for the kitchen. Such a system would relieve humans of the details involved in making out a grocery list.

One convenient way of keeping track of the various items in the pantry is to use the information that is now provided on most food packages specifically for that purpose, namely, the Universal Product Code, or UPC. This is, of course, put there for use by food stores, but there is no reason that the UPC cannot be used in the home.

The Universal Product Code appears on a product label as a patch containing bar codes, with a line of human readable numbers underneath. This distinctive design has now become familiar to most North American shoppers. Information contained in the bar codes can be read by an optical sensing device connected to a computer.

At present many computer experimenters are equipping their computers with an optical sensing device, a bar code reader that has a scanning wand, for the purpose of scanning the new machine readable software which uses similar bar codes. A good example of such software is the PAPERBYTE™ series of books which BYTE Publications produces. It is probable that the same scanning wand used for reading the software may be used to read the Universal Product Code. The scanning wand provides a quick and easy method to identify a given item without keystroking any information into the computer. It will, unfortunately, be necessary to do some keystroking to set up the system. One minimal implementation of an inventory system might be set up in the following manner. For each grocery item in stock, a data base would exist containing:

- a representation of the Universal Product Code for a given item,
- a human language description of the product including brand name, generic name, and size or quantity,
- the minimum quantity that should be kept on hand,
- optional information on the item’s shelf life,
- any other information which is deemed useful (for example, which members of a household like a particular item).

As the supply of an item becomes depleted, the container is thrown out. Immediately before disposing of the container, though, the UPC bars are scanned. The computer stores this code in a table of
items which are depleted and should be restocked. Prior to setting off on a shopping trip, the user requests a display (preferably on a hard copy device) of depleted products. The computer uses the depleted products table to reference the master data base, and retrieves the human language description of the product from the master data base and displays it for the user, along with other information. If the display is on a hard copy device, the user simply tears off the paper and uses it as a grocery list.

Probably the best way to establish and maintain the data base is with the use of an interactive program. The user would build the data base from scratch by starting with those items on hand at the time. For each item, the UPC bar codes are scanned, then the user types in the other information about the item. (Note that it is not necessary for the numeric product code to be keystroked by the user.) After the initial data is stored, the interactive program may be executed to update the file with information for new or different products. It is not necessary to start with a huge data base containing data for every possible product. Each household would keep information tailored specifically to its needs in its data base.

The size of the data base is dependent on the number of different products a given household buys. It should be noted that each brand of a given generic item has its own code. The data base may be kept small if a single brand of a given item is used consistently. The procedure of reading the UPC bar codes just before consigning the container to the garbage follows one of the cardinal rules of computer use, which is: *garbage in — garbage out.*

Special arrangements would still be necessary to handle those products not marked with the UPC in many stores, such as fresh meat and local produce. It might be possible, with knowledge of the encoding method of the UPC, to make a custom UPC bar code symbol by hand. This could be mounted permanently near the garbage can scanning station and scanned instead of a package symbol. The computer could then at least note that the supply of a non-encoded item was depleted and call attention to the fact.

An ingenious tinkerer could no doubt find many ways to improve the system. For example, some means to indicate exactly which nonencoded item is depleted might be devised. And it might prove useful to scan a package as it is bought, to verify that it is back in stock. Also, the addition of a modem for telephone communication gives rise to many possibilities.

A computer equipped with a modem could, with the proper programming, call a computer equipped food store and automatically order the necessary grocery items. And given the proper programming both in the home and at the store, it could dial up several different stores, compare prices and order from the store which provides the lowest price for the entire list. With electronic transfer of funds, the computer could even automatically pay the grocery bill.

Automating the kitchen inventory should give people the time to develop new recipes or new computer applications.
He did not want his optional entertainment chip tampered with; his films, recordings, reading and fantasy trips had all been carefully selected, carefully tested over the years.

About the Author

Lawrence F Willard has been a journalist and free lance writer for over 30 years, contributing to many magazines, including New Hampshire based Yankee Magazine. A ham radio operator, Larry teaches journalism and media courses at Manchester Community College in Manchester CT.

Jonathon Witherspoon Twombly floated up out of a warm and comfortable world of drifting, unconnected images to begin, unfortunately, a new day. He stared at the cream colored ceiling, as he always did, to read the wedge of light that fanned from the top of the window shade to intersect a discolored area of the ceiling in a fairly significant manner. Nine o’clock, he guessed, disdaining for three and a half seconds the absolute accuracy of his Minnie on the bedside table. He rolled over and looked at it, stubbornly translating 24 hour time to his own archaic measure. His guess was a mere four minutes and ten seconds slow. Pretty close, he noted contentedly.

The mini-mini-micro-processor, his own personal computer link to the vast and complex world of 1997, winked at him with a softly glowing numeral 3. Not much larger than a deck of playing cards and half as thick, Minnie rested upright in her umbilical slot, absorbing power for her batteries and sharing her thoughts with the house computer in its basement hideaway. A rather old microprocessor, Mike ran the house, but Minnie was boss as long she was plugged into the table, or as long she was on Twombly’s person and not more than a mile distant from the house. Beyond that range she could integrate with Mike up to a distance of 40 miles using the high power car facilities, and beyond the 40 mile radius she could use the worldwide network of relay stations. But that cost money and was rarely necessary. Jonathon Twombly did not travel very much or very far.

At the moment he was staring at the glowing figure 3 in disbelief. Three messages for him during the night? How unusual! Twombly was a nobody; no family, no friends, no job. He didn’t have to work, and so never would be allowed to. He lived on the regular income from his trust fund, and, with Minnie’s help, he kept his outgo exactly equal to his income. It was a good life.

He removed Minnie from her niche and keyed in a command. The four foot square screen built into the wall at the foot of his bed lit up and the readout began:

MSG 1 BELLOGRAM 7.6.97 2207 66234621 BP P12 TWOMBLY, JONATHON W 779 28 88980 BMA
YOU ARE HEREBY CITED BY TRAFFIC CONTROL OFFICER 229 BOSTON CITY POLICE FOR MOVING TRAFFIC VIOLATION 7.6.97 1201 HOURS PL 2395 SEC. 8. B. SECTOR QUADRANT 9 FINE 25 DOLLARS REMIT WITHIN 24 HOURS TO AVOID ARREST PC JOHN KELLEY.

Twombly swore mildly (he was not an aggressive man). He’d had the car on manual five minutes during the entire day and he’d managed to get a ticket. He might as well pay now and get it over with. He didn’t even bother to call up the picture the cops had surely filed. He didn’t want to see himself on the screen making an ass of himself. Payment of the fine would wipe the picture out of the police computer banks. He punched up his bank balance, confining it to Minnie’s small screen. $207.81. Even with seven cents added as interest during the night, it wasn’t a healthy balance. He swore again, mildly, and punched in the command, the amount and the police computer address, checked it on the screen and punched the execute button. $182.66. The city had $25; the bank had its 15 cent service charge. Twombly called up the second message:
MSG 2 VIDEOPHONE CALL 0231 7.7.97
CENTRAL HOTEL RM 63
HI TWOMB OLD CHAP. REMEMBER ME?
PUDDY, ROOMY, WESTERN U? IN TOWN
FEW HOURS. HOW ABOUT A DRINK? NOW.
LEAVING SUNUP. 766 26 0589 CHEERS.

Twombly shuddered, wiped the screen clear. He had set Minnie to store night calls, not wake him up; he wasn’t sorry. He called up the last message:

MSG 3 BELLOGRAM 7.7.97 0800 66091532
FBCC BOSSOFF TWOMBLY, JONATHON W
779 28 88980 BMA
YOU ARE HEREBY REMINDED
APPOINTMENT THIS OFFICE ANNUAL
CHECKUP AND FIVE YEAR
REPROGRAMMING 1400 HOURS THIS DATE.
PREPARE FOR ROUTINE PHYSICAL,
PSYCHOLOGICAL TESTS TO DETERMINE
AGING FACTOR. ALL NEW PROGRAM CHIPS
TO BE INSTALLED, INCLUDING OPTIONAL.
YOU MAY RETAIN OR CHANGE OPTIONAL.
NOTE: WHEN THE HELL ARE YOU GOING
TO LET US REPLACE YOUR ANTIQUATED
MINI FOR NEW ATOM POWERED MODEL?
P. T. HARRIS BUCHIEF.

Twombly wiped the screen. Of course he hadn’t forgotten. Minnie had already placed an order for a car. Good old Minnie. Like hell they would replace her. Not yet. He sat for a moment, thinking. They’d find him five years older, reflexes a bit slower. New programming would compensate. Obstacle detection devices would take over a little sooner when he drove on manual, putting him a little less in control. His heart would be monitored more carefully and his med­­save unit would probably get newer, more powerful drugs. Minnie would probably calm him down a little quicker when he got overexcited. Did he want his optional entertainment chip tampered with? No. His films, his recordings, his reading, his fantasy trips had all been carefully selected, carefully tested over many years. They would do without further change.

Twombly got up, dressed (he wanted no help from the waldos, those mechanical servants that Mike controlled), and dropped
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- LSI 11 - $890.00
- 6800 - $995.00

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Minnie into his inside jacket pocket from which nobody but he could remove it without calling out the police emergency vehicles and perhaps the National Guard; anyway, nobody had ever tried it. He went into his small but luxurious dining room to eat the late breakfast Minnie had summoned for him. He was served by one of his two household waldos, which glided across the carpet on a cushion of air, delicately bearing a plate of scrambled eggs in hands that could bend a steel I beam into a pretzel.

Mike operated the waldos, using their sensory substitutes for eyes, ears and sense of touch. Twombly had programmed Mike to speak through the waldos’ vocoder systems in an almost human male voice, and he had also fixed it so that when Minnie wanted to speak to him verbally through Mike, the waldos underwent a startling change of sex, answering in suitable feminine tones. She spoke to him now above the plate of scrambled eggs.

“I have ordered you a car, a Whinger Electric, to be here at one o’clock. Very few of the agencies still have those in their inventory. They are, as you know, obsolete. Next year we will have to pay the antique car premium to get one.”

“I know, I know; we’ll worry about that next year.” Twombly ate his eggs, retired to his study and programmed the next lesson in his study course, “Late 19th Century and Early Twentieth Century External Bathroom Architecture in Rural Areas.” Fifteen minutes before the hour of one o’clock he was standing on the sidewalk in front of his townhouse awaiting the Whinger Electric. He was not alone. Standing a few feet away from him was the occupant of the neighboring townhouse, a Professor John Carmody, who taught English to first year students at Radcliffe. Twombly wondered whether he should activate his nonintercourse signal, but Minnie’s low buzz indicated that the good professor had activated his own, thus solving the problem. It was, of course, the grossest kind of social blunder to speak to or take any notice of a person radiating a nonintercourse signal.

Just then the signal stopped, and before Twombly could activate his own signal, the professor spoke to him.

“Since your signal is off, sir, may I be permitted conversation with you?”

It was now too late to emit a nonintercourse signal, and the grossest kind of social impropriety not to answer.

“My dear Professor Carmody, you may indeed converse with me,” said Twombly.

“Nice day, isn’t it?”

“Yes, I perceive you are waiting for a car?”
"Indeed, yes. I am headed into the center of the city, to government sector. Do you wish to share my car?"

"No, no, my dear Mr Twombly; my own is on the way. Would you be interested in a small wager, say five dollars, as to which vehicle arrives first?"

"That would be most sporting," agreed Twombly. "Shall we say ten dollars?"

"Done," said Professor Carmody.

Although neither could now erect the nonintercourse barrier, by mutual unspoken agreement nothing more was said. At exactly one o’clock both vehicles came into view, arriving from opposite directions. Twombly’s arrived a fraction of a second before the professor’s. The professor nodded in token of defeat, and entered his car. Twombly’s bank balance would shortly grow by ten dollars. He felt very good about that. Entering the two seater electric, he took Minnie from his inside jacket pocket and inserted it in the slot in the dashboard. It was now his car, for a daily rental fee, until he removed Minnie and gave the car a signal to return to its depot. He put the car on automatic and keyed in the destination. He could not get a traffic ticket as long as the car was under automatic control by the city’s own traffic computer which directed the symbiotic duo of Minnie and the car’s computer.

Twombly leaned back, completely relaxed in the knowledge that he was in the safest environment ever known to mankind. No matter what difficulties there were, through rain, fog, sleet or snow the car would transport him without danger. If he had a heart attack, his medisave implant would go into action, administering adrenalin, electric shock, or whatever else was needed for the few minutes it would take for help to arrive. Minnie would work through the car computer and signal system to coordinate the meeting of the car with the nearest mobile medical unit, which would be receiving a flow of medical data and electrocardiograms. It was exceedingly difficult to die in an automobile, or on the street for that matter. Minnies could work directly into repeaters mounted on telephone poles no more than a mile apart throughout the entire city.

At government center the car parked itself to wait until Twombly’s return, since he had not given it instructions to return to the depot. He took Minnie out of the dashboard slot and returned it to his inside jacket pocket, stepped out of the car onto a moving walkway, and was carried into the building that housed the Boston office of the Federal Bureau of Computer Control. He took the elevator to the twelfth floor.
Office of Programming and Adjustment, where he underwent a battery of tests which proved that he was five years older. His Minnie was sent to one of many laboratories where highly skilled technicians made new program chips and inserted the chips in the Minnie to replace the ones which had served Twombly well for five years. It was late afternoon when Twombly left; an hour after that, one of the technicians approached the lab chief with an almost microscopic program chip in the palm of his hand.

“We have a condition red, I think,” he told the chief. “This is the alternate program entertainment chip from Twombly’s Minnie.”

“Carson,” said the chief, “that simply cannot be. He couldn’t get out of the building without a full complement of chips; the master computer wouldn’t let him through the door.”

Carson, his face almost as red as the little dot on the chip which meant alternate program, said: “He had a full complement of chips. I got the wrong one in. He got an experimental chip I was designing for my wife’s Minnie.”

“What kind of an experimental chip?” asked the chief in tones that made Carson’s flesh creep.

“You might call it a babysitting chip,” said the technician, “although it doesn’t just sit. I can tell you that we’re in a great deal of trouble if he activates that chip. We have to prevent that.”

“Condition red,” sighed the chief. “We have to key into his Minnie by way of the house computer, but we’ll have to get authorization from Washington. I’ll notify Harris; it’s his problem. He won’t like it much.”

“I don’t think we have time. He’ll most likely activate the entertainment chip after he finishes dinner; Twombly is predictable.”

“We have to take time. After that J E Lewyt scandal, where the untouchability of our beloved director was found wanting, we’ve been under very rigid orders about invading the privacy of private computers. We’ve got to get authorization.”

They got it after a three hour delay, but as Carson feared, it was too late. When the special code got them access to the Twombly house computer, it reported that Twombly had activated the alternate program entertainment chip. The chief sighed and requested a complete readout from the time of activation.

CHIP ACTIVATED 2030 HOURS. SEQUENCE COMPLETED: UNDRESSING, BATHING, DRYING, POWDERING, DIAPERING. AS INSTRUCTED BABY HAS BEEN PUT TO BED
"We can do without the burping," yelled the chief. "Carson, override the program at once; switch off the alternate program. My God, I think we have a law suit on our hands. You and I will end up in the coal mines."

"Program is off, chief. I'll see if I can get an informal but detailed report from his Minnie... it's coming now."

Chief of Laboratory Q, George Justine, had chewed the nails down to the quick on one hand and had started on the other when Carson leaned back in his chair and actually smiled.

"Twombly started to panic when the waldos grabbed him and started to undress him, but calmed down and gave in when he couldn't stop them. He seemed to be actually enjoying the bath, and when he was put to bed with the warm bottle he slurped it down and actually cooed. He is now in a deep, peaceful sleep, and his Minnie reports that his blood pressure is normal for the first time in months."

"Well, we're not off the hook yet, but it looks better."

"Chief, we'll call him in tomorrow and explain the mistake, and apologize. We'll give him back his entertainment chip and I'll take back the babysitter chip."

"I doubt it. I mean, we can call him in, but something tells me he isn't going to give up that chip. It fits in too well with his psychological profile. We'll have to give it to him in addition to the entertainment chip. We'll gain one thing; I think we can get him to take the newer model Minnie, because the one he has doesn't have room for any more alternate programs. If he wants to play baby, he'll have to exchange Minnies, and I think he will."

"I hate to lose that babysitter chip; I put a lot of work in on that."

"Carson, that's going to be the least of your worries. We're going to have to fill out lots of reports... you are. There'll be lots of investigations and an awful lot of flack. There is one possible ray of light, there may be other people like Twombly, and this may prove to be some kind of legitimate therapy. I don't know. That's for the psychologists to decide. Right now we have to get ready for the worst, charges of invasion of Twombly's privacy. We panicked. We went to the top to get authorization to enter the computer of a private citizen, citing clear and present danger. What did we achieve? We stopped a man from getting burped."
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**Commander in Chief**

**A Game for the TI-58 Programmable Calculator**

Larry Kollar
Room 225 W Wadsworth Hall
Michigan Technological University
Houghton MI 49931

Commander in Chief is a TI-58 snowball war game for one player (see listing 1). After entering the program, press E. This clears the memory and initializes the random number generator (program 15 in the library module). You are now ready to play. Enter the number of snowballs you want up to 100 and push A. If you try to enter more than 100 snowballs, the program will place only 100 snowballs in your register. No iceballs allowed.

After a few seconds, the calculator will come back with a 1 or a flashing 1. If the display flashes, you are at war. Next, you estimate how many snowballs the enemy has and push B. The display will flash how many snowballs the enemy actually has. Following this, it will display a 1, 0 or -1 and then the year number; or the display will flash 9,999,999,99. If this occurs, there has been a holocaust and the enemy is rendered inoperative. If there is no holocaust, the 1, 0 or -1 tells you whether you have won, achieved a standoff, or lost; then the year number is displayed. You and your enemy have lost half of your snowballs and each of you will add more on the next year.

If there is no war at all during the year, you have the option of declaring war. The procedure is the same as that in which the enemy has declared war. If you can make it through ten years, you win the Snobel Peace Prize.

**ACKNOWLEDGEMENTS**


Thanks to David Nahakian for helping me with some of the program sequences.
## Sample Game

<table>
<thead>
<tr>
<th>Year</th>
<th>Your Total Snowballs</th>
<th>Total Enemy Snowballs (not seen)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>68</td>
</tr>
<tr>
<td>2</td>
<td>180</td>
<td>127</td>
</tr>
<tr>
<td>3</td>
<td>260</td>
<td>209</td>
</tr>
</tbody>
</table>

(Enemy declares war. Player estimates 191 snowballs, an error of 18. This is multiplied by the actual enemy snowballs and the number of his snowballs. The resulting holocaust factor is 978,120. The holocaust factor needed to cause a holocaust is 1,500,000. There has been no holocaust, so each power loses half his/her snowballs, discarding fractions. Player wins.)

<table>
<thead>
<tr>
<th>Year</th>
<th>Your Total Snowballs</th>
<th>Total Enemy Snowballs (not seen)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>130</td>
<td>104</td>
</tr>
<tr>
<td>5</td>
<td>230</td>
<td>197</td>
</tr>
<tr>
<td>6</td>
<td>330</td>
<td>224</td>
</tr>
</tbody>
</table>

(Player declares war and estimates 251 enemy snowballs, an error of 27. The holocaust factor is 1,985,840. There has been a holocaust; and both sides are blitzed.)

### Listing 1: Commander in Chief, a game for the Texas Instruments TI-58 programmable calculator.

Note that some of the operations of this TI calculator series allow multikey entries into one location. This is indicated by an asterisk within the key.

### Loc. | Keys | Commentary
--- | --- | ---
000 | *Lbl E | Random number generator.
006 | *Pgm 15 *E* R/S *Lbl A | 100 is maximum number of snowballs added is one turn.
012 | \(\times\) t 1 0 0 \(\times\) t 1 | Lower limit
018 | \(\times\) t *Lbl SUM 00 | Upper limit
024 | 1 STO 10 | Add enemy snowballs
027 | 1 0 1 STO 11 | 0
032 | *Pgm 15 C *Int SUM 13 | 1
038 | 1 3 STO 11 | 0
042 | 15 C STO 20 | 0
046 | 9 \(\times\) t RCL 20 \(\times\) t | War ?
051 | \(\times\) *Lbl + 1 SUM 21 | 1
057 | RCL 21 R/S *Lbl B | 1
063 | RCL 13 *Pause = | \(\lfloor x \rfloor\)
068 | i CE X RCL 00 X | Holocaust factor
077 | STO 15 | RCL 13
079 | 1 5 0 0 0 0 | Maximum holocaust factor
086 | \(\times\) t RCL 15 \(\times\) t Inx RCL | 0
092 | 13 2 = | *Int STO
098 | 13 RCL 0 \(\div\) 2 = | 1
104 | *Int STO 0 \(\div\) RCL 13 | 1
110 | – | 1
111 | *Op 10 | Signum function (Who won ?)
113 | *Pause Pause RCL 21 GTO + | 1
119 | *Lbl \(\times\) CLR \(\div\) = RCL | Flash year number
127 | *Lbl Lnx CLR 1/x *CM’s R/S | You are rendered inoperative!
It really is a necessary part of your knowledge, even if you're never going to write FORTRAN programs.

The average small system user will not be able to use FORTRAN as a programming language for his or her system. Some small systems have BASIC, and there is at least one FORTRAN system for the 8080 (available from Microsoft), but FORTRAN is still chiefly a language for large computers (including minicomputers and mid-size computers). Nevertheless, there are many situations in which a knowledge of FORTRAN is important even to the small system user. The most important of these is in the description of algorithms. It is of no use to describe an algorithm in, say, INTEL 8080 assembly language, since this would not make sense to users of Motorola and other microcomputers; so algorithms are very often described either in FORTRAN, or in some other algebraic language. FORTRAN, though, seems to be the one that is used most often for this purpose, since more people know FORTRAN than any other algebraic language.

There are hundreds of books on FORTRAN today, all of which are written for the large system user who is, presumably, actually going to use FORTRAN to solve problems. It is very rare that one finds a description of FORTRAN written for those who merely need to understand algorithms written in FORTRAN, but who are going to rewrite those algorithms in some other language themselves. The present article is written to fill this need.

The basic function of an algebraic language, of course, is to allow one to write algebraic expressions directly. Given a formula like

$$ k = \frac{ij-i+j}{n} $$

one has to write, in assembly language, something like “load i; multiply by j; subtract i; add j; divide by n; store in k” in order to calculate the new value of k. On most small systems, the job is even harder than this. We have to call subroutines for multiplication and division, and in an 8080 based system, even addition and subtraction of quantities in memory cannot be done directly: the right addresses have to be loaded into H and L first. However, when we are describing an algorithm, rather than writing a program, the formula above is what interests us, and we would like to write it directly. In FORTRAN, we would write

$$ K = \frac{(i^*j-1+i^*j)}{N} $$

There are several differences between the FORTRAN version and the original formula. Some of them are due to the fact that we have to be able to key the FORTRAN formula into a system on a terminal or a keypunch. For instance, we have to use upper case letters instead of lower case and we have to use the slash (/) to mean “divide.” The parentheses are necessary because, if we did not use them, that is, if we wrote

$$ K = i^*j-1+i^*j/N $$

the formula we would be expressing would actually be

$$ k = ij-i+j $$

since division takes precedence over addition.
The last difference between the formula and its FORTRAN version is in the use of the asterisk (*). This is necessary whenever we have a multiplication, since \( IJ \), just as in assembly languages, would be the name of a single variable. In FORTRAN, the name of a variable must start with a letter, can contain only letters and digits (although some versions of FORTRAN allow a few extra characters, most do not), and has a maximum length which depends on the system being used. Typical maximum lengths for identifiers are eight characters (IBM 360 and 370) and six characters (UNIVAC 1100 series, DECsystem 10).

In addition to the use of formulas of this kind, FORTRAN involves a number of other statements which express commonly encountered sequences of instructions. Among these are:

1. **GO TO**. Where the 8080 assembly language user writes JMP K, meaning “Jump to K,” and the 6800 user writes BRA K, meaning “Branch to K,” the FORTRAN user writes GO TO 15, meaning “Go to statement number 15.” Statements in FORTRAN have numbers rather than names, and the numbers have nothing to do with addresses in the machine; they can be assigned arbitrarily and do not even have to be in sequence (as they do in BASIC).

2. **IF**. The keypunches used by many large system users do not have the characters \(<\), \(\leq\), \(\geq\), \(>\), or \(\neq\) (although they do have \(=\)) and FORTRAN therefore uses .LT. (less than), .GT. (greater than), .LE. (less than or equal), .GE. (greater than or equal), and .NE. (unequal). Thus “If A is less than B, then go to statement number 15” would be written in FORTRAN as

   \[
   \text{IF (A.LT.B) GO TO 15}
   \]

   FORTRAN is distinguished from BASIC (and ALGOL, PL/I, and various other algebraic languages) by requiring the parentheses after the keyword IF, and also by not making use of the word THEN. FORTRAN also uses .EQ. (equal) in comparing, and not the character \(=\), which is reserved for assignment statements involving formulas (such as in \( K = (1*J-I+J)/N \), discussed above).

3. **STOP**. This signals the end of an algorithm, although a large system will not actually stop at this statement, but will go on to do the next job (assuming that there are more jobs waiting to be done).

4. **END**. This is simply the last statement in a program and has nothing to do with stopping, which can happen at any time. That is, we can have several STOP statements in a program, but only one END statement.

5. **READ**. A READ statement in FORTRAN is largely self-explanatory; thus READ (5, 91) N, A, B reads in three quantities and calls them N, A, and B. The 5 in this statement is a FORTRAN convention: the standard input medium (as opposed to any special tapes or disk files which might be used) is referred to as unit number 5. The 91 is a reference to a FORMAT statement which describes, in this case, in what format N, A, and B are going to be given. This FORMAT statement can be ignored by the person who is merely interested in what the algorithm does.

6. **WRITE**. This is very much like READ, except for one peculiar convention: when one of the quantities to be written out is a constant string, this string is found in the associated FORMAT statement, rather than in the WRITE statement itself. An example should make this clear. Suppose we want to write out the sentence THERE ARE 7 ERRORS IN THE ABOVE PROGRAM. We have a count in our program

   \[
   \text{LET COUNT = 7}
   \]

   \[
   \text{WRITE (6, 92) C, COUNT, A, B}
   \]

   This would result in the output

   THERE ARE 7 ERRORS IN THE ABOVE PROGRAM.
ONLY PROGRAMMERS SHOULD BE ALLOWED TO SORT!

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called NERRS, which is, in this case, equal to 7. We would like to write a statement something like

WRITE “THERE ARE ”, NERRS, " ERRORS IN THE ABOVE PROGRAM”.

In FORTRAN, however, we have to write something like

WRITE (6, 92) NERRS

where statement number 92, the FORMAT statement, is

92 FORMAT (' THERE ARE ', 13, ' ERRORS IN THE ABOVE PROGRAM').

The 13 here is the format for NERRS (a three digit integer), while the 6 in the WRITE statement is like the 5 in the preceding READ statement; that is, unit number 6 is the standard output medium.

Where constant strings are not present, WRITE is very much like READ. That is, we can have a statement WRITE (6, 93) N, A, B which will write out the quantities N, A, and B. In some versions of FORTRAN, we find PRINT 93, N, A, B with the unit number 6 left out; the only thing to remember here is that we are not printing out the number 93, as this is the FORMAT statement number, just as before.

(7) DO. Suppose we want to repeat a group of statements N times. Then, just before these statements, we can write

DO 25 I = 1, N

where the last statement in the group to be repeated has statement number 25. This will not only cause the statements to be repeated, but will set the index I to a different value each time: 1 the first time, 2 the second time, and so on up through N the last time.

(8) CALL. The FORTRAN programmer can write CALL SUB, just like the 8080 programmer (the 6800 programmer would write JSR SUB, meaning "Jump to subroutine SUB"); the difference arises when the subroutine SUB has parameters. Where the small system user has to figure out his own way of passing parameters, FORTRAN does this automatically. If the parameters are A, B, and C, for example, the FORTRAN programmer simply writes CALL SUB(A, B, C).

(9) SUBROUTINE. At the beginning of every subroutine there is a statement like SUBROUTINE SUB(X, Y, Z), which says that the name of this subroutine is SUB and that its dummy parameters (sometimes called formal parameters) are X, Y, and Z. This means that if SUB is now called as above (that is, with the statement CALL SUB(A, B, C)), then X corresponds to A,
Y corresponds to B, and Z corresponds to C.

(10) RETURN. This is used in a subroutine in place of STOP; it stops the subroutine and returns to the program (which could possibly be another subroutine) which called this subroutine. If we use STOP in a subroutine, the entire job will stop.

(11) FUNCTION. In FORTRAN there are certain special functions: SORT (square root), SIN (sine), COS (cosine), and the like. Thus the FORTRAN statement Y = SORT(A) sets Y equal to the square root of A. But FORTRAN also allows the programmer to make up his own functions. These are coded like subroutines, with two exceptions. We start a function with a statement like FUNCTION F(X, Y, Z) which tells us that F is the name of the function and X, Y, and Z are the dummy parameters. At the end of the function (normally just before RETURN) we write F = e, where e stands for whatever we want the value of the function to be. If we then use the function F by writing U = F(A, B, C), then, just as before, X corresponds to A, Y corresponds to B, Z corresponds to C, and e will now be computed and U will be set equal to e.

(12) DIMENSION. This is used to define tables (arrays). DIMENSION A(50), for example, defines a table of 50 variables which are called A(1), A(2), and so on up through A(50). We can also, of course, make reference to A(i), A(j+1), and the like. DIMENSION B(3, 3) defines a matrix of nine variables, B(1, 1) through B(3, 3), and we can make reference to B(i, j) if i and j have values 1, 2, or 3.

(13) REAL. Most large systems, of course, have floating point representations for real numbers. FORTRAN assumes that every variable represents a real number unless its name begins with L. Thus REAL LAMBDA specifies a variable in a subroutine which is called this subroutine. If we use REAL instead of INTEGER for a variable, the entire job will stop.

(14) INTEGER. The INTEGER statement allows us to define variables whose names do not begin with I, J, K, L, M, or N to be integers rather than real numbers. An integer on a large system is typically 32, 36, 48, or 60 bits long; an integer on a minicomputer or a midsize computer is typically 12, 16, 18, or 24 bits long.

(15) COMMON. Normally, when we have a variable in a subroutine which is called (for example) J, and another variable in the main program (or another subroutine) which is also called J, these are treated by FORTRAN as two different variables. The
exception to this rule occurs when J appears in COMMON statements in both programs. The rules for writing COMMON statements properly are complex; but in a published program, one may always assume that the rules have been properly followed.

Every so often, one will be faced with a program written in some algebraic language other than FORTRAN, such as ALGOL or PL/I. The main differences between these languages are as follows:

1. GOTO. Statements in FORTRAN and BASIC have numbers, but statements in ALGOL and PL/I have names. When a name is defined it is followed by a colon.

2. IF. Most algebraic languages other than FORTRAN use the additional keyword THEN, and many also allow the keyword ELSE (meaning “otherwise”). Thus IF α THEN β ELSE γ means “If α is true, then do the statement(s) β; otherwise, do the statement(s) γ.”

3. STOP. ALGOL does not have a STOP statement; to stop in the middle of a program, one writes GO TO α, where α is a label (followed by a colon) just before END at the end of a program.

4. END. In ALGOL and PL/I there are two kinds of END. One is used just as in FORTRAN, and the other is in the middle of a program paired with BEGIN. The statements between BEGIN and END are called a block (or sometimes a compound statement), and may take the place of a single statement wherever one can legally occur in the language. PL/I also requires an END paired with each DO.

5. READ. PL/I has two kinds of READ, one called READ and the other called GET. The GET variation is used when built-in format conversions are to be exercised. Some variations of GET involve no statements at all, but many ALGOL programmers assume that there is a subroutine called inreal(x), which inputs the real number x, and similarly ininteger(x), which inputs the integer x.

6. WRITE. PL/I uses WRITE as well as another form called PUT. WRITE corresponds to READ and PUT corresponds to GET. ALGOL has outreal(x) and outinteger(x), which correspond to inreal(x) and ininteger(x).

7. DO. In PL/I, in order to repeat certain statements from i = 1 to N, we write DO I = 1 TO N (note the word TO), followed by the statements to be executed, followed by END. In ALGOL, we write

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for \( I := 1 \) step 1 until \( N \) do begin, followed by the statements, followed by end; if there is only one statement to be repeated, then begin and end are not necessary (although they may appear). In BASIC, we write \FOR I=1 \TO N, followed by the statements, followed by NEXT I.

(8) CALL. In BASIC we write GOSUB \( n \), meaning “Go to a subroutine at statement number \( n \)”; subroutines in BASIC do not have names as they do in FORTRAN, ALGOL, and PL/I. In ALGOL, we leave out the word CALL; thus \( \text{SUB}(A, B, C) \) by itself is a statement which calls the subroutine \( \text{SUB} \).

(9) SUBROUTINE. Subroutines in ALGOL and PL/I are called procedures, and where in FORTRAN one would write \( \text{SUBROUTINE } \text{SUB}(X, Y, Z) \), in ALGOL one writes procedure \( \text{SUB}(X, Y, Z) \), and in PL/I one writes \( \text{SUB}: \text{PROCEDURE}(X, Y, Z) \). The situation in ALGOL is especially confusing because a subroutine is written inside the program of which it is a subroutine, at the beginning of that program with all the other declarations (real, integer, and the like). This makes it very difficult, in practice, to figure out where the first statement of an ALGOL main program is, particularly if it has a lot of nested subroutines. You have to start at the beginning of the program and work your way through all the subroutines, each of which is declared by a procedure statement with a matching end (which you have to find); then you suddenly come, with no warning, upon a simple statement like \( I := 1 \) and, believe it or not, that is where you are supposed to start executing.

(10) RETURN. In PL/I you write \( \text{RETURN}(e) \) to correspond to \( \text{RETURN } F = e \) followed by RETURN in FORTRAN, where \( F \) is the name of a function.

(11) FUNCTION. The terms corresponding to the FORTRAN FUNCTION for ALGOL and PL/I are INTEGER PROCEDURE, REAL PROCEDURE, and the like; the adjective before PROCEDURE tells you whether the value of the function is supposed to be an integer, a real number, or whatever.

(12) DIMENSION. In BASIC, one writes DIM instead of DIMENSION. In ALGOL, one writes integer array or real array; in PL/I, one writes DECLARE, which may be shortened to DCL (and usually is). DECLARE in PL/I is an all-purpose declaration having dozens of variations, but DECLARE \( A(100) \), sometimes followed by various other keywords, is roughly like DIMENSION \( A(100) \) in FORTRAN, as is real array

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A [1:100] in ALGOL (the 1 here is the lower bound on subscripts, which may be arbitrary in ALGOL, although it is always 1 in FORTRAN).

(13) REAL. In ALGOL, the REAL attribute refers to representation as a floating point number. [Note that the attribute FLOAT performs this function in PL/I, and that REAL in PL/I is used only to distinguish real from complex numbers. . . . .]

(14) INTEGER. BASIC assumes that all numbers are real; integers will be treated as if they are real numbers, which usually works the way we want it to, although some operations like division must be watched carefully. In ALGOL, all integers must appear in integer statements.

(15) COMMON. In PL/I, all main routine variables are common (called "global" in PL/I parlance) to internal subroutines (ie: the subroutine is declared by a PROCEDURE statement within the boundaries of the calling PROCEDURE and its END) unless it is redefined in the subroutine. The EXTERNAL attribute is used to share variables between external procedures. In ALGOL, any variable in a main program may automatically be used in any of its subroutines, unless there is another variable declared in the given subroutine that has the same name.

(16) Assignment statements. In ALGOL, the symbol := is used where = is used in FORTRAN, BASIC, and PL/I. In addition, = is used where .EQ. is used in FORTRAN. Some versions of BASIC permit, and some require, the word LET at the beginning of every assignment statement.

(17) Semicolons. Every statement in ALGOL ends with a semicolon unless it is followed by end. Every PL/I statement is followed by a semicolon.

There are hundreds of other differences between the various algebraic languages, but these are the basic ones which are required to be able to read published algorithms in FORTRAN, ALGOL, BASIC, and PL/I. Most such algorithms, with a few notorious exceptions, are presented in such a way as to use only the rules described above. The reader whose appetite has been stimulated by the possibilities of algebraic languages might do well to supplement his small system knowledge by renting a small amount of time (perhaps $100 worth) on a large system and trying out various features of FORTRAN, PL/I, and the like. This is, of course, in addition to the use of cross assemblers and cross compilers, which still require large systems to produce small system object code.
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Comments on the RF Entry Method for Video Monitors

Victor A Wiseman
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Photo 1: Author’s system with Processor Technology SOL-20 computer and rear view of RF entry video display.

Photo 2: Typical display of the system.

This is a reply to a statement in Mr Fylstra’s article “Convert Your TV Set to a Video Monitor,” which appeared in the May 1978 BYTE, page 22.

While I will not contest Mr Fylstra’s statements and arguments that the direct video entry method is definitely superior to the radio frequency (RF) entry method, I must take a stand against his statement that the radio frequency entry method “…is enough to display at most about 32 characters per line.” Mr Fylstra has accurately identified and reported the pros and cons of the two methods, but an individual reading his article and contemplating a 64 or 80 character per line display would immediately discard the possibility of the radio frequency entry method. My experiences should prove this to be unfair.

When considering the options I had for adding a video display to my SOL-20, I considered buying a monitor for $180, converting my television for direct entry, and using the radio frequency entry method. Since I already had a portable television suitable for the job, I decided against spending $180 for a monitor. This left me with the direct video and radio frequency entry methods. I then armed myself with a Sams Photo-Fact folder and performed some exploratory surgery on my television. This convinced me that I could use the direct entry method, but it would require some care and time to do properly. I finally decided that the most expedient method would be the radio frequency entry method; the cost was low enough so that, if it didn’t work out, I would not have lost much.

As it turned out, the radio frequency entry method proved entirely satisfactory for my needs and I have been using it for the past year and a half.

Photo 1 shows my system. The processor is a SOL-20 which incorporates everything on a single printed circuit board, including the video display generator. The output of this generator is fed through the black cable coming from the back of the SOL and across the back of the television. This is part of a section of shielded coaxial cable supplied with the SOL-20 kit. It is connected to a small aluminum box containing a Pixe-Verter, a battery pack of 4 AA cells, and an on/off switch (hidden). The radio frequency output from the Pixe-Verter is fed through a twisted pair of solid conductor wires to the small black connector on the back of the television set. This connector was supplied with the set and is used for connecting an external antenna. The upper binding posts are for VHF and the lower are for UHF, the switch in the center is for a local/distant setting (it is set for local).
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The television itself is a Sony Model 9-51UW with a 9 inch (13.5 cm) diagonal screen. It is over 11 years old and well-used.

About the Photos

All photos were taken with a Leica M3 with a 50 mm F/2 dual range Summicron lens, using Tri-X ASA 400 35 mm film. The delayed shutter release was used to dampen vibration effects. Photo 1 was taken with existing light from a window on a sunny day at 1/60 second at f/5.6. Photos 2 and 3 were taken at a distance of 21 inches (53 cm) at 1/30 second at f/4. The bright diagonal bands seen on the screen are due to the discrepancy between the shutter speed, the scan rate of the television, and the focal plane shutter of the camera used to take the photos. The darkening at the top of the screen, the heightening of the characters at the top, and the slight slanting of the characters is due to the poor vertical and horizontal linearity of the set. The slight fuzziness of the display at the left of the pictures is due to depth of field restrictions. Overall, photos 2 and 3 accurately represent what is seen by the human eye and brain (eye persistency eliminates the bright diagonal bands).

Photo 2 is a common display of a portion of a program listing using all upper case characters. Photo 3 is a generated display of a selected portion of the available character set. Control characters were eliminated, since they would cause unwanted display functions like carriage returns and screen clearing. Photos 2 and 3 each show one or more lines with 64 characters each.

Photo 3 is most indicative of the limitations of the radio frequency entry method. The lower case characters m and w show a definite merging of the dot pattern. The upper case versions also show this effect to a lesser degree. In normal use, however, the human eye and brain manage to fill in gaps in definition.

I hope this material will show that the radio frequency entry method is capable of producing a very satisfactory video display of 64 characters per line.
space potential of the current 8 bit microprocessors has effectively become saturated.

This saturation of memory address space in the 8 bit 40 pin package microprocessors with a mere eight parts leads to the next new high in semiconductor technology's current innovations: the testing and subsequent approach to volume production of three excellent large scale microprocessors which provide 23 and 24 bit address spaces capable of reaching 8 or 16 million bytes of memory (or peripheral hardware.) I refer of course to the new crop of 16 bit traditional microprocessors introduced by Intel, Zilog and Motorola. Perhaps the first such part was the Intel 8086 announced last spring and most likely in production by the time this is written. (From one contact I heard mention of an even newer 8087, but have not seen any written information on such a part to date.) The second part, announced shortly after the 8086 last spring, is the Zilog Z-8000. But what appeals to my mind, after hearing engineering introductory talks on all three of these new products by representatives of the companies, is the Motorola 68000. It is my own personal favorite, providing a 24 bit byte address space and a relatively simple system design concept without elaborate memory paging and address bus multiplexing requirements. It is the kind of 16 bit microprocessor I like, namely one with a separate 24 bit byte address bus, a 16 bit bidirectional data bus and simple power supply requirements. If I were to build a new system of the homebrew variety at the present time, it is the one I would most likely use. For the moment then, the three processors from Intel, Zilog and Motorola are the best possibilities for overcoming the address limitation problems which become very real as the 64 K dynamic memory parts come to market.

The third major development of the current crop of large scale integration technology is that of new video display controller chips. These parts are actually in production at the present time, and are, no doubt, quietly buried in the designs of many of the personal computing products which have come to the market for the first time in late 1978 and those which will arrive in early 1979. We've already received a number of articles on this kind of device, articles which readers will see in an upcoming special issue on the theme of video graphic interfaces.

The final and most exciting development of recent months was relayed to me by Ken Bowles of the Pascal project at the University of California at San Diego (UCSD) in a phone conversation this past September 20. This is the development of a microcomputer chip set which directly executes the UCSD Pascal compiler's p-code intermediate language. The firm responsible for this innovation is Western Digital, 3128 Red Hill Av, POB 2180, Newport Beach CA 92663. In phone conversation with Dr Larry Lotito of Western Digital I found out some more details about the processor, which he and Ken jokingly call a "sand casting" of the UCSD p-code interpreter. This first high level language machine in microprocessor form will come to market in several forms in January of 1979.

As readers familiar with the development of minicomputer technology into microcomputer form will recall, Western Digital was the semiconductor manufacturer which designed and first supplied the chip sets for the Digital Equipment Corp (DEC) LSI-11 product several years ago. These chip sets consist of a microprogram controller and a set of read only memory programs which emulate the desired computer's architecture. After the first LSI-11 parts had been created and marketed, DEC began its own in house semiconductor fabrication efforts and Western Digital turned out to have less of a
market for its microprocessors than might have been expected.

In the past two years or so, several variations of the basic 16 bit architecture of this chip set have been offered on a custom basis, and at least one such variation has appeared in the form of an advanced S-100 bus computer (MCP-1600). Of course, Western Digital has continued to supply standard parts for the digital systems markets, such as floppy disk controller chips, and serial communications interfaces, among others. With the experience of producing more than one read only memory microcode definition for the MCP-1600 microprocessor system design, it was not hard for the firm to write the microcode needed to emulate a new design, a "P-engine" that executes the intermediate language codes produced by the Pascal compiler developed by UCSD. Western Digital calls the resulting chip set the "Pascal Micro Engine" and considers this name their proprietary trademark. According to Larry, this product will be widely available in several forms in January of 1979. What is significant is that the software development system for this chip set is the UCSD Pascal system without any modification: a com-

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Western Digital, however, considers itself mainly a semiconductor manufacturer, so one of the reasons for the relatively low price on the development system's processor kernel is to promote sale of the chip sets for use in new designs. We can expect to see more than one personal computer manufacturer taking advantage of this development, for the characteristics of the directly executed p-code method allow programs to run from six to eight times faster than would be possible using the LSI-11 versions of the software.

In the LSI-11 version of the UCSD system (or any other conventional processor's version) there are two levels of emulation. At the first level is the hardware needed to execute the instruction set of the particular microprocessor, be it 8080, LSI-11, 6800, 6502 or any other instruction set. The second level comes in when the particular microprocessor runs an interpreter which emulates the P-machine. With the Western Digital innovation, the P-machine is directly executed by the hardware which is seen by the system designer. This direct execution is the reason for the improvement relative to the LSI-11 which uses very similar hardware. Designers who are interested in creating dedicated microprocessor systems that use the most advanced and reliable software development techniques will find this chip set a natural one to use. Designers of personal computing products will also find it useful, for the extremely powerful UCSD Pascal software system fits naturally into the machine.

This announcement of a high level language machine for Pascal is perhaps the high point of the current crop of wonders which include the 64 K memories, large scale microprocessors and video controllers. Some people have disputed the relevance of high level languages like Pascal, on the ground that they demand expensive systems, but the arrival of the relatively inexpensive Western Digital machine next month is perhaps the last word on that argument for now. The nature of the new levels of sophistication in the larger microprocessor chips such as the 8086, Z-8000 and 68000 complement the new heights of memory density in the 64 K chips and further indicate both the need for and practicality of high level languages like Pascal in future personal computers.

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As a recent Apple II purchaser, I enjoyed your review of the Apple II (March 1978 BYTE, page 18). I was especially interested to see that you encountered most of the same problems I did, such as the interference with the color receiver. I too am using the M & R Enterprises modulator that installs inside the Apple II along with a low priced GE portable, and the interference with my first setup was pretty bad.

Something about the length of the lead to the TV set got me to thinking. I remember making dipole antennas, and somehow 4 feet seemed like a familiar dimension. Channel 3's picture carrier frequency is about 61 MHz, for a wavelength of about 5 meters. The cable from the modulator to the color set is about 4 feet (1.2 meters) long or almost exactly a quarter wave. That makes it a very good antenna for any harmonics (60 thru 65 MHz) of the Apple clock, character generator, etc. The cable is looped through a large ferrite toroid, which helps quite a bit, but a simple modification makes things even better. All you have to do is add an 18 inch extension cable, thus mistuning the channel 3 antenna, and 90 percent of the interference will disappear.

We just got around the problem of radio frequency interference with our Apple II by use of the M & R Enterprises UHF modulator recently acquired. Without even putting a single toroidal balun core on the coaxial cable, the same Panasonic color television runs without any interference....CH

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Texas Instruments Has Introduced the TMS 4164, a Single 5 V 64 K Byte Dynamic Programmable Memory, organized as 64 K byte by 1. It comes in a 16 pin dual-in-line package, and allows upward compatibility with the 16 K byte dynamic programmable memory. The TMS 4164 single 5 V power supply design is TTL compatible, offers lower power dissipation, and is more immune to system noise. Compact layout, and an optimized design and process combination for 5 V only operation result in improved performance.

Access times range from 100 to 150 ns maximum, with minimum cycle times of 200 to 250 ns. Power dissipation is 200 mW maximum or 3 µW maximum per bit. Comparing the 462 mW power dissipation of the 16 K programmable memory at 375 ns cycle time, total maximum power dissipation of the new memory is a reduction of 60 percent, with improved cycle times, while bit density is quadrupled. As a result of the lower power dissipation, the TMS 4164 features a 256 cycle refresh with a 4 ms maximum refresh period.

Due to TMS 4164 refresh compatibility with the 16 K byte programmable memory, the basic refresh controller timing does not require major changes. The only provision required is for an 8 bit refresh counter and multiplexer when upgrading to 64 K byte from a 16 K byte system. Also contributing to higher system operating efficiency is a 1.3 to 1.6 percent refresh overhead time, compared to 2.4 percent on the 16 K byte programmable memory. The TMS 4164 is priced at $125. For further information write to Texas Instruments Inc. Inquiry Answering Service, POB 1443, M/S 669, Houston TX 77001.

Chromatics Inc has introduced the CG series line of full 8 color graphic and alphanumeric readout computers. The line consists of 13, 15 and 19 inch models featuring noninterlaced screen refresh, high resolution shadow tubes, and S12 by S12 or S12 by 256 individually addressable and color selective dots. Each model employs a Z-80 processor with full memory and input and output (IO) structure. The 13 inch model starts at $8995.

A bulletin describing the system may be obtained from Chromatics Inc, 3923 Oakcliff Industrial Ct, Atlanta GA 30340.

This new MKB-2 keyboard is designed for use with the 64 and 80 character display video boards. Standard features on the MKB-2 include: a numeric key pad, upper and lower case, cursor control keys, 2 key rollover, and automatic repeat on all keys. The MKB-2 is assembled in a heavy duty steel case with parallel interface, strobe or pulse and on board regulation (5 V, 12 V), and comes complete with standard DB25S connector and black double injection molded keys.

The price of the MKB-2 is $149. For further information, write to MicroAge, 1425 W 12th Pl #101, Tempe AZ 85281.
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A 1 year subscription costs $20. For more information, contact Dump Publications, POB 2454, Jacksonville FL 32203.

New Publication Devoted to TRS-80 User

Dump Publications has announced the release of a software publication for users of the Radio Shack TRS-80 microcomputer system. Dump is a monthly periodical incorporating news, information, and running software ready to load from a 33 1/3 revolution per minute disk record. The Dump disk can be loaded into the TRS-80 system with the use of an ordinary phonograph.

Each issue contains a wide variety of programs from finance and education to games and machine language. Programs are provided with complete documentation and line editing information for Level I and II BASICS.

A 1 year subscription costs $20. For more information, contact Dump Publications, POB 2454, Jacksonville FL 32203.

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The basic building blocks of modern computers, radar, television and pulse communication circuits are presented in this programmed text entitled A Programmed Course In Basic Pulse Circuits, by the New York Institute of Technology. This 293 page programmed learning text is organized in a logical sequence of interrelated steps. Discussions on switching devices such as unijunction transistors and silicon controlled rectifiers are included. All devices are solid state, and some material on integrated circuits is presented. Each chapter begins with a set of objectives and concludes with a set of criteria tests to measure progress.

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Pricing on the fully assembled and tested TM 990/101M-1 including 1 K word by 16 bit erasable read only memory and 1 K word by 16 bit static programmable memory is $625 in single quantities. Inquiries should be forwarded to Texas Instruments Inc, Inqury Fulfillment, POB 1443, M/S 633 (Attn: TM990), Houston TX 77001.

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This 16 K word by 8 bit programmable NMOS memory system is S-100 and card size compatible. The EMM Model 1104 is a single card plug-in assembly which is fully burned-in and tested. The Model 1104 uses EMM 4 K byte static programmable memories, and no refresh circuitry is required.

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It allows maximum processor throughput with the use of hidden refresh control logic on board. Data access time is 300 ns and cycle time is 750 ns.

On board memory select is available in 4 K byte increments up to 64 K words of memory. A write disable switch on board makes the programmable memory a read only memory to the outside world.

Complete board power consumption is under 5 W. The board size is 5.75 by 9.75 inches (14.61 by 24.77 cm). For more information, contact Chrislin Industries Inc, 31312 Via Colinas #102, Westlake Village CA 91361.

The system consists of the memory array with support electronics including address and data buffering, timing and control, and voltage regulation. The memory array is divided into four 4 K by 8 bit memory blocks, and each block can be assigned to a 4 K byte address block within a 0 to 64 K byte range. Operating modes are read, write and deposit. The deposit mode is a phase memory cycle consisting of a write followed by a read.

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PERIPHERALS

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MP710s are electrically and mechanically compatible with Micromodule and EXORciser microcomputers and operate from their +5 VDC supplies. They are programmed as memory locations and with each input using one memory bit, any read command may be used. When the board is read, logic 0 represents an open contact (low voltage); logic 1, a closed contact (high voltage). Each read command inputs the status of eight channels. Address bits A0 and A1 select the set of inputs to be read. The remainder of the address lines are used to select the board itself. The address block occupied by each board is selectable and can be located anywhere in memory.

The price of the MP710 is $355 in quantities of one to nine. For further information contact Burr-Brown, International Airport Industrial Park, Tucson AZ 85734.

Process Control Output Module

The PCO-1A process control output module provides two complete 4 to 20 mA or 10 to 50 mA process control circuits on one Wyle microcomputer system output module. The 4 to 20 or 10 to 50 ranges are independently selectable for each circuit, and both outputs are short circuit protected. The PCO-1A is priced at $345 per module (2 output circuits). Contact Wyle Laboratories/Computer Products, 3200 Magruder Blvd, Hampton VA 23666.

Microprocessor Analog Interface Module

The Wince Analog Interface Module enables laboratory and control engineers to interface thermocouples and other transducers to a microprocessor and interface the microprocessor to motors, servos, etc. Options include a 16 channel multiplexer, an 8, 10 or 12 bit analog to digital converter and one or two 8 bit digital to analog converters. The base price is $99. Write to Wintek Corp, 902 N 9th St, Lafayette IN 47904 for further information.

Computer Video to UHF RF Interface Modulator

The Micro-Verter is designed to interface microcomputers to color or monochrome television receivers as an alternative to the video monitor. The Micro-Verter operates in the UHF channels above channel 14, beyond the normal range of switching harmonics, and is designed to interface directly with the Apple II as well as with most other microcomputers. It comes complete with video cable and radio frequency (RF) output stub coupler and requires no direct connection to antenna terminals except in special cases. The radio frequency signal is coupled directly into the UHF tuner input via a 1 cm stub coupler on the back of the modulator. The approximate size of the unit is 2 by 3.5 by 4.5 inches (5.5 by 8.5 by 11.5 cm) and it is priced at $35. For more information contact ATV Research, 13th and Broadway, Dakota City NE 68731.
Introducing the simple TRS-80 Up-grade

Fast, easy, guaranteed expansion to 16K at less than half the price of Radio Shack.

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No false starts and finding you need some little item or special tool. Our 'Kit contains all the parts: 8 prime dynamic RAMs and a complete set of preprogrammed jumpers. No matter which model you have (even if you later purchase Level II software), you're covered.

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Phone: 607/273-3271
P.O. Box 91 Ithaca, New York 14850

Available off-the-shelf at these fine computer dealers.

BYTE December 1978  215
PERIPHERALS

Z-80 Arithmetic Processing Unit

Fully compatible with the Zillog Z-80 MCB, this high speed arithmetic processing unit board (HAPUB) provides the hardware necessary to accomplish arithmetic, trigonometric, inverse trigonometric, logarithmic, exponential and square root functions. HAPUB simplifies software and allows the Z-80 to perform other operations while accomplishing these functions. Also featured are fixed point integer single and double precision (16 and 32 bit), and floating point single precision (32 bit) operation with bidirectional conversion capability. The board is compatible with the Zilog Z-80 card cage and 8 bit bidirectional data bus and costs $749. Contact Signal Laboratories Inc, 202 N State College Blvd, Orange CA 92668.

Power-One has announced an addition to their Hi-Vol series triple output DC power supply line. The new model, designated HCAA-60W, is built in the industry standard package size for a 60 W triple output open frame power supply. This model outputs 5 V at 6 A with adequate overvoltage protection, +12 to 15 V at 1 A, and -12 to 15 V at 1 A. The -12 to 15 V output may be changed to -5 V at 0.4 A by jumpering two printed circuit board terminals. Targeted for use in systems requiring multiple DC voltages, the HCAA-60W will power combinations of most semiconductor devices including TTL, PMOS, NMOS, CMOS and linear devices. Total isolation between the 5 V, ±12 V and ±15 V outputs allows the user to arrange polarities to suit specific applications.

Standard features include 115/230 VAC ±10% AC input capabilities, ±0.05% line and load regulation, and full protection against short circuit and overload. Maximum output ripple is 3 mV peak to peak.

Each unit is tested and burned in and carries a 2 year warranty. The size is 9.0 by 4.87 by 3.2 inches (22.86 by 12.37 by 8.13 cm) and it weighs 7.5 pounds (3.36 kg). The price is $84.95 from Power-One Inc, Power-One Dr, Camarillo CA 93010.

Triple Output DC Power Supply

Power-One has announced an addition to their Hi-Vol series triple output DC power supply line. The new model, designated HCAA-60W, is built in the industry standard package size for a 60 W triple output open frame power supply. This model outputs 5 V at 6 A with adequate overvoltage protection, +12 to 15 V at 1 A, and -12 to 15 V at 1 A. The -12 to 15 V output may be changed to -5 V at 0.4 A by jumpering two printed circuit board terminals. Targeted for use in systems requiring multiple DC voltages, the HCAA-60W will power combinations of most semiconductor devices including TTL, PMOS, NMOS, CMOS and linear devices. Total isolation between the 5 V, ±12 V and ±15 V outputs allows the user to arrange polarities to suit specific applications.

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Hard Copy Graphics Terminal

This plotter system, called Panographic-84, has a resolution of 100 steps per inch in the X and Y directions and a cumulative error of less than .020 inches (.05 cm) in 10 inches (25.4 cm) of travel. The drives are stepping motor operated for zero drift and no adjustments. Interfacing with a computer is via eight wires from the plotter to a parallel port. When driving the plotter from BASIC language programs, complete handshaking is not required since the plotter response is considerably faster than the speed at which BASIC can drive it. If the user wishes to drive the plotter from a machine language routine, full handshake capability is available. The polarity of handshake signals is switch selectable.

Options available at present consist of a computer operated pen lifter and a vacuum formed plotter cover. Software provided with the system is written in BASIC and listings of these short routines are provided.

The price for the plotter kit without pen lifter and cover is $995. The pen lifter kit sells for $85, as does the molded plotter cover. A factory assembled plotter with pen lifter and cover sells for $1400. For more information, write to Pan Dynamics Inc, 2950 Nebraska Av, Santa Monica CA 90404.
This is a one time purchase of NEW surplus keyboards, recently acquired from the Telecommunications Division of the Singer Corporation.

The keyboard features 128 ASCII characters in a 63 key format including a "N" key, rollover, lightly weighted switch control, escape and repeat functions.

Stapled panel and positive feel switches, makes the professional quality keyboard an excellent buy at only $64.95. Limited Quantities.

**Quiet Buss**

* $2995

8803-11

168 switch (MSA)

**HEXDECIMAL KEYBOARD**

* $34.95

Mini Switch Hexadecimal keyboards are designed for microcomputer systems that require 16 key input.

Each assembly consists of 16 hexadecimal keys and MSAs to form a 4x4 character array. The consoles are protected in the lower left corner and labeled with a DEC 'HEX'. Includes complete circuitry. A total of 16 characters can be displayed. Key code can be selected in one of 2 different code sets. Schematics included.

**S-100 Mother Board**

* $24.88

GOLD 100 PIN MINI UNIVAC KEYBOARD

- Fully loaded 128 ASCII characters in 63 key format
- M OS encoder circuitry
- Key rollover, lighted shift lock, control, escape and repeat functions
- SLOPED PANEL AND POSITIVE FEEL switches - makes this professional quality keyboard an excellent buy at only $64.95.

**CONNECTORS**

- IBM 25P male plug & hood

- DB25P female

* $395

**100 PIN MSA-AI/ART**

**APPLE II 8K MEMORY**

* $34.95

- Multicomputer system
- Exclusive design
- Single +5 volt supply

**CRT TERMINAL**

- Sanders Associates

These used video display terminals were in working condition when purchased from the reservation division of a major U.S. manufacturer.

The terminals are RS-232 and should easily interface to most micro-computers or other serial devices.

Please include $35.00 for shipping, the balance will be refunded.

**MEMORY**

**DYNAMIC**

1-7 8-32 32

1105 8K1 11.50 11.50

1106 8K16 13.00 12.25

(Apple II & TRS80)

1106 8K16

- As you may be aware, publishers require advertisers to submit their ad copy 60 to 90 days prior to "press" date. That much lead time in a volatile market place, such as memory circuits, makes it extremely difficult to project future costs and availability.

To obtain the best pricing on memory we have made volume commitments to our suppliers, which in turn affords us the opportunity to sell these circuits at the most competitive prices.

**S-100 PROTOTYPE BOARD**

- Includes roller socket design, no soldering, no box assembly, no tie wrapping for $500 systems.

- Also available as a kit, please inquire for unit pricing.

**TELETYPE MODEL 43**

- 60 of 10

* $29.95

- RS-232 Interface "K" 46/47500

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**SPECIAL**

- APPLE II 16K MEMORY

- COLOR + GRAPHICS + SOUND

**MEMORY**

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- APPLE II 16K MEMORY

**DISPLAY**

- APPLE II 16K MEMORY

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- Miniature Switches

**WIRE WRAP**

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**IC SOCKETS**

- Wire Wrap low profile pins

**DISCOUNT**

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**TRANSMITTER**

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**SPECIAL SPECIAL**

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**SPECIAL SPECIAL**

- Power Adapter
Mass Storage Unit Expands System 88 Filing Capabilities

PolyMorphic Systems has increased the storage capacities of its System 88 microcomputers through the introduction of a new option, the 88/MS, which consists of two drives for 8 inch floppy disks. One disk can hold 1.2 M bytes, or more than 500 pages of text. A System 88 microcomputer with one or two 88/MS units can handle all the files and processing needs of most small businesses and professional offices.

Present owners of any System 88 microcomputer can add the 88/MS mass storage unit with no changes in their equipment's operating system. Ready to use packages are available for doing tasks such as accounts receivable.

For more information on the 88/MS, contact PolyMorphic Systems, 460 Ward Dr, Santa Barbara CA 93111.

Short Length Cassettes Designed for Personal Computers

Microsettes are short length, high quality cassettes designed for microcomputers. They feature a premium quality Philips cassette and high energy audio tape. Each cassette comes in a hard, 2 piece Norelco style box with two extra labels. The 50 foot length of tape in the C-10 Microsette provides slightly more than five minutes of recording per side. For additional information about the C-10 Microsette write to Microsette Co, 777 Palomar Av, Sunnyvale CA 94068.

Circle 596 on inquiry card.

Floppy Disk Systems Software

Transparent to RT-11

The new Remex-11 floppy disk systems are integrated hardware and software units that connect directly to the PDP-11 Unibus or LSI-11 Q bus. The systems are available with a utility function that permits data interchange between IBM 3740 diskettes and any RT-11 supported device.

The new plug compatible versions of the Remex-11, the Remex 11/11 and 11/12, are completely software transparent to the RT-11 software on the LSI-11 computers while offering added features. The Remex-11 provides read only memory bootstrapping as a standard feature as well as individual write protect switches to each drive, busy and error status indicators, and an automatic reinitialize function.

For increased performance while still maintaining media compatibility with PDP-11 and LSI-11 systems, the Remex 11/21 and 11/22 are available. These systems will accept up to four diskette drives. Data can be transferred in 16 bit words, and up to 65 K words can be transferred in a single input/output (I/O) operation. For additions, the data buffer in the RT-11 controller can be increased to two full sectors.

The Remex 11/31 and 11/32 employ 16 sector and track soft sectoring format. A contiguous file allocation structure increases throughput by as much as 50 percent.

Both media compatible and expanded capacity systems connect to the PDP-11 by a bus extension cable; therefore no 10 slot is required.

Remex-11 prices begin at $3195 complete. For further information contact Marketing Manager, Remex Division, Ex-Cell-O Corp, 1733 E Alton St, Irvine CA 92713.

Circle 597 on inquiry card.

New Floppy Disks from Omni Products Company

New floppy disks are available from Omni Products Co, POB 223, Marlton NJ 08053. The disks include a full IBM compatible, soft sectored version, as well as Shugart compatible, hard sectored and Memorex compatible, hard sectored versions. They are designed to meet or exceed IBM and ANSI standards, and a written guarantee is furnished. Prices are $4.50 in quantities through nine and $4 for orders of more than 50. Include $1.50 for shipping per order. NJ residents should include 5% sales tax.

Circle 598 on inquiry card.
**16K E-PROM CARD**

**Imagine having 16K of software on line at all time!**

**S-100 (lmsa/Altair) Buss Compatible!**

**$59.95 kit**

**SPECIAL OFFER:**

Our 2708's (456NS) are $8.95 when purchased with above kit.

---

**NEW PRODUCTS FOR 1979**

New products are scheduled for delivery during January 1979. Some may be available sooner. Call.

**Z-80 CPU KIT**

**$129**

For S-100 Buss. Features Jump on Reset capability. We feel this board has the most correct PAM and VSYNC signal for trouble free operation. Complete kit. More data on request. (For 4MHz ADD $10)

**16K STATIC RAM KIT**

**$295**

For SS-50 (S.W. TECH. 6800) Buss. Fully static uses 2114 RAM's. 450 NS. At last, a quality RAM board for this popular Buss at an affordable price. Complete kit. Additional Data on request.

**DUAL DENSITY FLOPPY DISC CONTROLLER**


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**ALARM CLOCK CHIP**

N.S. MMS3515A.A. Six Digits. With full data. New! $2.49 each

**FULL WAVE BRIDGE**

4 AMP, 200 PIV. 69c 10 FOR $5.95

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**2708 EPROMS**

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**16K STATIC RAM KIT**

**$295.00**

COMPLETE KIT

**16K STATIC RAM KIT**

**FULLY S-100 COMPATIBLE!**

**FULLY STATIC, AT DYNAMIC PRICES!**

**WHY THE 2114 RAM CHIP?**

We feel the 2114 will be the next industry standard RAM chip. We've heard the horror stories about some Dynamic RAM Boars having trouble with DMA and FLOPPY DISC DRIVES. Who needs these kinds of problems? And finally, even among other 4K Static RAM's, the 2114 stands out. Not all 4K static Rams are created equal! Some of the other's have sticky chip enable lines and various timing windows just as critical as Dynamic RAM's. Some of our competitors' 16K boards use these "tricky" devices. But not us! The 2114 is the only logical choice for a trouble-free, straightforward design.

**BLANK PC BOARD WITH DOCUMENTATION - $33.00**

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**LOW PROFILE SOCKET SET - $12.00**

2114's 4K RAM's - 8 FOR $69.95

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S-100 Bus Prototyping Circuit Board
Accommodates up to 70 Integrated Circuits

Manual Details New Temperature Switch
An 8 page manual detailing the properties and applications of Midwest Components Inc's temperature switch is available from the company. This switch utilizes a reed switch and temperature activated magnets for sensing. For this manual, write to Midwest Components Inc, POB 787, 1981 Port City Blvd, Muskegon MI 49443.

Intelligent Keyboard Has Capacitive Keyswitches
This new solid state keyboard uses a second generation microprocessor and low profile capacitive keyswitches. The keyboard uses an 8 bit single integrated circuit processor with on chip read only memory, programmable memory and erasable read only memory. All key functions are software controllable. The microprocessor permits automatic repeats, multiple application programs in a single intelligent encoder, field program changes using new firmware, serial and parallel input/output (IO), and n-key rollover (3 key rollover being standard). The switches have a life expectancy of 100 million operations. The legends are selectable from a wide selection of symbols and letters in a host of languages and disciplines.

For further information about this keyboard, contact C P Clare & Company, 3101 W Pratt Av, Chicago IL 60645.

8080 Processor Board Offered
This S-100 bus 8 bit processor board uses the 8080A processor. 74LS244 bus drivers are utilized to provide low power with higher drive capability. A switch selectable jump on reset circuit is provided for use in systems without a front panel. Low profile sockets are provided for all integrated circuits.

The 8080 board is $175 assembled and $120 in kit form. For more information write to Electronic Control Technology, 763 Ramsey Av, Hillside NJ 07205.
APPLE II SERIAL I/O INTERFACE *
Part no. 2
Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain, RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine • jumper selectable • Can output in correspondence code compatible • Auto scroll • Non-destructive cursor • Cursor inputs: up, down, left, right, home, EOL, EOS • Scroll up, down • Requires +5 volts at 1.5 amps, +12, -12, and -5 volts at 30 mA • All 7400, TTL chips • Char. gen. 2513 • Upper-case only • Board only $15.00 ; with parts $42.00 ; assembled and tested $62.00.

MODERN *
Part no. 109
• Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • No coils, only low cost components • TTL input and output • Connect 8 ohm speaker and crystal mic. directly to board • Uses XR FSK demodulator • Requires +5 volts • Board $7.60 ; with parts $27.50.

DC POWER SUPPLY *
Part no. 6085
• Board supplies a regulated +5 volts at 3 amps, +12, -12, and -5 volts at 1 amp • Power required is 8 volts AC at 3 amps, and 24 volts AC.C.T. at 1.5 amps • Board only $12.50 ; with parts excluding transformers $42.50.

TAPE INTERFACE *
Part no. 111
• Plays and records Kansas City Standard tapes • Converts a low cost tape recorder to a digital recorder • Works up to 1200 baud • Digital in and out are TTL-parallel • Output of board connects to mic. in of recorder • Earphone of recorder connects to input on board • No coils required • Supplies +5 volts, low power drain • Board $7.60 ; with parts $27.50.

8K STATIC RAM
Part no. 300
• 8K Altair bus memory • Uses 2102 Static memory chips • Memory protect • Gold contacts • Wait states • On board regulator • S-100 bus compatible • Vector input option • TRI state buffered • Board only $22.50 ; with parts $160.00.

RF MODULATOR *
Part no. 107
• Converts video to AM modulated RF, Channels 2 or 3 • So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs Journal. Recommended by Apple. • Power required is 12 volts AC.C.T., or 5 volts DC • Board $7.60 ; with parts $13.50.

TIDMA *
Part no. 112
• Tape Interface Direct Memory Access • Record and play programs without bootstrap loader (no prom) has FSK encoder/decoder for direct connections to low cost recorder at 1200 baud rate, and direct connections for inputs and outputs to a digital recorder at any baud rate • S-100 bus compatible • Board only $39.00 ; with parts $110.00.

RS 232/TTL INTERFACE
Part no. 600
• Converts RS-232 to 20mA current loop, and 20mA current loop to RS-232 • Two separate circuits • Requires +12 and -12 volts • Board only $4.50 ; with parts $7.00.

ELECTRONIC SYSTEMS
To Order:
Mention part number and description. For parts kits add "A" to part number. In USA, shipping paid for orders accompanied by check, money order, or Master Charge, BankAmericard, or VISA number, expiration date and signature. Shipping charges added to C.O.D. orders. California residents add 6.5% for tax. Outside USA add 10% for air mail postage, no C.O.D.'s. Checks and money orders must be payable in US dollars. Parts kits include sockets for all ICs. Components, and circuit board. Documentation is included with all products. All items are in stock, and will be shipped the day order is received via first class mail. Prices are in US dollars. No open accounts. To eliminate tariff in Canada boxes are marked "Computer Parts" Dealer inquiries invited.

Circle 125 on inquiry card.
Single Chip Z80-SIO for LSI Microcomputer System

A high speed, dual channel, multi-protocol serial data communications controller circuit, the single chip Z80-SIO, has been introduced by Zilog, 10460 Bubb Road, Cupertino CA 95014. The SIO is designed to work with Zilog's Z-80 microcomputer family and also interfaces with most other 8 bit and 16 bit processors. The serial IO controller, an N/MOS 40 pin device, is a peripheral component that can control communications peripherals and format data in data communications networks. Each of the SIO's full duplex channels has four control lines for most commonly used modems. Applications include fiber optics, microwave transmission and satellite communications. For systems with 2.5 MHz clock rate, the SIO's data rate goes up to 550 K bits per second, while in a 4 MHz system, it's up to 880 K bits. Price is $49 in small quantities. Circle 622 on inquiry card.

Complex Sound Generator Integrated Circuit

The SN76477N, a complex sound generator integrated circuit, has been announced by Texas Instruments, POB 84, M/S 812, Sherman TX 75090. This IC can be used to generate virtually any complex sound: siren, gunshot, jet engine, whistle, pinball sounds, etc. Since it is an integrated injection logic (I2L) linear integrated circuit with low power consumption, it is ideally suited for battery powered applications. The SN76477N contains a voltage controlled oscillator, super low frequency oscillator, white noise generator, noise filter, oneshot, mixer, an attack and decay envelope generator. The desired sound is externally programmed by the user through logic and analog inputs. New sounds can be implemented or modified quickly. The SN76477N is designed for operation from -10°C to 40°C. It is offered in a 28 pin package. Price is $1.65 in quantities of 100. Circle 623 on inquiry card.

A low cost single channel direct memory access controller (DMAC) has been introduced by Western Digital Corp, 3128 Red Hill Av, POB 2180, Newport Beach CA 92663. The DM 1883 is said to be fully compatible with all popular microprocessors built today. It includes the following features: control of all memory handshaking and device control; full 16 bit memory address and block length capability; block or word move; automatic end of block (EOB) shutoff and interrupt on EOB or error detection; and the option of auto load and bus timeout interrupt. The DM 1883 is powered by a single +5 V supply. Circle 624 on inquiry card.

Second Sourced TR 1953 USART Replaces 8251

The second sourced TR 1953 universal synchronous and asynchronous receiver transmitter (USART) is said to be the lowest priced replacement for the 8251. The TR 1953's complete compatibility with the 8251 USART is further enhanced by synchronous and asynchronous operation, with 5 to 8 bit characters on both modes. Internal or external character synchronization and automatic sync insertion is featured in the synchronous mode; 1, 16 or 64 times bps rate, 1, 1½ or 2 stop bits and false start bit rejection on the asynchronous mode. The TR 1953 comes in a 28 pin package, with TTL compatible IO, and operates on a single +5 V supply. Write to Western Digital Corp, 3128 Red Hill Av, POB 2180, Newport Beach CA 92663 for a sample. Circle 625 on inquiry card.
The EW-2001  A “Smart” VIDEO BOARD KIT At A “Dumb” Price!
A VIDEO BOARD + A MEMORY BOARD + AN I/O BOARD – ALL IN ONE!

- STATE OF THE ART TECHNOLOGY USING DEDICATED MICROPROCESSOR I.C.
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$199.95
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Basic Software Included

SPECIAL FEATURES:
- S-100 bus compatible
- Parallel keyboard port
- On board 4K screen memory (optional)* relocatable to main computer memory
- Text editing capabilities (software optional)
- Scrolling: up and down through video memory
- Blinking characters
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- Provision for on board ROM
- CRT and video controls fully programmable (European TV)
- Programmable no. of scan lines
- Underline blinking cursor
- Cursor controls: up, down, left, right, home, carriage return
- Composite video
- *Min. 2K required for operation of this board.

DISPLAY FEATURES:
- 128 displayable ASCII characters (upper and lower case alphanumeric, controls)
- 64 or 32 characters per line (jumper selectable)
- 32 or 16 lines (jumper selectable)
- Screen capacity 2048 or 512
- Character generation:
  - 7 x 11 dot matrix
  - Options:
    - Sockets .................. $10.00
    - 2K Static Memory
      (with Sockets) ........... $45.00
    - 4K Static Memory
      (with Sockets) .......... $90.00
    - Complete unit, assembled and tested with
      4K Memory ............... $335.00
    - Basic software on ROM .... $20.00
    - Text editor on ROM ....... $75.00

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ASCII KEYBOARD KIT $74.00

Additional Improvements: Double Size Return Key
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- Selectable Positive or Negative Strobe, and Strobe Pulse Width
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- 3 User Definable Keys
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  - 17-3/16" x 5"

OPTIONS:
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  - Blue and White ........ $27.50
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- I.C. Sockets .............. $ 4.00
- Serial Output Provision
  - (Shift Register) ........ $ 2.00
- Upper Case Lock Switch for Capital Letters and Nos. $ 2.00
- Assembled (on Sockets) .... $90.00

APPLE II I/O BOARD KIT
Plugs Into Slot of Apple II Mother Board

- 18 Bit Parallel Output Port
  - (Expandable to 3 Ports)
- 1 Input Port
- 15mA Output Current Sink or Source
- Can be used for peripheral equipment such as printers, floppy discs, cassettes, paper tapes, etc.

OPTIONS:
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  - SWTP PR40 or IBM Selectric
- Price:
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    - Port for $49.00
  - 1 Input and 3 Output
    - Ports for $64.00
  - Dealer Inquiries Invited

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WRITE FOR FREE CATALOG
Minimum Order: $10

By 11 December 1978 223
A Single Board Microcomputer System

The SYM-1 is a complete microcomputer including keyboard, display and operating software. Some of the features of this stand-alone system include:

- A SY6502 microprocessor device;
- 1 K bytes of user programmable memory, expandable to 4 K bytes in board sockets;
- 28 key audio response keypad;
- RS-232 and current loop interface electronics and card cage are available for use with S-100 boards.

The SYM-1 is priced at $269. Contact SynerTek, 3050 Coronado Dr, Santa Clara CA 95051.

New Microcomputer System from OSI

Ohio Scientific has announced a new microcomputer system, designated the C3-OEM. Its applications include use as a general purpose computer or controller in large equipment such as medical diagnostic equipment, scientific equipment, analytical equipment and industrial control applications. It is also suited for small systems software since it will run

- software for the 6502, 6800, 8080 or Z-80.

Its features include:

- Single chassis construction, which can be either tabletop mounted or rack mounted, including dual 8 inch floppy disks for 500 K bytes of on line storage, 32 K bytes of static programmable memory, one RS-232 port, and Ohio Scientific's triple processor board which supports the 6502A, 6800 and Z-80 processors. The system comes complete with a 6502 disk operating system and BASIC for disk and multiple processor switching software.

- The smallest system, VP-80, includes 32 K bytes of programmable memory.

All VP series units include a video display offering programmable screen formats with up to 80 characters per line and 24 lines per frame. The video processor has graphic capabilities and supports an optional light pen. Reverse video, blinking and highlight for single characters or fields are included, as well as an underline or block cursor.

The entire VP series includes the CP/M disk operating system. Also available are several BASIC interpreters and the C-BASIC compiler. Text editing and assembler are included with the software.

Low Priced Microprocessor Comes Completely Assembled

This complete ready to use microprocessor offers an economical solution for both scientific applications and industrial usage. The MICRO-68 computer system is priced at $495 and comes completely assembled. Built around the Motorola/AMI/Hitachi 6800 processor, the MICRO-68 comes with its own integral power supply, 16 bit keyboard, 6 digit LED display, and 128 words of programmable memory. The 512 MON-1 Bug programmable read only memory contains all the software necessary to load programs easily, inspect and edit them as necessary, insert break points for debugging, and execute. Memory expansion to 64 K bytes and full 16 bit input and output can be obtained via the edge connectors, which are provided for. All of the memory lines of the MICRO-68 can be buffered on board. The MICRO-68 comes in a hardwood cabinet with a transparent smoked Plexiglas lid. The unit measures 9 by 16 by 2 inches (22.86 by 40.64 by 5.08 cm). Contact EPA Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110.
### DIODES/ZENERS

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### SOCKETS/BRIDGES

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### TRANSISTORS, LEDS, etc.

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<td>PNP</td>
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<td>2N3904</td>
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<td>NPN 15A 60v</td>
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<td>2N3567</td>
<td>NPN 15A 60v</td>
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<tr>
<td>TIP125</td>
<td>NPN Darlington</td>
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<td>LED Green, Red, Clear, Yellow</td>
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<td>MAN77</td>
<td>7seg countode (Red)</td>
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<td>7seg countode (Orange)</td>
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<td>FND359</td>
<td>7seg countode (Red)</td>
<td>1.25</td>
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- Bright, 257 ft., red display
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- Bright 300 ft. common cathode display
- Uses MMS514 clock chip
- Switches for hours, minutes and hold modes
- Includes all components, case and wall transformer
- Size: 3-1/4 x 1-3/4 x 1-1/2

JE730 $14.95

Jumbo 6-Digit Clock Kit

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- Includes MMS541 clock chip
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- 12 or 24 hour operation
- Includes all components, case and wall transformer
- Size: 6-3/4 x 3-1/8 x 1-3/4

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The incredible "Pennywhistle 103"

$139.95 Kit Only

The Pennywhistle kit is a simplified version of an electronic whistle and is built from auto parts which can be controlled with a key and a switch or a number pad. It can be controlled directly with a headphone jack and is adapted for home or other commercial use. It utilizes standard and basic components and is based on non-pressured, readily available auto parts.

Data Transmission Method
- Frequency: 2700 Hz (1/4063 kHz)

Maximum Data Rate
- 2700 Hz

Data Format
- Alternating binary (return-to-zero line encoding)

Frame Length
- 1000 ms for max

Possible Messages
- Upto 20 characters

Physical Dimensions
- All components mounted on a specially designed guide

Includes:
- A total of 20 separately mounted auto components
- A small 6-key pad

Requires a 9VDC adapter. Frequency Counter and Optional Accessories to align (9" of cable)

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- Documentation for conversion

TRS-16K $115.00

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DB25S-5 5 ft. 2-DB25S $17.95 ea

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DJ11-2 1 ft. 2 pins $2.95 ea
DJ11-4 1 ft. 4 pins $5.95 ea
DJ11-16 1 ft. 16 pins $9.95 ea

For Custom Cables & Jumpers, See JAMECO 1978 Catalog Page 85

CONNECTORS

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DB25S-5 $3.40 ea
DB25P-4 200 pair $2.95 ea

63-Key Unencoded Keyboard

This is a 63-key, terminal keyboard newly manufactured by a large computer manufacturer. It is unencoded with SPST keys, unused in any kind of PCB boards. Also includes 100 plastic 1/4" x 4" buttons. Most application in stock.

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19-key pad includes 10-keys, ABCDEF and 2 optional keys and shift key.

$16.95/each

Circle 200 on inquiry card.
Get Your Feet Wet with a Solderless Breadboard Without Wringing Your Wallet Dry

The PB-6 Pronto-Board Kit comes complete with a preassembled breadboarding socket, two preassembled solderless bus strips, four 5 way binding posts, a metal ground base plate, non-marring feet and all required hardware. When complete, its 630 tie points permit flexible configurations as many as six 14 pin dual-in-line package integrated circuits. Of the four binding posts, one is grounded to the ground base plate permitting high distributed capacitance and low distributed inductance for enhanced high speed circuit operation. The three remaining 5 way binding posts can be used to interconnect the circuit on the PB-6 to power and signal lines and the outside world. Kit is priced at $15.95 from Continental Specialties Corp, 70 Fulton Ter, New Haven CT 06509. Circle 546 on inquiry card.

Compucruise Reduces Fuel and Repair Expenses

Compucruise is an automotive microcomputer combining a 20 button backlit keyboard, 5 digit blue fluorescent display, and appropriate sensors to provide a fuel management system, trip computer, clock and digitally displayed cruise control. Compucruise monitors speed, distance, fuel flow, time, battery voltage and choice of three temperatures, inside, outside or coolant. Its fuel management system indicates average fuel consumption, fuel used and remaining, plus distance and time to empty. The precision quartz crystal computer features time, elapsed time, trip time, stopwatch and alarm. The trip computer displays distance, time and fuel to arrival. A total of 44 functions can be commanded by the touch of a button. Compucruise features cruise control that will accelerate your vehicle to any preselected road speed, can be instructed to adjust to traffic flow and has a resume feature. Either metric or English units can be displayed. With a command module no larger than a hand held calculator, Compucruise can be flush or bracket mounted, and complete hardware and installation instructions are included. The price is $189.95 from Zemco Inc, 136 Saranap Av, Walnut Creek CA 94595. Circle 546 on inquiry card.

Master System Clock for LSI-11

A master system clock for use with Digital Equipment Corporation (DEC) LSI-11, LSI-11/2, and PDP-11/03 computer families has been announced by Nortek Inc, 2432 NW Johnson St, Portland OR 97210. The dual width module combines the features of a KW-11L real time clock, a KW-11P programmable clock, and adds an RT-11 compatible date and time clock. An independently powered microprocessor helps insure that date, time and programmable count are maintained when the processor is not running. Simple operating system modifications eliminate the need for manually setting these values on power up. 13 programmable time rates from 1 MHz to once per hour are available. The programmable clock may also be used as an external event counter.

The basic unit with standard power supply and installation instructions is priced at $600. An optional battery backup power supply is available to provide protection against power failures for up to 24 hours. Circle 548 on inquiry card.

Low Cost Erasable Read Only Memory Eraser

The Information Central E-PROM Eraser is a 2 part unit consisting of a 2537 A ultraviolet lamp and a base that holds up to two erasable read only memories. It operates from 115 VAC. The price is $45; Illinois residents should add 5% state tax. For more information contact Information Central Inc, 5521 N Broadway, Chicago IL 60640. Circle 547 on inquiry card.

Attention Builders: Cases to House Prototype Electronic Circuits

These Design Mate cases are designed to house prototype electronic circuits. They are made of high impact one-piece insulated plastic and feature a slope front panel, a metal bottom and include mounting screws.

There are two models of the Design Mate case: the DMC-1 measures 6.75 by 7.5 inches (16.15 by 19.05 cm) with a height that slopes from 1.5 to 3.25 inches (3.81 to 8.26 cm); the DMC-2 measures 5.63 by 6.0 inches (14.30 by 15.24 cm) with a height that slopes from 1.5 to 3 inches (3.81 to 7.62 cm). The DMC-1 is $6.95 and the DMC-2 is $5.95. For further information contact Continental Specialties Corp, 70 Fulton Ter, New Haven CT 06509. Circle 550 on inquiry card.
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FOR PET $99
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addsthe ability to record and
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From the originator of the Digital Voltmeter, Non-Linear Systems comes the MS-15 Miniscope. It is a fine electronic instrument with a great deal of measuring capability and excellent accuracy. Its design is modern, utilizing the latest in low-power integrated circuits. Its compact design offers a free-stand or table top versatility, servicing most electronic equipment. It is handheld or portable so its use is restricted to the bench.

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<table>
<thead>
<tr>
<th>Type</th>
<th>Price</th>
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<td>4 pin</td>
<td>$9.45</td>
</tr>
<tr>
<td>6 pin</td>
<td>$7.45</td>
</tr>
</tbody>
</table>

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- For Auto, Home, Office
- Small size (2x2 in)
- Push button for second release for date
- Clocks may be ordered with either 24-hour or 12-hour format in a variety of colors.
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SPECIFICATIONS
Frequency Range: 50 Hz to 100 MHz guaranteed; 100 MHz types: 3 GHz, 10 GHz, 20 GHz, 30 GHz, 50 GHz, 60 GHz
Bandwidth: 1 GHz
Display: 4 digits
Resolution: 0.1 nsec
Accuracy: ±3
Input Impedance: 1 MΩ
Power Requirements: 100 to 120 VAC
Dimensions: 7 x 4 x 2.5 inches
Weight: 2.5 pounds

CSC Model MAX-100 Frequency Counter - Net Each $124.95

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These handheld units provide a comprehensive view of circuit conditions. Simple to use and easy to interpret, they feature a large backlit display and bright, white LED indicators that make readings easy to see. They include a built-in battery charger and a single push button that selects the measurement range. They are perfect for use in the laboratory, on the job site, or in the field.

CSC Model LM-1 Logic Monitor - Complete $59.95

LOGIC MONITOR 2
This unit monitors all types of digital systems, from simple logic circuits to complex microprocessors. It features a large, easy-to-read display, bright, white LED indicators, and a built-in battery charger. It is perfect for use in the laboratory, on the job site, or in the field.

LOGIC MONITOR 3
This unit monitors all types of digital systems, from simple logic circuits to complex microprocessors. It features a large, easy-to-read display, bright, white LED indicators, and a built-in battery charger. It is perfect for use in the laboratory, on the job site, or in the field.

CSC Model LM-2 Logic Monitor - Complete $112.95

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- MODEL 5560 (ASCII code w/cassette drive) - $1295

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- MODEL 725 IBM Selectric includes keyboard pickup switches, output solenoids, and magnet driver PCB to coordinate input/output signals.

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*See, PERSONAL COMPUTING, September 1978, "Techno Turkey and his Electric Selectric," by Lloyd Prentice and Peter Henry. In this advertisement to PERSONAL COMPUTING or to Meares Prentice or Henry does not imply their endorsement of PACIFIC OFFICE SYSTEMS or its products.*

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FOR SALE: MOS technology KIM 1 microcomputer, manuals and power supply included, $150. KIM 3 8 K memory board, manual and power supply included, $100. Martin Goldberger, 15 West 72 St, New York NY 10023, (212) 874-3176 evenings after 6 PM and weekends.

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FOR SWAP: Will swap BYTE issues May, November or December 1977, for September 1976 or January, February or April 1977. Bert Honroe, Schuurmanslaan 65, 3070 Kortenberg BELGIUM.

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FOR SALE: Poly 88 chassis with two Altair 4 K static memory boards, WAMECO 8080 processor board, Vector Graphic Reset-n-go programmable and read only memory board, Multi ple IO board with 4800 bps digital cassette deck. All are in excellent working condition. Will include nonworking 5 D Sales Z-80 processor board. Sell system for $500 or will sell separately. W R Giffen, PBO 781, Richardson TX 75080.

FOR SALE: PDP BL minicomputer with 4 K core and teletype interfaces. I Ehrlach, 284 Hendrix St, Philadelphia PA 19116.

FOR SALE: WinneX M6800 processor with ASCII keyboard, ACIA, monitor, two PAs, 5 K memory/ memory supplies, and cassette tape IO. $250 or best offer. Bob Watson, 2653 Pebble Beech Dr, Flagstaff AZ 86001, (602) 526-2312.

FOR SALE: AKI keyboard, matrix encoded, power supply and 5 level paper tape punch, $50. 5 level paper tape reader, $50. Ron Rogers, PBO 17147, Baton Rouge LA 70893.


WANTED: Cylindrical slide rule (such as Thatcher or Fuller) and pocket circular slide rule (such as Carpenter or Sperry) or any other unusual old slide rules. Also need pocket mechanical calculator (Curta). Describe and price. Dr George Wentz, PBO 626, San Marcus TX 78666, (512) 392-2872 after 7 PM.

FOR SALE: Centronics Printer # 100; used, $750. Aaron Epstein, 5437 Laurel Canyon Blvd, Suite 208, N Hollywood CA 91607, (213) 762-0020.

FOR SALE: Ithaca Audio Z-80 board, $35; Percom Data C1-8122 cassette interface, $70; D C Hayes board, $50. All bare boards with cables installed. TDL Macro assembler, text output program, Z-Tel, Zapple, text editor, $120 for all software. Kim, Calgary CANADA, 2B3-6B63.
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Pascal Blazes Into First Place

"A 'Tiny' Pascal Compiler, Part 1," page 58, by Chung and Yuen placed first in the September BOMB. Second place went to "WADUZITDO," page 166, by Larry Kheriaty. These articles placed 2.0 and 1.5 standard deviations above the mean, respectively; first and second prizes of $100 and $50 will be sent to the authors. In third place was "The Mathematics of Computer Graphics," page 22, followed by "Graphic Manipulations Using Matrices," page 156, in fourth.

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