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Volume 3 Number 10

October 1978 © BYTE Publications Inc
In This BYTE

One cause of seemingly unexplainable program errors may be incorrectly operating memory. A Memory Pattern Sensitivity Test discussed by Don Kinzer will help to determine if your memory is operating correctly.

If you need -12 or +15 V for your latest hardware design, and have only +5 V, what can you do? Read No Power for Your Interfaces? Build a 5 W DC to DC Converter by Steve Ciarcia. Several inexpensive, practical designs are described, to give you everything from -15 to +15 V from a +5 V source.

In Part 1 of A "Tiny" Pascal Compiler, in the September 1978 BYTE, Kin-Man Chung and Herbert Yuen described the syntax of a Pascal subset and described a hypothetical stack machine, called a p-machine. This month they describe a compiler that generates codes for the p-machine.

Would you like a fast and easy way to test your new memory board? Author Russell Adams shows you how in Testing Memory in BASIC. A simple program loads the memory locations with alternating 1s and Os to spot those bad bits.

The H8 computer from Heath features a novel firmware front panel monitor comprised of both hardware and software elements. Gordon Letwin, Heath software designer, describes the design philosophy and the features of the system in PAM/8:

Creating a Chess Player was written by two people at the forefront of research in computer chess: David Frey, editor of Chess Skill in Man and Machine, and Larry Atkins, coauthor of Chess 4.6, the world champion chess program that recently beat a Grandmaster in a simultaneous exhibition. The article discusses the thinking processes in the chessplayer’s mind and how such processes are transformed into a computer program.
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Finally, it had to happen to me. We all know that personal computers are supposed to be a cross between a necessity and a luxury. But the critics tend to harp on our tendency to get carried away by the fun and to ignore the practical uses of our wonderful servants. As if to answer that justified criticism, I finally came up with a genuine practical use for a small computer in the monthly operations of BYTE’s editorial office. Now this practical application is by no means the kind of automated editing and type preparation facility I would like to have some day if and when I ever become rich and famous. But this is a genuine, once a month, cyclically run application program.

At BYTE, we have so far purchased two Apple II computers (among others) for use in educating our employees, and in order to have some facilities around the office. One of these Apple II computers sits in my office, and at the time of this exercise...
More and more, you see the North Star HORIZON computer at work in business, research, and education. Its high performance qualifies the HORIZON for demanding professional applications. Over 10,000 users during the past two years have proven that North Star hardware has the reliability for day-in, day-out computing. The HORIZON is now a serious candidate for any small system installation.

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Well, the games part is true. The rest of the claims should be taken with a grain of salt. All of the personal computers will help you learn about computers and how they work in general and the kinds of things they can do for you. Only a few have the capacity to grow and handle meaningful work in a very real sense. And they don't come for peanuts.

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In sum, all small computers are not created equal and Sol users know it to their everlasting satisfaction.

Processor Technology
I enjoyed the article, "Top-Down Modular Programming," by Albert D. de Bea in July 1978 BYTE, page 32. I thought he did a good job of explaining the subject. While I realize that he was purposely trying to simplify matters, I do take exception to his comment that a module should be no more than 50 lines long.

The concepts of structured programming are intended as guidelines, not as the dogma for a programmer's religion. All of the better known proponents of the methodology stress this point, along with the idea that you must approach the study of structured programming with your eyes open, making your own evaluation. In this light I see the 50 line limit.

One of the bases for breaking a program up into modules is so that a complex problem can be handled with small, easy-to-understand pieces of code. One of the things about module size is, therefore, that a module ought to be able to fit on the printed page. This is so that all the information about the module is in one place and the programmer doesn't have to thumb through several pages to read the code for a single module. (Having experienced "modules" running as long as 10 to 15 pages, I heartily agree with this philosophy.)

In professional programming installations this idea has frequently been translated into a local standard of about 10 lines of code, since this is the length of lines which are printed on an 8½ by 11 inch (21.25 by 27.9 cm) page coming out of a line printer (allowing for headers, footers, etc). For the personal computer enthusiast, however, this limit might be more conveniently set at 24, 32 or 40 lines — the size of the video display.

For many more complex problems, it is possible that a significant module cannot be constructed in 24 lines. This is no problem — just make the modules longer. The point is to try to restrict the module size to a length which enhances the programmer's ability to understand the code.

The basics of structured programming must be studied, evaluated, and possibly modified to work in each individual situation. There are a lot of great ideas included in the structured programming lore, but they shouldn't be adopted blindly.
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Enough about us. How about what computers do. To attempt to describe all the things your computer might do, would be to describe your imagination. So instead, we'll briefly list some of the many things for which small computers are already being used.

In business, the advent of the versatile and compact microcomputer has put the benefits of computing within reach of small companies. With systems starting at less than $6000, the businessman can computerize things like accounting, inventory control, record keeping, word processing and more. The net result is the reduction of administrative overhead and the improvement of efficiency which allows the business to be managed more effectively.

In the home, a computer can be used for personal budgeting, tracking the stock market, evaluating investment opportunities, controlling heating to conserve energy, running security alarm systems, automating the garden's watering, storing recipes, designing challenging games, tutoring the children . . . and the list goes on.

In industry, the basic applications are in engineering development, process control, and scientific and analytical work. Users of microcomputers in industry have found them to be reliable, cost-effective tools which provide computing capability to many who would otherwise have to wait for time on a big computer, or work with no computer at all.

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A Memory Pattern Sensitivity Test

Don Kinzer
3885 NW Columbia Av
Portland OR 97229

Faulty memory is a very difficult problem to detect. Most distributors of memory board kits supply a simple memory test designed to detect assembly errors such as misplaced components, solder bridges, etc. These tests are ineffective in detecting certain types of memory related problems. One of these problems, called pattern sensitivity, manifests itself in the very disturbing fact that accessing one memory location alters another memory location, but only when the memory contains a certain pattern of bits.

It is my intention, through this article, to make the experimenter aware of potential memory problems and to provide some information which may be helpful in diagnosis of the problems by discussing a recent experience.

Every memory test is capable of detecting only a certain few of the many possible memory faults. Because of this, the user should be armed with a battery of memory tests and run them all at the first sign of trouble. Better yet, the tests could be run at regular intervals. A very good selection of such tests is contained in a package available from Technical Systems Consultants (POB 2574, W Lafayette IN 47906) as their SL68-23 Diagnostic Package. This package contains, among other tests, five memory tests, written in 6800 code, to expose bad bits, convergence problems, and some types of pattern sensitivity. This package is highly recommended for all system users as the tests can be rewritten for the user’s own machine.

As indicated before, the more tests, the better. The new test I am about to describe was discovered quite by accident. I was writing a resident assembler for my 6800 and was working on the sort routine which alphabetizes the symbol table. The sort, called a shell sort, works by comparing symbol table entries and exchanging them if they are not in alphabetical order. The process involves a tremendous amount of data shuffling. To my dismay, after the sort, the labels and their values had changed. TEMPl became TEMQl. Before the sort MASK was hexadecimal 3E; after the sort it was hexadecimal BE. Needless to say, I wasted a lot of time looking for a software bug before I decided to test the memory.

It occurred to me that writing a test program which operated in a manner similar to the sort routine would help track down

Listing 1: Memory E-CHANGE program written for the 6800 to test for memory pattern sensitivity.

```
E07E 9 DATA    ED7E
E0D1 10 OUTCH   ED67
E067 11 OUTHL   ED68
E068 12 CIINH   ED7E
8 * EXTERNAL ROUTINES (PUBLIC ROUTINES)

1 * EXCHANGE
2 * A MEMRNY TEST
3 *
4 *
5 *
6 *
7 *
8 *

0000 16 ORG 0
0000 17 BEGIN  RMB 2
0002 18 END    RMB 2
0004 19 XTMP1  RMB 2
0006 20 XTMP2  RMB 2
0008 21 DECNT  RMB 1
22 *
22 *
23 *
24 INIT   LDS #3F07F set up stack
25 START  JSR PCNF  go do our
26 LOOP   FSR  save starting point
27 LDX BEGIN get beginnig address
28 IX   adjust
29 INTLP INX point next location
30 STAB 0,0 initialize
31 ENC set next value
32 CPX   END see if done
33 BNE INTL if not, do again
34 *
35 *
36 BUBBLE STX XTMP2 save end pointer
37 END  XTMP2 HEGIN
38 EXCHG STX XTMP1 save top pointer
```

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Cirle 15 on inquiry card.

Apple's smart peripherals make expansion easy. Just plug 'em in and they're ready to run. I've already added two disks, a printer and the communications card.

---

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the trouble. The result is a program called EXCHANGE which is shown in listing 1.
The program works by initializing the memory to be tested to a sequence of
the 256 eight bit numbers. Then pointers are set to the beginning and end of that same
block of memory, XTEMP1 and XTEMP2 respectively. Next, the data at each of the
pointers is exchanged. The pointers are then moved toward one another. The process
of exchanging and moving repeats until the pointers meet. The inverted sequence is then
checked for accuracy. Any discrepancies are reported by printing the memory location
which is incorrect, the location where the data resided before the exchange, what the
data was supposed to be and what the data actually was.
The first time I ran the test, the program crashed. The memory problem had caused a
byte of the program to change. After several tries with the same results, I took my
machine to work and attached an oscilloscope to the data bus. I found that the data
lines had an unbelievable amount of noise. At the advice of a friend, I installed resistive
terminations on the data lines, which immediately cleaned up the signals. This
determined the majority of the memory problem and even allowed the EXCHANGE
program to run without crashing. Several hours of further testing using EXCHANGE
exposed three more malfunctioning 2102s in my 12 K byte system.

After all of this I am happy to say that the sort routine was in fact working properly.
Furthermore, the pattern sensitivity problem explains away several bugs in other
programs I have worked on.

Before closing I would like to offer a few pointers on using EXCHANGE. If you
suspect memory problems, run a bit test or convergence test to rule out physical
problems (like shorted wires) and bad bits (nonfunctioning memory parts). If the
problem persists, run EXCHANGE on the entire contiguous memory (except, of
course, where EXCHANGE is located) noting any errors as they are printed. Next, run
EXCHANGE on smaller areas corresponding to each set of 2102s. Replace the memory
chips as necessary but don't throw them away yet. If the memory is still bad in the
same area then the memory chips are not to blame and it is time to put an
oscilloscope on your system to see what the problem is.

Based on my own experience with a homebrew computer I recommend running a
battery of tests after any system hardware changes to uncover memory problems before
they turn up as a bug in your next program.
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<tr>
<td>C2-4P — The professional portable</td>
<td>4K RAM</td>
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<th>RAM</th>
<th>Price</th>
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<tr>
<td>C2-0 — Great starter for users with a terminal</td>
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<td>$ 298</td>
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<tr>
<td>C3-S1 — World’s most popular 8&quot; floppy based microcomputer</td>
<td>32K RAM</td>
<td>$ 3590</td>
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<tr>
<td>C3-OEM — Single package high volume user version of C3-S1</td>
<td>32K RAM</td>
<td>$ 3590</td>
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<tr>
<td>C3-A — Rack mounted multi-user business system directly expandable to C3-B</td>
<td>48K RAM</td>
<td>$ 5090</td>
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<td>48K RAM</td>
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Since its introduction in August, 1977, the Challenger III has gained tremendous acceptance in small business, educational and industrial development applications. Thousands of C3-S1's have been delivered and today hundreds of C3-S1 demonstrator units are set up at computer retailers around the country.

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- The Challenger III is the fastest microcomputer in BASIC (see "BASIC Timing Comparisons," Kilobaud, October, 1977, where Ohio Scientific out benchmarks all competitors).
- The Challenger III is the only computer system with a 6502A, 6800 and Z-80 offering the programmer all popular micros for maximum versatility.
- The C3 is backed by the largest base of systems level software for any microcomputer system including:
  - For the 6502A:
    - Microsoft 6 and 9 Digit BASIC
    - Assembler Editor
    - Word Processor
    - OS-65D Development DOS
    - OS-65U End User DOS with Extended BASIC
      - For Floppys
      - Winchester Hard Disks
      - Multi-users (Level 2)
      - Distributed Processing (Level 3)
  - For the 6800:
    - Floppy DOS
    - Assembler Editor
  - For the Z-80:
    - Floppy DOS
    - Microsoft Disk Extended BASIC
    - Microsoft FORTRAN
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    - Macro Assembler and Editor
    - And Much More
- The C3 supports OS-65U, the ultra high performance "virtual data memory" DOS for floppys and hard disks which makes complex file structures like multi-key ISAM easy to use.
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- The C3 electronics and software are available in alternate mechanical configurations for special applications including the C3-OEM for volume users and the C3 letter series (C3-A, C3-B) which are optimized for use with hard disks.
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- C3 systems have phenomenal performance-to-cost ratios. The C3-S1 base price with 32K RAM, dual floppys, RS-232 port complete with 8K BASIC and DOS is under $3600 and expansion accessories are comparably priced. For example, the CD-74, 74 million byte Winchester disk complete with interface and OS-65U operating system at about $6000.

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The C3-B was designed by Ohio Scientific as the state of art in small business computing. The system places its power where it's needed in the small business environment; in the data files. The C3-B's advanced Winchester technology disk, coupled with its smart controller and dedicated high speed memory channel, gives the C3-B data file performance comparable with today's most powerful maxi-computers.

Yet, the C3-B costs only slightly more than many floppy only computers but offers at least a thousand times performance improvement over such machines (50 times storage capacity multiplied by 20 times access speed improvement).

But what if your business client cannot justify starting with a C3-B? Then start with Ohio Scientific's inexpensive C3-S1 floppy disk based system running OS-65U. When he is ready, add the CD-74 big disk and directly transfer programs and files from floppy to big disk with NO modifications.

That's upward expandability!

* Rack as shown above complete with 74 megabyte disk, dual floppy, 48K of static RAM, OS-65U operating system and one CRT terminal under $13,000.

Multiple terminal systems with printers and applications software are priced in the mid-20's.
Photo 1: 5 W DC to DC converter, which produces 0.2 A at +12 and −12 VDC from a 5 VDC source. The circuit uses a special custom wound toroidal transformer (see figures 5a and 5b). Note: the prototype shown uses 1000 µF 25 V capacitors, which were later replaced with 100 µF 25 V versions.

Build a 5 W DC to DC Converter

Steve Ciarcia
POB 582
Glastonbury CT 06033

Recently I attended a local computer club meeting where we discussed the question of power supplies. Many people were remarking that, while they enjoyed building the projects in my articles, often their power supplies were not compatible with the multiple voltages I required. Many of the newer single board computers that some members owned contained only a hefty +5 V supply and a note that the user should add additional supplies if the basic board is expanded.

This is not an industry copout by any means. The newest digital designs from companies like Intel are made to run on +5 V and this is considered an advance in technology. The 8080A processor requires +12, +5 and −5 V for operation, while the new 8085 uses only a single +5 V supply. As long as all other components such as universal asynchronous receiver-transmitters (UARTs), programmable memories, erasable read only memories (E-EROMs) and read only memories (ROMs) in the computer are all +5 V, we can eliminate additional power supplies and save money. Computer manufacturers have done just that.

This situation does not cause any problems as long as the user stays with the basic unit, or expands it using single +5 V supply devices. Erasable read only memories such as the Intel 2716 and programmable peripheral interfaces such as the 8255 are designed specifically for this application.

The problem arises when the single supply computer tries to be communications compatible with the rest of the world, or when a bipolar analog interface is added. The RS-232C interface generally requires + and −12 V potentials, and digital to analog converters such as the Motorola 1408L8, which run on +5 and −12 to −15 V.

The Whole World Isn't TTL Compatible

What is the experimenter to do when a −15 V supply is needed and the computer has only +5 V, or when one wishes to tie an RS-232 terminal into a system? Obviously the answer is to add an additional power supply or two—but, what kind?

Power supply requirements should be based on load requirements. If 0.5 A at +15 V is needed to power a particular interface, then perhaps a 1 A traditional transformer-rectifier-filter-regulator design is in order. More often than not, though, the interface might use one or two dual supply
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Figure 1: Typical DC to DC converter, a device used to convert one DC voltage into another. The oscillator section supplies a train of square waves to the buffer drivers. On the first half cycle, capacitor C1 is charged to approximately 4 V, and on the second half cycle, C2 is charged to -4 V. The voltage across the two capacitors is twice the input voltage, or approximately 8 V (open circuit). The 1 mF capacitor between IC1d and the two diodes isolates the circuit so that the 8 V can be referenced to ground.

integrated circuits and require only 50 mA, or if the interface is designed with CMOS circuitry, the current requirement could be 5 mA or less. While the 60 Hz transformer design may be more than adequate, the volume and weight of the low frequency magnetics is bulky and may not fit easily within the present enclosure.

The DC to DC Converter

In an application that requires higher voltage at low current, the DC to DC converter is the natural choice for the designer. As its name implies, it converts one DC voltage to another, usually a higher one. All DC to DC converters incorporate oscillator sections to provide AC either to drive transformers or to drive diode-capacitor voltage multipliers. The converters operate at high frequencies to reduce transformer weight. We’ll explore the particulars later.

A DC to DC converter need not be low power, but the designs and applications presented here are specifically for low current and limited space applications. The majority of the circuits occupy less than 2 square inches (12.9 square cm).

A DC to DC converter draws its power from some major power bus, such as a +5 V or +12 V computer supply, and converts this source voltage to a higher level of either the same or reversed polarity. The simplest configuration is shown in figure 1. IC1a and IC1b form the oscillator which is common to all DC to DC converters. IC1c, IC1d and IC1e are buffers with the outputs of IC1d and IC1e 180 degrees out of phase,

Figure 2: A CMOS DC to DC converter used for low current applications. This circuit produces -15 V from a +15 V source and provides a relatively constant output voltage because of the shunt regulator formed by diodes D1 and Q1.
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Most often DC to DC supplies are used where a negative voltage is required to power a bipolar linear interface or a dual supply large scale integrated circuit such as a keyboard encoder.

Figures 2 and 3 are examples of converters which would be suitable for these low current applications. Figure 2 produces $-15\,\text{V}$ from a $+15\,\text{V}$ source and provides a relatively constant output voltage because of the shunt regulator formed by the diode, D1, and the transistor, Q1. Changing the zener diode, D1, to $13\,\text{V}$ makes the output $-12\,\text{V}$ instead of $-15\,\text{V}$.

The circuit outlined in figure 3 uses the voltage control input of an NE555 timer circuit to produce a variable output of $0$ to $-10\,\text{V}$.

**Inverting Supplies**

In most cases single voltage converters use diode steering and charged capacitor voltage multiplication. Transformers or other inductive devices must be incorporated if dual outputs are a requirement. Figure 4 is a very simple $\pm15\,\text{V}$ converter which is powered from a $+5\,\text{V}$ supply.
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Figure 5a: 5 W DC to DC converter pictured in photo 1, which produces 0.2 A at +12 and -12 V from a 5 V source. See figure 5b for details of winding a toroidal transformer for this circuit.

1. Q1 and Q2 are General Electric type D44H4 transistors (or equivalent).
2. TI 88 millihenry toroid (see text).
3. All resistors ¼ W 5%.
4. All capacitors are 100 V ceramic unless otherwise marked.

Figure 5b: Toroid winding details for the custom transformer used in the circuit of figure 5a (see photos 2 thru 5).

<table>
<thead>
<tr>
<th>Number</th>
<th>Type</th>
<th>+5 V</th>
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<tbody>
<tr>
<td>IC1</td>
<td>7404</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC2</td>
<td>74004</td>
<td>14</td>
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<td>IC3</td>
<td>555</td>
<td>8</td>
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<td>IC5</td>
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</tr>
<tr>
<td>IC6</td>
<td>7437</td>
<td>14</td>
<td>7</td>
</tr>
</tbody>
</table>

Table 2: Power wiring table for figures 1 thru 5.

A 100 kHz oscillator switches a transistor on and off, inducing a current into the primary of transformer, T1. The voltage produced at the secondary is rectified and regulated to -15 V.

As with all inductive devices which are pulsed, a high voltage spike is reflected back to the collector of the transistor. Rather than shunting this voltage, as would be the case when we put a diode across a coil, D1 routes this spike to a filter and regulator combination to provide a +15 V output.

Building a DC to DC Converter

One of the first things to determine after deciding to use a DC to DC converter in your system is just how much current it must provide. Table 1 lists the typical voltages and operating current requirements (worst case) of a sampling of devices.

It should be apparent from this listing that EROMs are power-hungry devices and will use more than the 10 mA that the converters discussed thus far can supply. For this reason the unit described in figure 5 is designed to produce a full 200 mA at ±12 V.

This design uses a push/pull inverter technique to create AC which drives transformer, T1. T1 is a toroid transformer and

Photo 2: Surplus 88 millihenry toroidal transformer rewound with two secondaries of 175 turns of #26 wire each (after first unwinding the existing two windings of approximately 350 turns each). The unit is used in the circuit of figure 5a.
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its doughnut shape is quite unlike the more common rectangular filament transformers. The shape and style of the toroid are specifically designed for high frequency operation, which is the main attribute of this inverter design. Heavy magnetic cores are necessary only for low frequencies such as 60 Hz. Since this converter's switching speed is 20 kHz, relatively little magnetic material is necessary, and high power output can be obtained.

The toroid in this design is a surplus 88 millihenry toroid, frequently advertised in the amateur radio magazines. A source I have found is: M Weinschenker, POB 353, Irwin PA 15642. Order 88 millihenry unpotted toroids. The price is five for $2.95 plus $1 postage.

There are two ways to wind this toroid. Since it presently contains two windings of approximately 350 turns each, adding a primary sounds most logical. In reality though, 180 turns of #20 wire couldn't possibly fit in the remaining space, and the number of windings seems to vary from source to source. To obtain a properly wound toroid, it is best to first completely unwind the toroid and then rewind two 175 turn secondaries. The rewound toroid looks like photo 2. Since inductors exhibit an output polarity that is important when tying two secondaries in series, it is advisable to

---

*Photo 3: Adding the primary winding, step 1: wind 40 turns of #20 wire evenly around the toroid.*

*Photo 4: Adding the primary winding, step 2: make a loop for the center tap and continue with 40 additional turns.*

*Photo 5: The completed transformer. The ends of all enameled wires should be cleaned of insulation before soldering.*
mark the starting lead on each coil and wind each in the same direction. It is not catas-

trophic if you don’t. Polarity can be deter-

mined empirically later.

The primary is wound with #20 wire over the two secondaries as in photo 3, and should be distributed evenly around the toroid. When 40 turns have been wound, make a loop in the wire so that it will stick out (as shown in photo 4) and then continue winding the next 40 turns in the same direction. The complete toroid should look like photo 5.

The design outlined in figure 5a is a DC inverter. The NE555 20 kHz oscillator sources the high current 7437 buffers which are necessary to drive the push/pull transistor combination of Q1 and Q2. The continuous on/off action of the transistors produces an alternating current of 20 kHz in the primary winding of the toroid. This in turn induces a voltage proportional to the ratio of the primary to secondary turns, times the primary input voltage into the secondary winding. With approximately 4 V into the primary (taking into account the collector to emitter voltage drop, V_{CE}, transists Q1 and Q2), 18 to 20 V should be present on each secondary.

The output of the toroid is treated as it would be in a traditional DC regulator design. The two secondaries are connected in series (terminals 5 and 6 connected) to produce 45 V between terminals 4 and 7. If a low voltage is obtained instead of 45 V, then the secondaries are out of phase and the terminals of one of the coils should be reversed. The two terminals which are connected at this point are the center tap and should be grounded.

Four diodes and two capacitors function as the full wave rectifier and filter input to a pair of 3 terminal voltage regulators. The result is a well-regulated + and -12 V supply with output current in excess of 200 mA on each. Overall conversion efficiency is better than 50%.

One note to keep in mind when testing this device: since the output is 5 W with 50% efficiency, the continuous input current to the converter will be approximately 2 A (at 5 V). Peak current will be higher at each clock transition. Use a supply with sufficient current capabilities or it will degrade the performance of the converter and possibly not even work.

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When Niklaus Wirth introduced Pascal in 1971, one of the design objectives was to allow efficient program compilation. As far as we know, all existing Pascal compilers use the one pass compilation technique.

Newcomers to Pascal sometimes criticize features of the language such as declaring variables before use, and having constant and type declarations precede variable declarations. But such features are necessary to make a one pass compiler work (aside from the fact that it is also good programming practice to declare identifiers before use). Compared with multipass compilers, the job of writing a one pass compiler is relatively simple, since there is no need to store the program in its intermediate form.

Figure 1 shows the structure of our one pass Pascal compiler. The main portion is made up of the scanner, syntax analyzer, semantic analyzer and code generator. A brief overview of these functional portions of the compiler follows. Detailed descriptions will be given later.

The syntax analyzer is commonly called the parser. Its main function is to detect syntactical errors in the source program. The smallest unit of the source program that the parser looks at is called a token. For instance, the reserved word while, the symbol :=, or the identifier idname would be tokens. The main job of the scanner is to read the source program and output a token when needed by the parser. Irrelevant information such as blanks, comments and line boundaries are ignored.

To further simplify the work of the parser, the values of numeric constants are also evaluated by the scanner. The parser then parses the program according to the rules laid down by the syntax diagrams which were described in part 1 (“A Tiny Pascal Compiler,” September 1978 BYTE, page 58) and generates error messages if illegal constructs are found. Identifier names are entered into a symbol table as they are declared. The symbol table is consulted by the parser as well as the semantic analyzer. After a Pascal construct is recognized, its meaning is analyzed by the semantic analyzer and appropriate p-codes are generated. Occasionally, there are forward references whose addresses cannot be determined at the time the codes are generated, but have to be resolved at a later time. Thus updates to the object program have to be done at the appropriate time.

This may sound complicated, but in fact a one pass compiler is actually the simplest compiler imaginable. The technique used by our parser is usually referred to as top-down parsing or goal oriented parsing. The top-down parsing algorithm assumes a general goal at the beginning. This goal is then broken down into one or more subgoals, depending on input strings and the rules in the syntax diagrams. The subgoals are realized by breaking them down into finer subgoals.

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Listing 1: BASIC version of the p-compiler. This program takes the Pascal program and compiles it into p-code. The term p-code stands for pseudocode, an assembler language code for a hypothetical computer which can be converted into an existing assembler language. Listing continues thru page 48.

A top-down parser without backup can be implemented by using a technique called recursive descent. Such a parser uses a recursive procedure for each nonterminal in the syntax diagrams. A call is made to this procedure whenever a parse for such after some processing that we have made the wrong choice. We would then have to undo what had been done by the wrong choice and back up to the point where we could try other alternatives. This is usually a messy business and involves a lot of bookkeeping. Fortunately, in the parsing of Pascal, no backup is necessary. A keyword is present at each decision point, and it determines what subgoal we should choose. An example will make this clear.

Suppose our goal is to recognize a statement. A statement can be a number of basic constructs: it can be an assignment statement, an if statement, a case statement or any other construct defined by the syntax diagram. The Pascal grammar is so designed that we know which type of statement we should choose by just looking at the next token. If the token is if, then we know it is going to be an if statement; if the token is case, it is going to be a case statement, etc. There would seem to be a problem if the token is an identifier, since the statement can be the beginning of an assignment statement or a procedure call. But this can be easily resolved by consulting the symbol table, where we also keep the attributes (data types, addresses, etc) of the identifiers. This is one of the reasons why identifiers and procedures must be declared before use: it makes compiler writing easier.

<table>
<thead>
<tr>
<th>Line</th>
<th>Number</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>370</td>
<td>1950</td>
<td>Enter entry into symbol table</td>
</tr>
<tr>
<td>380</td>
<td>2060</td>
<td>Search symbol table</td>
</tr>
<tr>
<td>400</td>
<td>2170</td>
<td>Constant declaration</td>
</tr>
<tr>
<td>470</td>
<td>2240</td>
<td>Get constant</td>
</tr>
<tr>
<td>480</td>
<td>2340</td>
<td>Variable declaration</td>
</tr>
<tr>
<td>490</td>
<td>2380</td>
<td>Simple expression</td>
</tr>
<tr>
<td>500</td>
<td>2610</td>
<td>Term</td>
</tr>
<tr>
<td>510</td>
<td>2650</td>
<td>Factor</td>
</tr>
<tr>
<td>520</td>
<td>2850</td>
<td>Expression</td>
</tr>
<tr>
<td>530</td>
<td>3290</td>
<td>Statement</td>
</tr>
<tr>
<td>540</td>
<td>3490</td>
<td>Block</td>
</tr>
<tr>
<td>550</td>
<td>5340</td>
<td>Error routines</td>
</tr>
<tr>
<td>560</td>
<td>5360</td>
<td>Print error msg</td>
</tr>
<tr>
<td>570</td>
<td>5500</td>
<td>Error routines</td>
</tr>
<tr>
<td>580</td>
<td>5600</td>
<td>Print error msg</td>
</tr>
<tr>
<td>590</td>
<td>5700</td>
<td>Enter a line</td>
</tr>
<tr>
<td>600</td>
<td>5800</td>
<td>Search symbol table</td>
</tr>
<tr>
<td>610</td>
<td>5900</td>
<td>Get constant</td>
</tr>
<tr>
<td>620</td>
<td>6000</td>
<td>Variable declaration</td>
</tr>
<tr>
<td>630</td>
<td>6100</td>
<td>Simple expression</td>
</tr>
<tr>
<td>640</td>
<td>6200</td>
<td>Term</td>
</tr>
<tr>
<td>650</td>
<td>6300</td>
<td>Factor</td>
</tr>
<tr>
<td>660</td>
<td>6400</td>
<td>Expression</td>
</tr>
<tr>
<td>670</td>
<td>6500</td>
<td>Statement</td>
</tr>
<tr>
<td>680</td>
<td>6600</td>
<td>Block</td>
</tr>
<tr>
<td>690</td>
<td>6700</td>
<td>Error routines</td>
</tr>
<tr>
<td>700</td>
<td>6800</td>
<td>Print error msg</td>
</tr>
<tr>
<td>710</td>
<td>6900</td>
<td>Enter a line</td>
</tr>
<tr>
<td>720</td>
<td>7000</td>
<td>Search symbol table</td>
</tr>
<tr>
<td>730</td>
<td>7100</td>
<td>Get constant</td>
</tr>
<tr>
<td>740</td>
<td>7200</td>
<td>Variable declaration</td>
</tr>
<tr>
<td>750</td>
<td>7300</td>
<td>Simple expression</td>
</tr>
<tr>
<td>760</td>
<td>7400</td>
<td>Term</td>
</tr>
<tr>
<td>770</td>
<td>7500</td>
<td>Factor</td>
</tr>
<tr>
<td>780</td>
<td>7600</td>
<td>Expression</td>
</tr>
<tr>
<td>790</td>
<td>7700</td>
<td>Statement</td>
</tr>
<tr>
<td>800</td>
<td>7800</td>
<td>Block</td>
</tr>
<tr>
<td>810</td>
<td>7900</td>
<td>Error routines</td>
</tr>
<tr>
<td>820</td>
<td>8000</td>
<td>Print error msg</td>
</tr>
<tr>
<td>830</td>
<td>8100</td>
<td>Enter a line</td>
</tr>
<tr>
<td>840</td>
<td>8200</td>
<td>Search symbol table</td>
</tr>
<tr>
<td>850</td>
<td>8300</td>
<td>Get constant</td>
</tr>
<tr>
<td>860</td>
<td>8400</td>
<td>Variable declaration</td>
</tr>
<tr>
<td>870</td>
<td>8500</td>
<td>Simple expression</td>
</tr>
<tr>
<td>880</td>
<td>8600</td>
<td>Term</td>
</tr>
<tr>
<td>890</td>
<td>8700</td>
<td>Factor</td>
</tr>
</tbody>
</table>

Table 1: For easy reference the main subroutines of the p-compiler are listed here along with remarks regarding their uses.
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a nonterminal is required. It is easy to see why such a scheme would work. The stacking mechanism of the run time procedures ensures that we get back to the correct position in the syntax diagram after completing the parse of the nonterminal.

If you look at the syntax diagrams carefully, you will see that diagrams for certain nonterminals actually contain the nonterminal itself, either immediately or after several expansions. In terms of compiler writing this means that the procedures corresponding to these nonterminals would call themselves recursively.

### BASIC Recursive Subroutines

Most versions of BASIC do not adequately support recursive subroutine calls. In North Star BASIC, the multiline function call can be invoked recursively, in a limited fashion. This is because the function parameters are local within the function definition and are pushed onto a stack when making a call.

The surprising fact is that most BASICS do not forbid a recursive call if one is made. For instance, the following BASIC subroutine, which is an inefficient way of printing the first N integers in descending order, is probably permitted in most BASICS:

```
100 PRINT N
200 IF N=0 THEN RETURN
300 N=N-1
400 GOSUB 100
500 RETURN
```

The problem of doing recursive calls in BASIC is that of preserving the values of the identifiers in the subroutines. This can be done by using a stack. The values of the identifiers are pushed onto the stack before a recursive call, and popped out of the stack in the reverse order when returning from the call. In BASIC, the stack can be simulated by an array:

```
10 DIM S(100)
11 P=0
12 REM INITIALIZE STACK POINTER
   :   :   :
1000 REM PUSH X INTO STACK
1010 S(P)=X
1020 P=P+1
1030 RETURN
1040 X=S(P-1)
```

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It is generally difficult to implement a compiler with sophisticated error recovery features. Such a compiler would not only detect errors, but would also try to repair the damages caused by such errors. The compiler has to make some assumptions about the nature of the errors and the intention of the author. This is usually difficult.

If our concern is solely that of locating all errors in a single parse of the source program, there are simple ways of doing it. Upon detecting an error, the compiler simply skips the input text until it can safely resume the compilation process. To do this the compiler looks for certain keywords or stopping symbols for hints to resume the parsing process. For instance, if we find an error while parsing a conditional expression, we simply skip the input tokens and search for such as then and do or perhaps begin. If we do this for all the parts of the language constructs, we will at least have a compiler that would resume compilation after an error is encountered in the hope of finding all syntactic errors in one pass, and which would give meaningful diagnostics for most errors.

To reduce the size of the program shown in listing 1, comments are kept to a minimum. Each module or subroutine is clearly identified. To facilitate easy reference, the important subroutines and variables are shown in table 1 and table 2, respectively.

Scanner and Symbol Table Management

Each time the p-compiler calls the scanner (line 1260, listing 1), the input text is scanned and a new token is produced. This is done by calling a subroutine (line 1040) that returns a character from the input string. Since the input/output (IO) routines are line oriented instead of character oriented, a line buffer (L$) is used to
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In our compiler we also provide the capability of invoking or recalling a file of Pascal text from disk. This is initiated by a command that starts with a dollar sign ($) in the first column followed immediately by the name of the disk file to be inserted and compiled. Since North Star BASIC allows four disk files to be open at the same time, there can be four levels of file nesting. The variable FS is used to indicate this level. If it is equal to -1, then input is taken from the keyboard. The initial input is from the keyboard. This feature is quite useful, since we can store procedures that are commonly used in a disk library, and have them recalled when needed.

Usually, the token that the scanner returns is a number that represents the token class the symbol is in. To make the program more readable, we use string variable $0$. Possible values returned by the scanner are: :, :=, BEGIN, IDENT, and NUM. The last two tokens, which are tokens for identifiers and numbers, require some further information. A$ and N3 are also used to store the textual representation of the identifier and the value of the number, respectively.

The recognition of a valid token is a straightforward process and will not be detailed here. Since := and := are both valid tokens, the scanner, after seeing the :=, must also look at the next character to determine the correct token. This can be done by using a one character look ahead. When the scanner is entered, a character is assumed to have been read, and upon exit from the scanner, a character beyond the current token is read.

Another problem that the scanner may have is that of recognizing reserved words. The reserved words are stored in a table in sorted order. When an identifier is found, it is compared with the entries in the table, by performing a binary search. If it is not in the table, it is assumed to be a user defined identifier.
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Figure 2: Example symbol table at various points of compilation.
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for each type of identifier. For constants, the information is the values of the constants; for program variables, the information is the address pair (level, offset from base address); for procedures and functions, it is the address pairs and the number of parameters; and, lastly, for array variables, the information is the address pair as well as array sizes. See table 2 for actual variables that are used to store these quantities.

The symbol table is used by both the parser and the semantic analyzer. The information in the symbol table is used in a number of ways. The type of identifier is used, for instance, to check the type consistency in an expression. When a variable is referenced or a procedure or function called, the symbol table is searched to obtain the level and relative address from the base address. The number of parameters in a procedure or function is used to check the correct matching of parameters in actual procedure or function calls.

An identifier is searched for by starting from the end of the symbol table and working towards the beginning. (Viewing the table as a stack, we say that we search from the top of the stack down to the bottom.) There are two reasons for this searching direction. First, identifiers in the current block are more likely to be referenced and should be searched first. Secondly, suppose that a variable X is declared in both an outer and an inner block: by searching for X from top to bottom of the stack, we can be sure that we will find X of the inner block first, in accordance with the scope rule.

Parser, Semantic Analyzer, and Coder

The parser, the semantic analyzer and the coder are not separate routines, but are intermixed in a large routine. In most cases, after the successful parsing of a statement, its meaning is also understood by the compiler. Thus the semantic analyzer either requires minimal extra processing or is implicit in the parser and disappears altogether.

The parser, as we have mentioned before, uses a top-down technique called recursive descent. Since there is a close correspondence between the parser and the syntax diagrams of the Pascal grammar, there should be no difficulties in understanding the parsing process. The parser adopts the convention of one token look ahead which is similar to the one character look ahead convention used by the scanner. The variable $S_{0}$ is used to hold the next token to be read by the parser.

There is a part of the Pascal grammar, commonly referred to as the dangling
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The code generator requires more work: care must be taken to store important values in stacks due to the inability of BASIC to fully support recursive subroutine calls. Otherwise the coder is more or less straightforward, since the p-codes are so designed (see part 1) that there is a direct correspondence between simple Pascal statements and p-codes. Table 3 shows the almost direct translation of Pascal statements into p-codes.

The declarative statements (const, var, proc, and func) do not produce any executable statements; they merely provide information about declared identifiers. The first executable code encountered when entering a procedure or function block is a forward jump instruction to the main body of the block. This jump is necessary since in general there may be procedures and func-
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Listing 2: Sample Pascal program with compiled p-code. The number at the beginning of each source line is the offset of the corresponding p-code from the base address.

```
<table>
<thead>
<tr>
<th>Variable</th>
<th>Name</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A$</td>
<td>String of the token returned by the scanner</td>
</tr>
<tr>
<td></td>
<td>C0</td>
<td>Input buffer pointer</td>
</tr>
<tr>
<td></td>
<td>C1</td>
<td>P-code address pointer</td>
</tr>
<tr>
<td></td>
<td>D0</td>
<td>Run time storage counter</td>
</tr>
<tr>
<td></td>
<td>E9</td>
<td>Error code</td>
</tr>
<tr>
<td></td>
<td>F5</td>
<td>Active input file unit number; keyboard=1</td>
</tr>
<tr>
<td></td>
<td>K1</td>
<td>Number of parameter in the previous block</td>
</tr>
<tr>
<td></td>
<td>L0</td>
<td>Length of the input line</td>
</tr>
<tr>
<td></td>
<td>L1</td>
<td>Static level of procedure</td>
</tr>
<tr>
<td></td>
<td>L5</td>
<td>Input line buffer</td>
</tr>
<tr>
<td></td>
<td>M$</td>
<td>P-code mnemonics</td>
</tr>
<tr>
<td></td>
<td>N0</td>
<td>Reserved word table size</td>
</tr>
<tr>
<td></td>
<td>N1</td>
<td>Largest integer</td>
</tr>
<tr>
<td></td>
<td>N2</td>
<td>Length of identifier name</td>
</tr>
<tr>
<td></td>
<td>N3</td>
<td>Numeric value of token (token = &quot;NUM&quot;) or ASCII value of string token = &quot;STR&quot;</td>
</tr>
<tr>
<td></td>
<td>N4</td>
<td>Stack pointer for $S$</td>
</tr>
<tr>
<td></td>
<td>N5</td>
<td>Stack for numeric values</td>
</tr>
<tr>
<td></td>
<td>N6</td>
<td>Stack pointer for $S$</td>
</tr>
<tr>
<td></td>
<td>N7</td>
<td>Stack for strings</td>
</tr>
<tr>
<td></td>
<td>N8</td>
<td>Next token</td>
</tr>
<tr>
<td></td>
<td>T0</td>
<td>Symbol table size</td>
</tr>
<tr>
<td></td>
<td>T1</td>
<td>Symbol table pointer</td>
</tr>
<tr>
<td></td>
<td>T8</td>
<td>Symbol table identifier</td>
</tr>
<tr>
<td></td>
<td>T0S</td>
<td>Symbol table: type of identifier</td>
</tr>
<tr>
<td></td>
<td>T1( )</td>
<td>Symbol table: level</td>
</tr>
<tr>
<td></td>
<td>T2( )</td>
<td>Symbol table: value (constant)</td>
</tr>
<tr>
<td></td>
<td>T3( )</td>
<td>Symbol table: array size (array)</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>Value to be pushed or popped</td>
</tr>
<tr>
<td></td>
<td>XS</td>
<td>Next character to be read by the scanner</td>
</tr>
<tr>
<td></td>
<td>W0R</td>
<td>String to be pushed or popped</td>
</tr>
<tr>
<td></td>
<td>W0S</td>
<td>Table for reserved words</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

Table 2: Important variables used in the p-compiler.

Note that no space is allocated for constants. If a constant is referenced, a load literal (LIT) instruction is generated instead of a load (LOO) instruction. Also note that the procedure or function parameters and the function return value do not reserve any space in the procedure or function block called. Space is reserved before the call is made. Therefore, these values have negative displacement from the base address of the called procedure or function.

When a call is made to a function, the space for function return value is allocated by incrementing the stack pointer (line 2980 in listing 1) (this step is skipped for a procedure call). The parameter expression is then evaluated (line 4250), putting the resultant value on the stack. Thus, space is allocated for each parameter and initialized with the value of the parameter expression. Upon return from a procedure, the stack pointer is decremented by an amount equal to the space allocated for the parameters, returning the stack to its state just before the call.

Note also that no space is allocated for constants. If a constant is referenced, a load literal (LIT) instruction is generated instead of a load (LOO) instruction. Also note that the procedure or function parameters and the function return value do not reserve any space in the procedure or function block called. Space is reserved before the call is made. Therefore, these values have negative displacement from the base address of the called procedure or function.

When a call is made to a function, the space for function return value is allocated by incrementing the stack pointer (line 2980 in listing 1) (this step is skipped for a procedure call). The parameter expression is then evaluated (line 4250), putting the resultant value on the stack. Thus, space is allocated for each parameter and initialized with the value of the parameter expression. Upon return from a procedure, the stack pointer is decremented by an amount equal to the space allocated.

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### REFERENCES


### Table 3: Code generation for various Pascal constructs. For readability, the p-codes are given in assembly form. The italic identifiers in the Pascal statements are nonterminals that can be substituted by any valid expansion. The codes for these quantities are represented by parenthesized identifiers.

<table>
<thead>
<tr>
<th>Pascal source</th>
<th>p-codes</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>x+10*y[5]</code></td>
<td><code>LOD X 10</code></td>
</tr>
<tr>
<td><code>a:=exp;</code></td>
<td><code>LIT 5</code></td>
</tr>
<tr>
<td><code>if exp then stm1 else stm2;</code></td>
<td><code>OPR exp</code></td>
</tr>
<tr>
<td><code>for i:=exp1 to exp2 do stm;</code></td>
<td><code>STO A</code></td>
</tr>
<tr>
<td><code>while exp do stm;</code></td>
<td><code>JPC (stm1)</code></td>
</tr>
<tr>
<td><code>case exp of</code></td>
<td><code>JPC (stm2)</code></td>
</tr>
<tr>
<td><code>c1b1,c1b2:stm1;</code></td>
<td><code>1b1 JPC</code></td>
</tr>
<tr>
<td><code>c1b3; :stm2;</code></td>
<td><code>1b2 INT</code></td>
</tr>
<tr>
<td><code>else :stm3;</code></td>
<td><code>1b1 (exp)</code></td>
</tr>
<tr>
<td><code>end;</code></td>
<td><code>1b1 INT</code></td>
</tr>
<tr>
<td><code>repeat stm until exp;</code></td>
<td><code>1b2 ... (exp)</code></td>
</tr>
<tr>
<td><code>i:=func(a,exp1,exp2);</code></td>
<td><code>1b3 INT</code></td>
</tr>
</tbody>
</table>

for the parameters, getting back to the state before the procedure call. Upon returning from a function call, the stack pointer is also decremented by the same amount, but since a space has been allocated before the function call, the function return value is now on top of the stack, ready for further processing. This simple scheme works very efficiently and should lower the overhead usually associated with procedure or subroutine calls.

Listing 2 gives an output from the compiler for a Pascal program that prints out the maximum of four numbers. There are of course better ways of writing the program, but it does illustrate some ideas of the compiler discussed so far.

There is no optimization of the p-codes produced. Limited optimization can be done on the local level, and some optimization is actually done in the p-code to machine code translator. The problem of producing efficient codes is a difficult one, and is not addressed properly in our project. Given the simplicity of the p-machine and p-code, the p-compiler is efficient. But whether the combination of p-compiler and translator produces efficient 8080 code is uncertain.

This completes our discussion of the p-compiler. In part 3 (see November 1978 BYTE), we give a detailed discussion of a translator for converting the p-code into executable 8080 machine code.
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There are six parts to the book. The first introduces numbers systems and the second introduces the high level language which is used throughout the rest of the book. The third discusses techniques for programming various types of arithmetic such as multiple precision, floating point, etc. The fourth section introduces data structures and treats programming techniques for arrays, stacks, strings, chains, trees and graphs. The fifth part discusses techniques for searching with various structures; and the last part discusses sorting algorithms.

The book provides a good introduction and a reference to a number of programming techniques which are not dealt with in introductory programming texts. Most subjects discussed in Microprocessor Programming for Computer Hobbyists do not appear in the average BASIC or assembler text. Because the examples are given in a concise, high level language, they are easy to follow no matter what computer you have.

There are also several shortcomings to the book. First, I indicated that the examples are written in a superset of PL/M. I would have preferred the use of standard PL/M, since I have access to a PL/M cross compiler. Those who do not know PL/M will probably not suffer from this confusion. For the benefit of such readers, the book promises to show you how to translate between its high level language and your machine code, but this is hardly mentioned at all outside of the introduction.

All in all, this is a very good reference book. My only real quibble is that it uses a nonstandard high level language, and does not deliver all that it promises in the way of transferring this to a hobbyist computer.

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What Have You Found?

I would like to express my opinion about Mr O'Reilly's letter advocating the discovery and use of undefined op codes ("Instruction Search," May 1978 BYTE, page 153). Let me state what I think could be the reasons for the existence of undocumented op codes in a microprocessor instruction set:

- The op code was implemented unsuccessfully and under certain circumstances does not work correctly. The manufacturer was unable to justify correcting the problem, and chose to omit the instruction from the documentation.
- The instruction is an accident, an artifact of the specific implementation. It will work on some devices, but perhaps not on devices from a second source or even from another production run from the same vendor.
- The documentation of the instruction was accidentally left out. In this case, the vendor should have already issued corrections to the documentation, and you have not in fact disclosed any new information.
- The device you tested was defective. The feature does not work for anybody else.

Now I'm not out to criticize you for discovering new things about your processor; I'm just out to warn you that if the feature you think you have discovered is not acknowledged and supported by your vendor, you are taking a chance if you expect it to function correctly and to continue to be a feature in future versions of the processor.

If you refer to The Mythical Man-Month by Fred Brooks, you will find a revealing discussion of the consequences of the extra op codes on the IBM 7090. Brooks makes a very strong case for the significance of the "architecture specification" of a system, which states clearly what is to be expected of a piece of hardware, and equally clearly specifies those situations in which the results of an operation are "undefined." Briefly, the outcome of undefined operations is left up to the implementers, and may be chosen by them as they see fit. Cost, convenience and plain luck have much to do with the eventual results.
Testing Memory in BASIC

I hate to toggle in a program through the front panel of my computer. Yet every time I finish a new memory board I have to do this to a machine language memory test program. I therefore resolved to write a memory test program in BASIC which could be loaded with an 8 K interpreter in 8 K of proven memory. The BASIC program in listing 1 is the result.

The program is written in MITS 8 K version 4.0 BASIC and uses multiple statement lines with statements delimited by a colon (:). In addition to the normal functions of most BASICS, the program requires PEEK and POKE with arguments between 0 and 32767. In addition, the program needs the following BASIC primitives which may not exist on every system:

- CLEAR 80
- INPUT "... prompt. ...": USE PEEK and POKE with arguments between 0 and 32767. In addition, the program needs the following BASIC primitives which may not exist on every system:

**Listing 1: A BASIC memory test program. The memory to be tested is first loaded with the alternating patterns “01010101” and “10101010” in the even and odd memory locations, respectively. After testing all the locations, a second pattern (the logical inverse of the first) is loaded and tested. If any bit is influencing the state of an adjacent bit, the bad bit will be detected.**

```plaintext
0 REM ** BASIC MEMC~Y TEST REV.5 **
1 REM COPYRIGHT 1978 F.E. ADAMS
26 CLEAR 80
30 INPUT "START WITH BEGINNING OF PAGE": A
35 IF A<2 OR A>7 OR A<>INT(A) THEN PRINT "ERROR":GOTO 30
40 INPUT "END WITH END OF PAGE"; P
45 IF A<>INT(B) OR B<A OR B>7 THEN PRINT "ERROR":GOTO 40
60 P1=85: P2=170: GOSUB 300
70 R=8: X=GOSUB 300: S.
75 X=B: GOSUB 300: S.
80 PRINT: PRINT "TEST PATTERN 1 LOADING": PRINT
90 P1=170: P2=85: GOSUB 300
100 P1=85: P2=170: GOSUB 300
110 PRINT: PRINT "TEST PATTERN 2 LOADING": PRINT
120 R=8: X=GOSUB 300: S.
125 PRINT: PRINT "MEMORY TEST FROM "; X; " TO "; S; " OCTAL"
130 PRINT: PRINT "ADDRESS"," DATA"," SHOULD BE"
135 GOSUB 350
140 PRINT: PRINT "TEST COMPLETED"
150 END

300 FOR I=A TO 8-1 STEP 2
305 POKE I, P1: POKE I+1, P2
310 NEXT I
320 RETURN

350 FOR I=A TO 8-1 STEP 2
355 Z=PEEK(I): IF Z<>D THEN GOSUB 365
365 X=D: Y=Z: GOSUB 300: S.
370 IF X<>Y THEN PRINT "BAD BITS DETECTED"
380 NEXT I
390 IF LEN(DS)<>8 THEN DS="O"+DS: GOTO 390
400 PRINT "BAD BITS DETECTED"
410 RETURN

500 NS="";
505 K=INT(X/R): L=Z-X*R
510 NS=RIGHT$(STR$(L, 1))+NS
515 IF K<>0 THEN X=X-K*GOTO 505
520 RETURN
525 OK
```

The program has two parts: lines 25 to 130 contain the main program, while lines 300 to 520 contain four subroutines. Subroutine 300 loads a test pattern into memory; subroutine 350 reads back the data in memory and compares it to what the data should be; subroutine 365 prints out the bad address and the data; and subroutine 500 converts a base ten number into a base R number.

The memory under test is subjected to two test patterns. The memory is first loaded with the alternating pattern 0101-0101, 10101010, the first byte being placed in all the even addresses and the second being placed in all the odd addresses. After reading and comparing the first pattern, the second pattern is loaded. The second pattern consists of 10101010 loaded in all the even addresses and 01010101 in all the odd addresses. This alternating pattern is used so that if a bit is influencing the state of another adjacent bit, the bad bit will be detected (the pattern assumes that adjacent addresses are physically wired up as in the memory parts specifications). The BASIC interpreter must be limited to the lowest 8 K of memory. In MITS 8 K you answer the initial dialog MEMORY SIZE? with 8191. Also the trigonometric functions must be deleted. The program asks which pages of memory are under test. The first 4 K of memory is defined as page 0 and the last 4 K of memory is defined as page 15. The memory under test must be addressed between page 2 and 7, inclusive. This is sufficient space to test six 4 K boards, three 8 K boards, or one 16 K board.

The program takes about two minutes
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to test 4 K of memory. A sample printout
is shown in listing 2. The program first asks
the questions START WITH BEGINNING
OF PAGE? and END WITH END OF
PAGE?. These questions are answered with
the appropriate page numbers of the
memory under test. The program then
prints TEST PATTERN #1 LOADING
and starts loading the memory with the
first test pattern. Next, the two lines
MEMORY TEST #1 FROM TO
OCTAL and the headings ADDRESS,
DATA, and SHOULD BE are printed. The
program then reads back the data in the
memory and compares it to what the data
should be. If the data does not compare,
the address in octal is printed under the
heading ADDRESS, the data in the memory
address is printed in binary under the
heading DATA and the data that should
have been in the address is printed in binary
under the heading SHOULD BE. The bits
of the two bytes which do not compare
indicate that they are defective. If no bad
locations are detected, NO BAD BITS
DETECTED is printed. The program then
prints TEST PATTERN #2 LOADING and
repeats basically the same above described
display only for test #2.

This program should not only detect
inoperative memory but also "slow"
memory, "forgetful" memory and "bleed­
ing" memory. Just type in the program and
save it on tape; then the next time you have
a new memory board to test, no more
toggling!•

Listing 2: A sample run of the memory test
program.

RUN
START WITH BEGINNING OF PAGE? 6
END WITH END OF PAGE? 6
TEST PATTERN #1 LOADING
MEMORY TEST #1 FROM 6000 TO 67777 OCTAL
ADDRESS DATA SHOULD BE
NO BAD BITS DETECTED
TEST PATTERN #2 LOADING
MEMORY TEST #2 FROM 6000 TO 67777 OCTAL
ADDRESS DATA SHOULD BE
NO BAD BITS DETECTED
TEST COMPLETED
OK
RUN
START WITH BEGINNING OF PAGE? 7
END WITH END OF PAGE? 7
TEST PATTERN #1 LOADING
MEMORY TEST #1 FROM 70000 TO 77777 OCTAL
ADDRESS DATA SHOULD BE
70000 11111111 01010101
70002 11111111 01010 01 01
70004 11111111 01010101
70006 11111111 01010101
70010 11111111 01010101
70012 11111111 01010101
70014 11111111 01010101
70016 11111111 01010101
70020 11111111 01010101
70022 11111111 01010101
TEST PATTERN #2 LOADING
MEMORY TEST #2 FROM 70000 TO 77777 OCTAL
ADDRESS DATA SHOULD BE
70000 11111111 01010101
70002 11111111 01010101
70004 11111111 01010101
70006 11111111 01010101
70010 11111111 01010101
70012 11111111 01010101
70014 11111111 01010101
70016 11111111 01010101

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The first book in the Programming Technique series is entitled PROGRAM DESIGN. It discusses in detail the theory of program design. The purpose of the book is to provide the personal computer user with the techniques needed to design efficient, effective, maintainable programs. Included is information concerning structured program design, modular programming techniques, program logic design, and examples of some of the more common traps the casual as well as the experienced programmer may fall into. In addition, details on various aspects of the actual program functions, such as hashed tables and binary tree processing, are included.

ISBN 0-931718-12-0
Editor: Blaise W. Liffick
Pages: 96
Price: $6.00
Publication: Fall 1978

In SIMULATION, the second book of the series, are articles dealing with various aspects of specific types of simulation. Both theoretical and practical applications are included. Particularly stressed is simulation of motion, including wave motion and flying objects. The realm of artificial intelligence is explored, along with simulating robot motion with the microcomputer. Finally, tips on how to simulate electronic circuits on the computer are detailed.

Editor: Blaise W. Liffick
Pages: approx. 80
Price: $6.00
Publication: Fall 1978

The third book is NUMBERS IN THEORY AND PRACTICE. This book includes information of immense value to both the novice and the experienced personal computerist. The mechanics of the binary system are discussed, including division and multiplication, as well as the places to look for numerical error in programs. Floating point numbers, what they are and how to use them, are covered. There are also sections on numerical methods (functions, approximations, statistics), Boolean math, and several different approaches on how to obtain random numbers.

ISBN 0-931718-14-7
Editor: Blaise W. Liffick
Pages: approx. 100
Price: $6.00
Publication: Fall 1978

The fourth book so far scheduled in this series is called BITS AND PIECES. The articles collected for this book are mostly unrelated and do not neatly fit into the topics of the previous three books, but still have a lot to do with programming techniques. Areas such as multiprocessing and interactive computing with the personal computer are discussed, as well as stacks, sorting, Polish notation, and program optimization. This is by far the most general book of the series.

Editor: Blaise W. Liffick
Pages: approx. 100
Price: $6.00
Publication: Fall 1978
RA6800ML: AN M6800 RELOCATABLE MACRO ASSEMBLER is a two pass assembler for the Motorola 6800 microprocessor. It is designed to run on a minimum system of 16 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (such as Motorola MIKBUG read only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

The Assembler can produce a program listing, a sorted Symbol Table listing and relocatable object code. The object code is loaded and linked with other assembled modules using the Linking Loader LINK68. (Refer to PAPERBYTE™ publication LINK68: AN M6800 LINKING LOADER for details.)

There is a complete description of the 6800 Assembly language and its components, including outlines of the instruction and address formats, pseudo instructions and macro facilities. Each major routine of the Assembler is described in detail, complete with flow charts and a cross reference showing all calling and called-by routines, pointers, flags, and temporary variables.

In addition, details on interfacing and using the Assembler, error messages generated by the Assembler, the Assembler and sample IO driver source code listings, and PAPERBYTE™ barcode representation of the Assembler’s relocatable object file are all included.

This book provides the necessary background for coding programs in the 6800 assembly language, and for understanding the innermost operations of the Assembler.

LINK68: AN M6800 LINKING LOADER is a one pass linking loader which allows separately translated relocatable object modules to be loaded and linked together to form a single executable load module, and to relocate modules in memory. It produces a load map and a load module in Motorola MIKBUG loader format. The linking Loader requires 2 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (for instance, Motorola MIKBUG read only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

It was the express purpose of the authors of this book to provide everything necessary for the user to easily learn about the system. In addition to the source code and PAPERBYTE™ bar code listings, there is a detailed description of the major routines of the Linking Loader, including flow charts. While implementing the system, the user has an opportunity to learn about the nature of linking loader design as well as simply acquiring a useful software tool.

TRACER: A 6800 DEBUGGING PROGRAM is for the programmer looking for good debugging software. TRACER features single step execution using dynamic break points, register examination and modification, and memory examination and modification. This book includes a reprint of “Jack and the Machine Debug” (from the December 1977 issue of BYTE magazine), Tracer program notes, complete assembly and source listing in 6800 assembly language, object program listing, and machine readable PAPERBYTE™ bar codes for the object code.
TINY ASSEMBLER 6800, Version 3.1 is an enhancement of Jack Emmerichs' successful Tiny Assembler. The original version (3.0) was described first in the April and May 1977 issues of BYTE magazine, and later in the PAPERBYTE™ book TINY ASSEMBLER 6800 Version 3.0.

In September 1977, BYTE magazine published an article entitled, "Expanding The Tiny Assembler". This provided a detailed description of the enhancements incorporated into Version 3.1, such as the addition of a "begin" statement, a "virtual symbol table", and a larger subset of the Motorola 6800 assembly language.

All the above articles, plus an updated version of the user's guide, the source, object and PAPERBYTE™ bar code formats of both Version 3.0 and 3.1 make this book the most complete documentation possible for Jack Emmerichs' Tiny Assembler.

ISBN 0-931718-08-2
Author: Jack Emmerichs
Pages: 80
Price: $9.00
Publication: Summer 1978

SUPERWUMPUS is an exciting computer game incorporating the original structure of the WUMPUS game along with added features to make it even more fascinating. The original game was described in the book What To Do After You Hit Return, published by the People's Computer Company. Programmed in both 6800 assembly language and BASIC, SUPERWUMPUS is not only addictively fun, but also provides a splendid tutorial on setting up unusual data structures (the tunnel and cave system of SUPERWUMPUS forms a dodecahedron). This is a PAPERBYTE™ book.

ISBN 0-931718-03-1
Author: Jack Emmerichs
Pages: 56
Price: $6.00
Publication: Summer 1978

MONDEB: AN ADVANCED M6800 MONITOR-DEBUGGER has all the general features of Motorola's MIKBUG monitor as well as numerous other capabilities. Ease of use was a prime design consideration. The other goal was to achieve minimum memory requirements while retaining maximum versatility. The result is an extremely versatile program. The size of the entire MONDEB is less than 3 K.

Some of the command capabilities of MONDEB include displaying and setting the contents of registers, setting interrupts for debugging, testing a programmable memory range for bad memory locations, changing the display and input base of numbers, displaying the contents of memory, searching for a specified string, copying a range of bytes from one location in memory to another, and defining the location to which control will transfer upon receipt of an interrupt. This is a PAPERBYTE™ book.

ISBN 0-931718-06-6
Author: Don Peters
Pages: approx. 72
Price: $5.00
Publication: Summer 1978

BAR CODE LOADER. The purpose of this pamphlet is to present the decoding algorithm which was designed by Ken Budnick of Micro-Scan Associates at the request of BYTE Publications, Inc., for the PAPERBYTE™ bar code representation of executable code. The text of this pamphlet was written by Ken, and contains the general algorithm description in flow chart form plus detailed assemblies of program code for 6800, 6502 and 8080 processors. Individuals with computers based on these processors can use the software directly. Individuals with other processors can use the provided functional specifications and detail examples to create equivalent programs.

Author: Ken Budnick
Pages: 32
Price: $2.00
Available now
In Defense of Analog?

I am an avid and enthusiastic supporter of the personal computing hobby and of BYTE. (At present I am building a full 6502-based OSI machine which pleases me very much.) But I am an old timer in electronics and think that all the fantastic digital devices which have been developed over the last few years have convinced people that general purpose analog computers belong in museums.

I feel there are a couple of things we digital hackers ought to consider:

1. Computing is computing. Setting up an analog machine to solve a differential equation is as satisfying as writing an elegant software program and, given some proper peripheral equipment, the results can be useful and aesthetically pleasing.
2. In some areas, analog machines can do a better job more easily; compare wiring an analog machine to writing a Runge-Kutta program or performing a slow digital computation when a less precise but real time analog computation will do.
3. The present CA3XXX series of op amps should be able to increase the accuracy of an analog machine by several orders of magnitude, especially when using a good analog/digital design for a digital readout.

Surely among your readers there are people who think as I do; I'd like to contact such people and find out the following things:

1. Does any manufacturer produce printed circuit boards or kits to build a reasonably powerful machine — say 4 or 5 integrators?
2. Does anyone have an old general purpose machine which could be updated? Is it for sale?

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Most of the BASIC interpreters available on the microcomputer market today do not provide the PRINT USING option. I have written a formatting subroutine that will perform some of the PRINT USING functions for monetary output:

- Round the monetary amount to the nearest cent.
- Convert the numeric value to a character string and check the digits after the decimal point. If the last one or both digits are missing, insert zeroes.
- Insert a dollar sign in front of the converted amount. If the amount is less than 1, insert a 0 in front of the decimal point.
- Supply the length of the amount.

Before calling the subroutine, we have to pass the dollar figure to be processed to the variable X1. The converted figure is passed back in the variable X$. The length of the formatted amount is passed back in X3.

The routine in listing 1 has been written in the Commodore PET-2001 version of Microsoft BASIC. Modifications may be required for other BASIC interpreters. The remarks can be deleted for faster execution and memory savings.

I use this subroutine in most of my programs. I place it rather high in the program (line numbers 3000 thru 3099) so I can always use the same line numbers.

Listing 1: BASIC program for formatting dollars and cents in BASIC interpreters that do not have the PRINT USING function. Also shown is a sample run of the program.

```
10 INPUT A
20 X1=ABS(A):GOSUB 3000
30 PRINT TAB(20-X3);X$
40 GOTO 10
3000 REM ******************************
3001 REM THIS SUBROUTINE WILL FORMAT
3002 REM DOLLARS AND CENTS
3003 REM ******************************
3004 REM ROUND THE AMOUNT
3005 X1=INT(X1*100+.5)/100
3010 X0$=":X$="
3020 IF X1=0 GOTO 3030
3025 IF X1<1 THEN X0$="0"
3030 X1=STR$(X1)
3035 X2=LEN(X1$)
3040 X2=X2-1
3041 REM DELETE SPACE IN FRONT
3042 REM OF THE FIRST DIGIT
3045 X1=MID$(X1$,2,X2)
3050 FOR I=1 TO X2
3055 X2=MID$(X1$,I,1)
3060 X3=I
3065 IF X2<="9" THEN GOTO 3095
3070 NEXT I
3075 X9$="00"
3080 GOTO 3090
3085 IF X3=(X2-1) THEN X9$="0"
3090 NEXT I
3095 X3=LEN(X9$)
3099 RETURN
```

Sample run:

```
?2 $2.00
?2.2 $2.20
?2.22 $2.22
?222 $222.00
?775.756 $775.76
```
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PAM/8: A New Approach to Front Panel Design

Since the first personal computers appeared about three years ago, the field has been growing and advancing at an ever increasing rate. The variety and complexity of products increases even while the cost decreases. Indeed, the field has evolved so rapidly that it has gone through two generations (using the term somewhat loosely) in those three years. The first generation machines were typified by the first 8800 system sold by MITS, a bare bones machine festooned with switches and lights. It took a fair amount of technical know how to build one of these to get it operational. Before long, however, a new generation of machines was available. These, such as the SwTPC 6800, were usually cheaper and simpler to build, using fewer but more powerful integrated circuits.

And in July 1977, the Heath Company announced its two versions of the home computer idea, the H8 and H11 systems. I write as one of the persons who took part in the design of the H8's front panel firmware, an 8080 program called "PAM/8" which shows how software and hardware are often intimately related.

Microprocessor Front Panels

The ideal front panel for a microcomputer should allow its user total control and access to the processor's workings. A good panel system should allow an instantaneous display of the processor's states, register contents, memory contents, and other operating flags. An operator should be able to force a new state, register value, or memory value upon the processor with ease at any time without otherwise interfering with the executing program. In other words, it should be possible to examine any memory location or any register at any time without disturbing the program.

Ten years ago the implementation of such a front panel was obvious. The processor was built up from components such as integrated circuits, and the flags and registers were directly available on the circuit cards. In the remainder of this article, I will refer to this type of machine as a discrete processor, although it may be built out of high level integrated circuits. To build a suitable front panel for such a discrete processor, it is merely necessary to run a wire to a front panel indicator. Likewise, special logic can be built to allow flags and registers to be set from the front panel switches, usually when the machine is in a halted condition. Readers may have had experience with some of these minicomputer systems, such as the CDC 1700 or the IBM 1130 and 1620. This design works reasonably well, but the binary format is inconvenient and the cost of the front panel hardware and logic can be prohibitive for use in a personal computing system.

The situation was considerably changed with the advent of microprocessors. Now, for the first time, a full-fledged computer is within the financial reach of the general public. Unfortunately, the very development which brought this exciting possibility also brought problems. With a 1 integrated circuit microprocessor, the processor flags and register contents were no longer available for a front panel system, being buried out of reach of any possible hardware hookups. A typical microprocessor integrated circuit only has 40 connection pins (or pinouts). These are partly taken up with power supply and clocking signals, as well as the data and address buses. The remaining pins are allocated to receiving and providing signals to interface the processor to the rest of the computer system. As a result, there is no direct way to determine the contents of the processor's registers.
Previous Front Panel Systems

Attempts to solve this fundamental problem of control over the microprocessor have been responsible for the major differences between competing machines. The first widely available machine, the MITS 8800, used a direct approach to front panel design: it simply had LED readouts for each pinout on the microprocessor chip and a bank of switches hooked across the data and address busses. Some additional logic was incorporated to control the running state of the microprocessor and to allow memory locations to be read to and written from via the front panel. This scheme is a straightforward adaptation of traditional panel design; unfortunately, there wasn't a great deal of correspondence between the useful items a programmer might want and the data available on the processor pinouts.

The difficulties of using such a panel system are by now nearly legendary: it is very awkward and time consuming to get information in and out of the processor. For example, to simply determine the contents of a register, it is necessary to stop the processor, write a small program to store the register in a memory location, key it in to some unused portion of memory, run it, read the stored value from memory, and then restore control to the interrupted program. Needless to say, this is a tedious process with many opportunities for error.

The problems with this approach no doubt influenced the designers of the second generation machines. They used a different approach wherein a console terminal was used in conjunction with a monitor program (usually in read only memory) to provide the equivalent of front panel service. With such a system, a programmer could display desired information such as memory or register contents directly in octal or hexadecimal. This represented a great step forward: entry speed was increased, and the clerical task of encoding and decoding binary values was eliminated. Another great benefit of this system was that most of the monitors incorporated a bootstrap loader so that the loader did not have to be keyed in each time.

This technique has been rapidly gaining popularity at the expense of the lights and switches system, for obvious reasons. Several companies are offering such monitors encoded in read only memory boards to allow users to convert their old systems. However, this new technique still has a few disadvantages: it requires a console terminal, which adds considerably to the system cost, and once a user program has started execution the services of the monitor system are no longer available.

PAM/8 Design Goals

It was mentioned above that the front panel system is the area in which many of the differences between computer systems are found; this holds true for the Heath H8 system as well. The H8 employs a new concept in microprocessor front panels: it uses a unique combination of software and hardware to allow the emulation of a complete real time front panel system which I believe to be superior in performance to even the discrete minicomputer panel systems.

When the H8 project began, Heath engineers studied the requirements for a good front panel system closely and drew up a list of the major features to be satisfied. There were nine major requirements of a good front panel:

- The front panel system must present and accept data in a convenient octal format. Encoding and decoding binary is a job more suited to a computer than a human being.
- The front panel system must incorporate facilities to load and dump memory to and from an external device such as a cassette interface. A nearly foolproof error detection scheme must be used so that mysterious errors will not be introduced by bad loads.
- The front panel system must allow memory and register contents to be conveniently displayed and changed. In addition, display has to be in real time. That is, if the front panel is displaying the contents of a register and the running program changes those contents, the change should be immediately visible on the panel.
- The front panel system must be capable of execution control. That is, the operator should be able to step through a program one instruction at a time, and be able to set breakpoints within his code.
- The front panel system must provide facilities for inputting and outputting to IO ports.
- The front panel system must be easy to use, and (as much as possible) should reduce the opportunity for operator error. Whenever a front panel operation is performed, the programmer must be informed of the operation's success or failure.
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Undoubtedly, this was a formidable list. Happily, though, Heath was able to report success with the creation of the PAM/8, the panel monitor for the H8 computer.

**PAM/8 Description**

The front panel of the H8 computer is shown in photo 1. Three features are immediately obvious: a 16 key keypad, nine 7 segment LED displays, and four single LED lamps.

The 16 key keypad (see photo 2) is the sole input device to the PAM/8 system. It is used for commands for PAM/8, to enter data into memory and registers, and as a bank of sense switches. Some keys have more than one function; however, no confusion results because PAM/8 provides a clear indication at all times of which meaning will be taken for such keys.

The second visible feature is the group of nine 7 segment LED displays. These are used to display addresses, data, and register names. 16 bit values are displayed in “split octal” notation. Each byte is represented as three octal digits; therefore, a 16 bit value is simply presented as two such byte groups together. Thus, in split octal notation, 377 + 001 = 001 000.

The third visible feature consists of four LED lamps (see photo 3). Three of these lamps display true hardware conditions: power on (PWR), processor running (RUN), and interrupts enabled (IE). In fact, these are the only hardware indicators in the PAM/8 system. All other displays, indicators, and keypads are under firmware control. The remaining LED, MTR, is lit when the computer is in monitor mode. Monitor mode means that the user program is not running, and the keypad is available for PAM/8 commands. When the user program is running, PAM/8 ignores most keypad commands so that the user program can use it as an input (sense switch) device.

The best way to describe the operation of the PAM/8 monitor is to go through the list of design goals again, describing how it fulfills each objective. In the process, I will touch upon some other pieces of PAM/8 hardware not visible on the front panel.

---

Photo 1: Front panel of the Heath H8 computer. At left are nine 7 segment LED displays and four single LED lamps; at right is the 16 key keypad. The front panel is controlled by a novel firmware panel monitor (PAM/8) made up of both hardware and software elements.

Photo 2: H8 16 key keypad, the sole input source for the panel monitor (PAM/8). The keypad is used to enter commands and data. Some keys have more than one function, but the monitor provides an indication of which meaning will be taken for these keys.
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The front panel system must be capable of displaying and altering both memory and registers conveniently. To display the contents of a memory location or register, strike the MEM (#) or REG(.) key followed by a 6 digit address (for MEM) or a 1 key register select (for REG). In the case of memory display, the address will appear in the left six digits, the value in the right three. In the case of a register, the value of the register (if 16 bits) or the register pair (for 8 bit registers) is displayed in the left six digits, and the register name(s) is displayed in the right two digits. See photo 3 for examples.

To change the contents of a register or memory location, first display the old contents as described above. Next strike the ALTER (/) key. You can then alter the register or location by entering six (or three) octal digits. As each 3 digit group is entered, the PAM/8 monitor provides a beep in acknowledgement. In the case of memory alteration, the memory address is automatically incremented by one. This allows you to enter a series of memory locations by entering a steady stream of values.

When the altering is complete, restriking the ALTER key clears the alter mode and restores the 0 through 7 keys to their usual function.

It is important to note that the register and memory displays are real time: if the contents of that register or location change, the display will immediately show the new value. Thus, to watch the PC register in a
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running program, merely select it for display and type GO. Should you now decide to watch the contents of a memory byte, press RTM/0 (# and 0 simultaneously) to halt the program, select the memory location, then press GO to resume execution from where it halted.

"The front panel system must be capable of execution control." PAM/8 provides five types of execution control:

- Run
- Halt
- Jump
- Breakpoints
- Single Instruction

Pressing the GO key starts a program running at the current value of the PC register. The desired start address can be entered into the program counter beforehand. To stop a running program, press RTM (return to monitor, keys 0 and # simultaneously). Execution of the program will immediately halt, and the MTR light will come on. The operator can now examine registers and memory locations and may alter them if desired. Pressing GO causes execution to resume where it left off. To jump the processor to a section of code, press RTM, alter the PC register and press GO.

When a HLT instruction is encountered by a user program, the PAM/8 gives a single alarm beep and execution of the user program is halted. The PC register points to the byte following the HLT operation. Pressing GO causes execution to resume following the HLT opcode. The user can make use of breakpoints to debug programs by assembling or patching in HLT operations.

PAM/8 also includes a single instruction facility. Each time the SI key is struck, the instruction pointed to by the program counter is executed and the user program is immediately halted. This works for all 8080A instructions except DI (disable interrupts) including jumps, subroutine calls, and other control-transfer instructions. Holding down the SI key causes the execution of an instruction every 400 ms. It is especially instructive to display a register and use the SI key to execute instructions one by one while watching the effect these instructions have on the registers being displayed.

"The front panel system must provide facilities for communicating with IO ports." To communicate with an IO port, use the MEM key to enter the 3 digit data value and the 3 digit port address as a 6 digit memory address. Striking the OUT key causes the data value to be output to the port. Striking the IN key causes the value read from the port to be displayed in the leftmost three digits.

"The front panel system must be easy to use and should reduce the possibility for error." In order to increase convenience and minimize operator errors, PAM/8 is designed to maximize the bandwidth of the operator-machine communication channel. Thus, PAM/8 communicates in three different ways: by the digit displays, by the alarm horn, and by the display decimal points. The use of the digit displays in communication is obvious. Many panel operations, such as entering addresses and values, cause the display to change. For instance, when altering memory, the value of each key struck is shown in the displays. The front panel horn actually serves three purposes:

- Verify keystrokes.
- Provide information (such as the beep when entering byte values).
- Provide alarm indications (such as a CRC error when loading).

The PAM/8 uses the digit decimal points independently of the values on the digits themselves. As can be seen from photo 1, some keys have multiple uses. PAM/8 uses the decimal points to indicate which use of the key is currently active. When the REG or the MEM key is struck, PAM/8 expects an address (or register number). The decimal points are lit continuously, indicating that the address must be entered and that the keys 0 through 7 will be taken as address values. When the ALTER key is struck, PAM/8 displays a rotating pattern on the decimal points, indicating that a value must be entered, and the keys 0 through 7 will be taken as data values.

"The front panel system must be transparent." In operation, PAM/8 is totally transparent to a task program; i.e., the program need not take any notice of the presence of the PAM/8 system; any existing 8080A program can run on the H8 without change (assuming it is ORGed correctly, and the IO is compatible). Since PAM/8 is implemented partially in system software, it does require processor service for operation. Normally, PAM/8 uses about 15 percent of the processor's capacity, leaving 85 percent for task programs. Most programs are compute bound for very short periods of time, and this presents no difficulties. Programs which must run at full speed can set a flag bit in the PAM/8 programmable memory area to turn off the front panel, which then gives the task program 100 percent of the
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processor's capacity. The task program can then reenable PAM/8 when it desires.

"The front panel system must be versatile." Although a user program need not communicate directly with PAM/8, such communication is possible. In general, there is a set of special control bytes in the PAM/8's programmable memory area which can be used to control system operation. For example, a user program can cause PAM/8 to display any arbitrary segment pattern on the LED displays. Likewise, the user program can cause PAM/8 to stop refreshing the displays so that the program can refresh them itself. In general, it is possible to totally close down PAM/8 operations and to have a user program take them over, thus totally replacing the PAM/8 monitor with a homebrew system. Of course, user programs can make use of the PAM/8 utility subroutines to communicate with the tape system, read the keypad (with audio feedback and auto repeat), sound the horn, and so forth.

"The front panel system must be inexpensive." PAM/8 provides powerful features at a low cost due to its firmware design. The read only memory software handles display decoding and refreshing, keypad debouncing, and all high level functions. The necessary hardware consists of the keys, the LED displays, and a few SSI and MSI logic gates. In general, the PAM/8 design costs less than a good toggle switch and lamp panel.

How It Works

As mentioned above, PAM/8 is a firmware system, meaning that its functions are implemented by a closely integrated combination of hardware and software. The hardware resides on the front panel circuit board itself, and the software resides in a 1 K read only memory on the processor board. This read only memory contains a program which does most of the work for the PAM/8 system. Actual hardware was used only when the function could not be implemented by the program.

The central concept in the PAM/8 system is its built-in clock interrupt. When the system is powered on (or master cleared) PAM/8 sends a command to the panel control port requesting an interrupt every 2 ms. This interrupt interval is derived from the system's crystal clock and is therefore called the clock interrupt. The presence of this interrupt allows PAM/8 to perform two processes, or tasks, simultaneously. Of course, they are not actually performed simultaneously, since the computer has only one processor, but to a being as slow as a human the operations appear simultaneous.

This division of the work load between two independent tasks, the task time and the interrupt time processes gives PAM/8 its power. For the sake of clarity, the functions of these two tasks will be discussed separately and it will be assumed that they are truly simultaneous.

Interrupt Time

The interrupt time task is always running (unless shut off by the user program) and has three main jobs:

- Process display refreshing and updating.
- Maintain system clock.
- Allow user program clock servicing.

The most important job of the interrupt time process is to refresh the front panel displays. The displays are not latched and decoded; the display hardware consists of a 4 bit digit select field and an 8 bit pattern select field. Every interrupt cycle (2 ms), a segment pattern and digit number are output by the code. The digits are refreshed round robin so that each digit is lit every 18 ms (nine digits at 2 ms each). This gives an overall refresh rate of 55 times a second, which is sufficient to eliminate flicker. The segment patterns being refreshed are obtained from a 9 byte programmable memory area. Each 8 bit byte contains the pattern for a digit (seven segments, one decimal point). Every 32 clock interrupts, or about 16 times a second, the 9 byte pattern being displayed is updated. The PAM/8 monitor examines flag locations to determine which memory location or register is being displayed and decodes its value into nine bytes of display bar code. If a register is being displayed, the program finds its value on the stack where it was pushed when the clock interrupt occurred. It should be noted that both of these processes, refreshing and updating, may be controlled by a user program. There is a bit for each function allocated in a PAM/8 control byte; setting the bit causes the function to be discontinued. Most programs which make use of this feature turn off display updating, but they leave display refreshing turned on. Then the program can display any arbitrary pattern by simply placing segment bar patterns into the 9 byte area in memory.

The second main job performed by the interrupt time task is the maintenance of the system clock. The PAM/8 monitor
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maintains a 16 bit count of the clock interrupts received. Since this count is updated during the clock interrupts, it appears to task time programs that the location "magically" increments itself. Many programs, including the task time portion of PAM/8, make use of this counter.

The third major job of the interrupt time task is the handling of user clock processing. Normally, PAM/8 returns directly from the clock interrupt so that the operation will be transparent to the user program. However, a user program can set a bit in a PAM/8 control byte requesting that a user subroutine be called during every clock interrupt. This allows the user to also write task time and interrupt time systems, as well as giving multitasking capability.

Task Time Task

While all this clock interrupt processing is taking place, the H8 is also running a task time program. Task time refers to the "problem solving" program which runs when interrupts are not being serviced. Under the PAM/8 system, the task time program may be the user program itself, or it may be the PAM/8 command processing program.

When the system is initialized after power up, the task program is the PAM/8 command processor, which continually reads the keypad for operator commands. Keypad debouncing, key strike verification (beeps) and auto repeat on the keypad are all time dependent functions; PAM/8 makes use of the system clock to implement them. When a command is recognized, it is executed immediately. Having the interrupt time task running simultaneously with the command loop greatly simplifies command processing. For example, pressing the +key (when displaying memory) is supposed to cause the next location to be displayed. All the command processor needs to do is to increment the "address being displayed" word in memory. Sometime during the next 32 clock interrupts the interrupt task will decode this new address and its contents, causing the new address and value to be "magically" displayed (after a maximum wait of 1/6 of a second). In a similar manner, the routines to handle the LOAD and DUMP functions merely update the address being displayed word after every byte is loaded or dumped; the interrupt time task sees to it that the address being loaded is continuously displayed on the panel LEDs.

After reading this discussion, you can probably guess how the GO command is implemented: the PAM/8 monitor merely restores the user registers from the stack. The PC register is restored last, which causes execution to begin at the specified location. The interrupt task time process proceeds as before, decoding and displaying the selected memory or register contents. Should the location or register be altered by the running program, the front panel window will very quickly (typically in 32 ms) show the change.

HLT and Return to Monitor

So far, we've seen that the interrupt time and task time processes don't intermingle; each keeps to its own. The processing of the HLT instruction and the RTM (return to monitor) command are exceptions to this principle. When a HLT instruction is encountered the processor waits with the program counter pointing to the next byte. When the next clock interrupt comes along, the interrupt processing code takes a look at the preceding instruction; if it is a HLT, the code passes control directly to the PAM/8 task time command loop, never...
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returning to the user program. Naturally, a little bit of cleaning up is performed to smooth over the abrupt transition from interrupt time to task time. This feature allows the use of the HLT instruction as a breakpoint and also provides transparent support of the HLT operation. When a program halts, the front panel comes alive, and user program execution stops. Striking the GO key causes execution to resume following the HLT instruction.

The RTM command is a key command executed by pressing the 0 and # keys simultaneously. This command serves the purpose of the RUN/HALT switch on hardware front panels: striking RTM causes execution of the user program to cease, and it causes the front panel to become active. The RTM command is implemented by a joint hardware and software effort: on a hardware level, the pressing of the two keys causes a clock interrupt to be requested immediately, without waiting through the 2 ms interval. On the software level, the clock interrupt code in PAM/8 checks the keypad for the special RTM key combination. If it is present, the same process that was used for the HLT operation is used: control passes directly to the PAM/8 task time command loop, not back to the interrupted user program.

Using the PAM/8

The design of recent microcomputer systems has shown a trend away from front panel designs toward the "no front panel" monitor. This is being done for a very good reason: a terminal monitor based on programmable memory or read only memory is much easier to use and is more powerful than hardware front panels. This fact also applies to the PAM/8 system: a good console oriented monitor and debugger, such as Heath's HBUG, is much more convenient for debugging programs. This is not to say that PAM/8 does not perform an indispensable task, as I will try to show in the following real life examples.

A typical experience in the life of a computer experimenter is the debugging of some peripheral interface. I've spent many a long hour slaving over a processor, trying to make some new device or interface talk to my computer. A favorite technique I use for this is to enter a 2 statement program into memory:

```
L1 IN <port number> 
JMP L1
```

This program simply inputs from the port assigned to the recalcitrant device into the accumulator, then loops back to do it again and again. Then all I do is set the PC register to the L1 address, punch up the accumulator for display, and press GO. The value read from the port will be continuously displayed in the A register, even while I adjust the hardware. By watching the panel displays, I can instantly see any results of my labors, such as, "if I ground this line, will that bit come on?"

Another important use for PAM/8 is as an aid to debugging software. Often I find myself debugging a complex piece of software that maintains various state flags in memory. For example, a command completion subroutine, which examines characters as they are entered for valid syntax, is a state dependent program. As each character is entered, the program sets flag bits indicating various things such as "two alphabetic characters entered," or "have just seen a blank," etc. When debugging this code, I simply display the address (or register) containing the state flags on the front panel. Then, as I strike test keys one by one, I can immediately judge the program's reaction by examining the state flags. This technique can be used to monitor working programs as well. For example, I have a loader program which I use to download programs from other computers. It keeps the address currently being loaded in the HL register pair. By simply displaying this register pair, I can watch the load progress (or fail!).

A real time front panel can be used for more than just debugging. The presence of the displays and keypad provides another channel of communication with the processor, independent of the console terminal. The displays can be used to indicate any desired status, and the keypad can be used as a bank of "sense switches," even while the console is being used by the program. For example, the BASIC interpreter supports commands to control the displays and read the keypad.

Conclusions

The PAM/8 front panel system provides an inexpensive and effective "firmware front panel" which emulates a complete hardware front panel. Its design combines the capabilities of a true hardware panel with the flexibility of firmware and ultimately provides the user with a greater communications bandwidth to a personal computer.
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<th>Sales tax</th>
<th>$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$35 shipping/handling or $25 carton</td>
<td>$</td>
<td>TOTAL</td>
<td>$</td>
</tr>
</tbody>
</table>

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First Steps in Computer Chess Programming

The fascination of chess gains a new dimension with microcomputer chess. No longer are the struggles confined to giant machines. With the advent of the Chess Mate, Chess Challenger, Boris, and Computer Chess, as well as some custom software packages, the day of microcomputer chess has dawned. Writing a program to play chess on a small system is no small matter, though. Consider just for a start the challenge of meaningfully representing the board and its pieces in computer memory: there are 64 squares, 32 pieces, 6 piece types and 2 piece colors. Since the machine is a microcomputer, storage requirements must be kept to a minimum. Next comes the job of moving the pieces. Only when these first problems of piece representation and move generation have been solved can the chess programmer go on to consider strategy.

Sargon, a chess playing program we developed for Z-80 machines, solves the representation problem through the use of a board array. Move generation is accomplished through a network of routines diagrammed in figure 1. The functions of the routines are as follows:

- **GENMOV**: Generate move routine. Generates the move set for all of the pieces of a given color.
- **MPIECE**: Piece mover routine. Generates the move set for a given piece.
- **INCHK**: Check routine. Determines whether or not the King is in check.
- **PATH**: Path routine. Generates a single possible move for a given piece along its current path of motion.
- **ADMOVE**: Admove routine. Adds a move to the move list.
- **CASTLE**: Castle routine. Determines whether castling is legal and adds it to the move list if it is.
- **ENPSNT**: En passant routine. Tests for an en passant pawn capture and adds it to the move lists if it is legal.
- **ATTACK**: Attack routine. Finds all the attackers on a given square.
- **ADJPTR**: Adjust move list pointer. Links around the second move in a double move (i.e., castle or en passant pawn capture).
- **ATKSAV**: Attack save routine. Saves attacking piece value in the attack list and increments the attack count for that color piece.
- **PNCK**: Pin check routine. Checks to see if an attacking piece is in the pinned piece list.

Several of the routines involved are multipurpose routines. Their involvement in move generation is incidental to a main function elsewhere in the move selection logic. The key routines in move generation are MPIECE, PATH, CASTLE and ENPSNT. Of these,
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Figure 2: Decimal (a) and hexadecimal (b) representations of the chessboard used in the Sargon program. Each square of the board is represented by a single byte in memory. Border squares are assigned a flag value of hexadecimal FF. The use of the border simplifies move generation, since it becomes easy to determine when a piece moves off the board.

The Board in Memory

The chessboard in memory is an array of 120 bytes that can be visualized as in figure 2. Each square of the board is represented in memory by a single byte. Border bytes are assigned a flag value of hexadecimal FF. The border simplifies move generation, since it becomes easy to determine when a piece moves off the board.

The Pieces in Memory

Each piece is represented in memory by one byte of data. The meaning and function of the bits are as follows:

- **Bit 7**: color of the piece.
  - 1 - Black
  - 0 - White

- **Bit 6**: not used.

- **Bit 5**: not used.

- **Bit 4**: castle flag for Kings only.
  - Set if the King has castled.

- **Bit 3**: moved flag.
  - Set if the piece has moved.

- **Bits 2-0**: Piece type.
  - 1 Pawn
  - 2 Knight
  - 3 Bishop
  - 4 Rook
  - 5 Queen
  - 6 King

The pieces in play occupy squares of the board. If a board square is empty, it has the value 00. Thus the board set up for play would be as shown in figure 3.

### Piece Mover Data Base

In order to generate moves for the pieces on the board, data must be maintained to describe the possibilities for each piece. This is accomplished through the use of three tables. Values for the tables are given in table 1.

- **DIRECT**: Direction Table. Used to determine the direction of movement of each piece.
- **DPOINT**: Direction Table Pointer. Used to determine where to begin in the direction table for any given piece.
- **DCOUNT**: Direction Table Counter. Used to determine the number of directions of movement for any given piece.

The pieces in play occupy squares of the board. If a board square is empty, it has the value 00. Thus the board set up for play would be as shown in figure 3.

### About the Authors

Dan and Kath Spracklen are the creators of Sargon, the microcomputer chess program that won the microcomputer chess tournament at the 1978 West Coast Computer Faire. Dan Spracklen is a 13 year programming veteran. His experience ranges from scientific simulation programs to real time commercial applications. He is currently a senior applications analyst for Sperry-Univac. Kath Spracklen is a graduate student in computer science at San Diego State University. An experienced tournament player, Kath provided the chess background for Sargon.
Equate statements supply symbolic equivalents for the piece types and colors.

Start is the first address in Sargon and should lie on an even 256 byte page boundary. Indexing in the Z-80 makes use of an address, contained in either the IX or IY index registers, plus a displacement. The displacement is a signed number $+127$ to $-128$. Thus a 256 byte area of memory centered on the index address is accessible. For this reason TBASE is placed in the middle of the tables section.

The value of "." is the current program counter. Direct is now the displacement of the direction table from the table base. So if the value of TBASE is loaded in the IY index register, "DIRECT(V)" will reference the first element in the direction table.

Diagonal directions used for Bishop, Queen, and King.
Rank and file directions used for Rook, Queen, and King.
Knight move directions.

White pawn directions including two forward moves and two diagonal moves for captures.
Black pawn directions.

Displacement from table base.
Starting point in direction table. In the order BP, WP, N, B, R, Q, K.

Number of directions to use from table. In the same order as DPOINT.

The board array consists of 120 bytes in memory.

Uses the area of memory between START and START+80H. These indices are used to index into the various tables. Since TBASE is on an even boundary, its address is of the form XX00, where XX depends on the load address. The table address needed for a particular routine is formed by storing a one byte value in the 00 portion. Since addresses are stored in memory with the low order byte first, XX00 would be stored as 00XX. Then changing the 00 portion is simply a matter of storing a one byte value in the index.

Working storage area to hold the contents of the board array for a given square.

Gets the piece to be moved into register A. In GENMOV, the routine which calls MPiece, the piece value in register A, had been exclusive ORed with COLOR, the color of the piece to determine whether or not to call MPiece. Another exclusive OR restores the piece.
This clears all the flag bits and leaves just piece type and color.
Is it a Black pawn?
Listing 1, continued (Listing 1 is concluded on page 95):

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JRNZ</td>
<td>MP2</td>
<td>No-Skip. Decrement, making piece type a 0 for a Black pawn.</td>
</tr>
<tr>
<td>DCR</td>
<td>A</td>
<td>Clear color bit and leaves just the piece type.</td>
</tr>
<tr>
<td>MP2:</td>
<td></td>
<td>This is the first step in forming the index into DPOINT and DCOUNT. T1 contains the value of TBASE (XX00) stored in low-high order (0XX0). After storing the piece type (0-6) in T1, it contains the address of TBASE + TYPE. This operation loads the entire TBASE + TYPE address into the IY index register.</td>
</tr>
<tr>
<td>STA</td>
<td>T1</td>
<td>DCOUNT is the displacement from TBASE to the start of the direction count table. So DCOUNT + TBASE is the starting address of the direction count table. Then DCOUNT(Y) is:</td>
</tr>
<tr>
<td>LIYD</td>
<td>T1</td>
<td>DCOUNT + CONTENTS IY Register</td>
</tr>
<tr>
<td>MOV</td>
<td>B,DCOUNT(Y)</td>
<td>= DCOUNT + TBASE + TYPE (0-6)</td>
</tr>
<tr>
<td>MP5:</td>
<td></td>
<td>= START OF TABLE + TYPE (0-6)</td>
</tr>
<tr>
<td>MOV</td>
<td>A,DCOUNT(Y)</td>
<td>This move instruction pulls the direction count for the given piece type and places it in register B.</td>
</tr>
<tr>
<td>STA</td>
<td>INDX2</td>
<td>Similarly, this instruction pulls the direction table pointer for the given piece type and places it in register A.</td>
</tr>
<tr>
<td>LIYD</td>
<td>INDX2</td>
<td>The direction table pointer will be used to index into the direction table.</td>
</tr>
<tr>
<td>MOV</td>
<td>C,DIRECT(Y)</td>
<td>Gets the direction and places it in register C.</td>
</tr>
<tr>
<td>LDA</td>
<td>M1</td>
<td>Gets the “from” position which was stored in M1 in GENMOV.</td>
</tr>
<tr>
<td>MP10:</td>
<td></td>
<td>Save in M2 to form the address of the current position.</td>
</tr>
<tr>
<td>CALL</td>
<td>PATH</td>
<td>Generate a single move in the given direction.</td>
</tr>
<tr>
<td>CPI</td>
<td>2</td>
<td>Did the moving piece encounter a piece of the same color, or is new position off the board?</td>
</tr>
<tr>
<td>JRNC</td>
<td>MP15</td>
<td>Jump if yes to either question. No move to add to move list. Ready for new direction.</td>
</tr>
<tr>
<td>ANA</td>
<td>A</td>
<td>Was the square moved to empty?</td>
</tr>
<tr>
<td>EXAF</td>
<td></td>
<td>Save the answer to this question by swapping flag register for alternate flag register.</td>
</tr>
<tr>
<td>LDA</td>
<td>T1</td>
<td>Get type of moving piece.</td>
</tr>
<tr>
<td>CPI</td>
<td>PAWN+1</td>
<td>Is it a pawn?</td>
</tr>
<tr>
<td>JRC</td>
<td>MP20</td>
<td>If so, jump to special pawn handling logic. PAWN+1 is equal to the number 2. A White pawn would be of type 1 while a Black pawn would have type set to 0. In either case the carry flag would be set upon a comparison to a value of 2. Valid move, so add it to the move list.</td>
</tr>
<tr>
<td>CALL</td>
<td>ADMOVE</td>
<td>Restore the answer to the empty square question.</td>
</tr>
<tr>
<td>EXAF</td>
<td></td>
<td>If it is not empty, go get ready for next direction. No further moves are possible in this direction.</td>
</tr>
<tr>
<td>JRNZ</td>
<td>MP15</td>
<td>Get piece type. Some pieces may only make one move in a given direction.</td>
</tr>
<tr>
<td>LDA</td>
<td>T1</td>
<td>The King is such a piece. Is this piece a King?</td>
</tr>
<tr>
<td>CPI</td>
<td>KING</td>
<td>If so, go get ready for a new direction.</td>
</tr>
<tr>
<td>JRZ</td>
<td>MP15</td>
<td>Compare piece type to a Bishop.</td>
</tr>
<tr>
<td>CPI</td>
<td>BISHOP</td>
<td>If piece type is bishop or greater (ie: Bishop, Rook, or Queen) go make another move in this same direction.</td>
</tr>
<tr>
<td>JRNC</td>
<td>MP10</td>
<td>Increment direction index for next direction in the direction table.</td>
</tr>
<tr>
<td>MP15:</td>
<td></td>
<td>Decrement the direction count (in register B). If count is not yet 0, go back and repeat this process for the new direction. Otherwise all of the directions have been considered.</td>
</tr>
<tr>
<td>INX</td>
<td>Y</td>
<td>Fetch piece type again.</td>
</tr>
<tr>
<td>DJNZ</td>
<td>MP5</td>
<td>Is it a King?</td>
</tr>
<tr>
<td>LDA</td>
<td>T1</td>
<td>If so, call castle to add it to the move list if legal.</td>
</tr>
<tr>
<td>CPI</td>
<td>KING</td>
<td>Return to GENMOV.</td>
</tr>
<tr>
<td>CZ</td>
<td>CASTLE</td>
<td>Get the number of move directions left to consider. If this is the first direction, register A=4.</td>
</tr>
<tr>
<td>RET</td>
<td></td>
<td>Are there three directions left to look at?</td>
</tr>
<tr>
<td><strong><strong><strong><strong><strong><strong>PAWN LOGIC</strong></strong></strong></strong></strong></strong></td>
<td>MOV</td>
<td>A,B</td>
</tr>
<tr>
<td>MP20:</td>
<td></td>
<td>A carry on this compare indicates a diagonal move. If so, branch to diagonal logic.</td>
</tr>
<tr>
<td>CPI</td>
<td>3</td>
<td>Equality on this compare indicates a forward move of two squares.</td>
</tr>
<tr>
<td>JRC</td>
<td>MP35</td>
<td>Branch to check for legality.</td>
</tr>
<tr>
<td>JRZ</td>
<td>MP30</td>
<td>Otherwise this is a forward move of one square. Restore the answer to the empty square question.</td>
</tr>
<tr>
<td>EXAF</td>
<td></td>
<td>If the square is not empty, this is not a valid move. Go check the next direction.</td>
</tr>
<tr>
<td>JRNZ</td>
<td>MP15</td>
<td>Get the “to” position of the move.</td>
</tr>
<tr>
<td>LDA</td>
<td>M2</td>
<td>Is it on the last rank and therefore a promotion of a White pawn?</td>
</tr>
<tr>
<td>CPI</td>
<td>91</td>
<td>If so, go set promotion flag.</td>
</tr>
<tr>
<td>JRNC</td>
<td>MP25</td>
<td>Otherwise, is it on the first rank and therefore a promotion of a Black pawn?</td>
</tr>
<tr>
<td>CPI</td>
<td>29</td>
<td>If no, skip setting flag.</td>
</tr>
<tr>
<td>MP25:</td>
<td></td>
<td>Load the address of the promotion flag.</td>
</tr>
<tr>
<td>LXI</td>
<td>H,P2</td>
<td>Set the flag (bit 5 of P2).</td>
</tr>
<tr>
<td>SET</td>
<td>5,M</td>
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<tr>
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Table 1: Direction table (a) and direction table pointer and counter (b). In order to generate moves for the chess pieces, data describing the possibilities for each piece is kept in table 1a. Table 1b shows the direction table pointer, which tells where to start in the table for a given piece, and the direction table counter, which determines the number of directions of movement for a given piece.
Figure 4: Generating all the possible Knight moves from the Queen Bishop 3 (QB3) square. The Knight is piece type 2 (see text) and has a DPOINT (direction table pointer) value of 8 and a DCOUNT (direction table counter) value of 8 also. So in generating the Knight's moves, DIRECT + 8 will be the starting point in the direction table, and 8 values will be used: -21, -12, +08, +19, +21, -08, and -19. The Knight starts at White’s QB3 square, which is square 43 (see figure 2a, decimal representation). Thus the first possible Knight move is 43 - 21 = 22 (QN1), and so on.

Sample Move Generation

Suppose a Knight occupies the QB3 square. A Knight is piece type 2 and has a DPOINT of 8 and a DCOUNT of 8 (see table 1b). So in generating the Knight’s moves, DIRECT + 8 will be the starting point in the direction table and 8 values will be used. Those values are -21, -12, +08, +19, +21, -08, and -19. The Knight starts at White’s QB3, which is square 43 (see figure 2a, decimal representation). Thus the first possible Knight move is 43 - 21 = 22 (QN1), and so on.

Move Generation—The Algorithms Explained

Move generation is controlled by GENMOV, which scans the board array and calls MPiece for each piece encountered.
Then MPiece, the piece mover routine, generates all possible legal moves for that piece (moves that place the King in check are eliminated later in the program). The piece is brought in from memory. It is a one byte data value, as previously discussed, which contains piece type, flags and color. The flags are deleted from the piece before checking for type. Basic piece types are indicated by values from 1 to 6. Except for pawns, White and Black pieces move alike. So a special case is needed for the Black pawn. If the given piece is a Black pawn, the piece type is decremented, making it type 0.

The type of the piece, now one from 0 to 6, is used as an index into the DCOUNT, direction table count, and DPOINT, direction table pointer arrays. The values for the given piece are fetched. The direction table pointer is then used as an index into DIRECT, the direction table, and the first move direction is fetched. The "from" position of the piece is the square on which the piece currently stands. This "from" board index and the direction table value are passed as parameters to the routine PATH.

PATH generates the move indicated and returns a flag which describes the status of the "to" position of the piece. Flag values are:

0 "to" position is empty.
1 "to" position contains a piece of the opposite color.
2 "to" position contains a piece of the same color.
3 "to" position is off the board.

PATH accomplishes its task by fetching the "from" position, adding the direction counter, and storing the result as the "to" position. It then uses the "to" position to form an index into the board array. The current contents of the square are fetched. If the square contains hexadecimal FF, it is off the board. The off board flag is set and control is returned to MPiece.

If the square is on the board, the contents of the square are saved in memory location P2. The color and flag bits are then cleared and the remaining piece type is saved in T2. If the square is empty, control is returned to MPiece with the flag value still set to 0. Otherwise the color of the piece on the "to" square is compared with that of the moving piece. The appropriate flag is set to indicate whether or not the pieces are of the same color, and control is returned to MPiece.

Upon return from PATH, piece mover
checks to see if the square is occupied by a piece of the same color or is off the board. If so, this cannot be a legal move, so a check for further moves must follow a new direction. Otherwise a check is made to see if the square is empty. The answer is saved. A check is made to see if the piece being moved is a pawn. If so, control is passed to the special pawn logic. Otherwise the move generated must be added to the move list. ADMOVE is called for the job. After the move has been added to the move list, the answer to the empty square question is recovered. If the square is empty and the piece is a Bishop, Rook, or Queen, it is possible to continue moving in the same direction. In this case control passes back to the call to PATH for another move in that direction. Kings and Knights may make only one move in a given direction.

When the time comes to consider a new direction of movement for the piece, the index into the direction table is incremented. DCOUNT, the number of directions to con-

Listing 1, continued:

MP26: CALL ADMOVE
INX Y
DCR B
LXI H,P1
BIT 3,M
JRZ MP10
JMP MP15

;******** MOVE OF 2 SQUARES********
MP30: EXAF
JRNZ MP15

MP31: CALL ADMOVE
JMP MP15

;*********DIAGONAL MOVE**********
MP35: EXAF
JRZ MP36
LDA M2
CPI 91
JRNC MP37
CPI 29
JRNC MP31
LXI H,P2
SET 5,M
JMPR MP31

;*****DIAGONAL SQUARE EMPTY*****
MP36: CALL ENPSNT
JMP MP15

;**********PATH ROUTINE**********
PATH: LXI H,M2
MOV A,M
ADD C
MOV M,A
LIXD M2
MOV A,BOARD(X)
CPI OFFH
JRZ PA2
STA P2
ANI 7
STA T2
RZ
LDA P2
LXI H,P1
XRA M
BIT 7,A
JRZ PA1
MVI A,1
RET

;**********SAME COLOR**********
MVI A,2
RET

;**********OFF BOARD**********
MVI A,3
RET

Add this move to the move list.
Increment direction index for two square move direction.
Decrement the direction count.
Load the address where the piece was saved.
Check the flag in the piece which tells whether it has moved before.
If the pawn has never moved, go generate a second forward move. (The pawn can move two squares on the first move.) Otherwise go get new direction, skipping second forward move.

Restore the answer to the empty square question.
If the square is not empty, this is not a valid move. Go check the next direction.
Otherwise add this move to the move list.
Go check the next direction.

Restore the answer to the empty square question.
If the square is empty, it is not a normal pawn capture.
Go try en passant.
Get the "to" position of the move.
If the board index is 91 or greater, this is the last rank and a White pawn promotion.
If so, go set promote flag.
Otherwise, if the board index is less than 29, this is the first rank and a Black pawn promotion.
If not, just go add the move to the move list.
Load the address of the promotion flag.
Set the flag (bit 5 of P2), and go add the move to the move list.

Check for possible en passant capture and add it to the move list if legal.
Go check the next direction.

Get the address of the location where the "from" position was stored.
Get the "from" position from that memory location.
Add in the direction from the direction table, giving the "to" position.
Use "to" position to form an index into the board array.
Load the board index.
Get the contents of the board at the "to" square.
Is the "to" position of the board?
If so, go set off-board flag.
Save contents of the board at "to" square.
Isolate piece type.
Save piece type.
Return if the square is empty. The flag value is returned in the A register and it is already 0.
Get piece again.
Load the address of the moving piece.
Compare the pieces.
Check to see if the colors match. If so, after the exclusive OR the color bit will be 0.
If they match, go set match flag.
Otherwise, set different color flag and return.

Set same color flag and return.
Set off-board flag and return.
sider, is decremented. When DCOUNT reaches zero, all the moves for the piece have been generated. If the piece involved is the King, a call to castle will add any legal castling moves. Then control is returned to GENMOV.

All that remains is to discuss the special pawn logic. Pawns are peculiar in that they capture diagonally, but move straight ahead. They also have the option of moving one or two squares forward on their first move. Furthermore, if they reach the eighth and final rank, they may be promoted to another piece. Sargon always promotes its own pawns to Queens. A flag in variable P2 indicates pawn promotion.

The pawn logic in MPIECE first checks to see if the direction of movement is along a diagonal. If so, the square must be occu-

Figure 5: Flowchart of the piece mover routine, MPIECE.

Note: The authors' complete Sargon chess playing program is available in book form. The documentation includes a complete Z-80 listing with detailed comments. The price is $15 from Dan and Kathe Spracklen, 10832 Macouba Pl, San Diego CA 92124, or from local computer stores for $17.95.
plied by an enemy piece. It may also be possible to move to the eighth rank in capturing, so pawn promotion must be considered here as well. Another type of diagonal pawn move is the *en passant* capture. It must be considered by a call to ENPSNT. Finally it is time to consider a new direction, as is done for the other piece types.

If, however, the direction of movement is forward, the "to" square must be empty. Pawn promotion must be checked for on forward moves. If the piece has never moved before, another move in the same direction is a possibility. Otherwise it is time to consider a new direction. Figures 5 and 6 are flowcharts of MIPECTΕ and PATH, respectively.

**The Other Move Generation Routines**

The move generation driver is GENMOV, the generate move routine. The basic function of GENMOV is to generate the move set for all pieces of a given color. It scans the board checking for a piece of the same color and calls MIPECĘ, the piece mover routine.

CASTLE and ENPSNT are also key routines in move generation. CASTLE checks the legality of both King side and Queen side castling. It adds them to the move list if legal. Basic checks must include:

- Has King moved?
- Is King in check?
- Has Rook moved?
- Are the intervening squares empty?
- Are any squares that the King passes through under attack?

ENPSNT checks for any *en passant* pawn captures and adds them to the move list if legal. The tests must include:

- On the fifth rank?
- Was previous move the first move for the enemy pawn?
- Is the enemy pawn on an adjacent file?

INCK, the check routine, performs the function of determining whether or not the King is in check. The basic method used is to scan outward from the King looking for attackers, by calling ATTACK.

The attack routine finds all attackers on a given square by scanning outward from the square until one of the following occurs:

- A piece is found that attacks this square.
- A piece is found that doesn't attack this square.
- The edge of the board is reached.

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In the case where this routine is called by CASTLE or INCHK, the routine is terminated as soon as an attacker of the opposite color is encountered.

ADMOVE adds a move to the move list. The move list is a linked list. Each move in the move list is stored in a 6 byte area. The meaning of each byte is as follows:

0&1 MLPTR — Move list pointer. A pointer to the next move in the move list. Used to facilitate sorting the list.

2 MLFRP — Move list from position. The board position from which the piece is moving.

3 MLTOP — Move list to position. The board position to which the piece is moving.

4 MLFLG — Move list flags.

5 MLVAL — Move list value. Contains the score assigned to the move in evaluation.

It is hoped that this introductory discussion will assist potential chess programmers in getting started. With the essentials of move generation out of the way, the fun part of evaluation can begin.

BIBLIOGRAPHY

In writing Sargon, it was our original intention to put together the first version without any research into the attempts made by others. In this respect Sargon is a unique creation. After competing in the Second West Coast Computer Faire, we began to investigate some of the literature. This bibliography presents some of the references we found most helpful, together with our evaluations.

1. Michie, Donald, On Machine Intelligence, Edinburgh University Press, 1974. Michie's book provides an excellent treatment of exchange evaluation. He uses the concept of an exchange polynomial for accurately determining the outcome of battles engaged on the board. The basic approach we used in XCHNG, the Sargon exchange evaluator, turned out to be surprisingly similar. Sargon's approach, however, is far less computationally complex. We highly recommend this reference to anyone planning to write a chess program without look-ahead.


3. Fine, Reubin, Ideas Behind the Chess Openings, David McKay, New York, 1943. Fine's book makes a great starting point for anyone contemplating the addition of an opening book. Although Fine does not present enough lines of play for a complete book, it does provide a good orientation to other references.


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Matrix operations are done but you don't need BASIC MAT functions; the matrix is fully explained later. Using charts and explanations, you can write the program in any form from assembler to BASIC and higher languages. Assembler will work faster since this is a "number crunching" program. The main constraints are memory and the ability to hold many arrays in main memory.

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<tr>
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<th>ASM</th>
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<td>250 nsec. chips</td>
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Circle 318 on inquiry card.
admittance value is also given; the program is required to calculate the admittance as part of analysis.

Review of Complex Numbers

If you are unfamiliar with complex number notation or admittance, some review is necessary before beginning any programming. Complex numbers exist in either rectangular or polar form; rectangular form is used here.

<table>
<thead>
<tr>
<th>Complex Number Arithmetic</th>
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| The rules for rectangular form arithmetic are shown in the table below. Note that division and inversion have equal value denominators for both real and imaginary parts. Finding the denominator first in the division routine will increase computational speed. Note also that inverting \((C + jD)\) is equal to dividing \((A + jB)\) by \((C + jD)\) and setting \(A\) at unity and \(B\) at zero.

Actual test equipment such as oscilloscopes present magnitude and phase angle. This is the polar form, and conversion is as follows:

Given rectangular form \(A + jB\),
magnitude = \(MAGN = A + B\) and
phase angle = \(PHA = (B/A)\).

Conversion from polar to rectangular form is:

Given polar form \(MAGN\) at angle \(PHA\),
real part = \(MAGN \times \cos(\text{PHA})\) and
imaginary part = \(MAGN \times \sin(\text{PHA})\).

Trigonometric functions in the language will determine whether angles are in radians or degrees. Most are in radians. The conversion factor from radians to degrees is:

\[
\text{Degrees} = 57.29577951 \times \text{radians}.
\]

Given Complex Numbers of \((A + jB)\) and \((C + jD)\)

Addition:
\[(A + jB) + (C + jD) = (A + C) + j(B + D)\]

Subtraction:
\[(A + jB) - (C + jD) = (A - C) + j(B - D)\]

Multiplication:
\[(A + jB) \times (C + jD) = (AC - BD) + j(AD + BC)\]

Division:
\[
\frac{A + jB}{C + jD} = \left[\frac{AC + BD}{C^2 + D^2}\right] - j \left[\frac{AD - BC}{C^2 + D^2}\right]
\]

Inversion:
\[
\frac{1}{C + jD} = \left[\frac{C}{C^2 + D^2}\right] - j \left[\frac{D}{A^2 + D^2}\right]
\]

Summary of complex arithmetic used for analysis.

This requires two floating point numbers for every complex number. The lefthand number is called the real component and the righthand number, separated by the \(j\), is called the imaginary component. Don't let the imaginary term fool you — it is very real. The naming comes from mathematical notation. [Note that electronics applications use \(j\) instead of the mathematical symbol \(i\) to avoid confusion with the symbol for current . . . BWL.]

Admittance is the reverse of impedance. You may be more familiar with impedance and the notation:

\[Z = R + jX\]

with \(X\) being reactance, either positive or negative. Admittance is:

\[Y = G + jB\]

with \(G\) being conductance and \(B\) susceptibility, either positive or negative. The relationship \(Y = 1/Z\) is true but there are special rules governing complex number mathematics. These rules are summarized in the text box on complex number arithmetic.

The circuit to be analyzed is converted into a model for the computer by copying each component as a branch. Each branch has two node numbers corresponding to connections in the circuit. All nodes above ground must have sequential numbering, beginning with 1, but the node numbers may be in arbitrary positions. A ground node is signified by 0.

A complete set of branch descriptions comprises a circuit list. The circuit list we use requires three integer values and two floating point values to completely define a node. The three integer values are for the connections to other nodes and for indicating what number node we are presently at. The two floating point values define the complex admittance of the branch. To be useful, the minimum number of branches available should be at least 20.

You will notice that signal sources are currents and not voltages. This and use of admittances are deliberate in the solution of a node voltage. Consideration of node voltage solutions is important for our analysis.

Fundamental Circuit Matrix

A simple resistor network is shown in figure 1. This circuit can be analyzed quickly using pencil and paper, but will serve to show the mechanism of solutions. Keeping this circuit in mind, inspect the general
EEs

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GENERAL ELECTRIC

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The conductance of 50 ohms is 0.02 mho, 25 ohms is 0.04 mho. The mho is also called the siemens. Using only the real parts of admittance and following the rules of table 2 yields the numeric forms:

\[
\begin{align*}
0.06 E_1 - 0.04 E_2 &= 1.0 \\
-0.04 E_1 + 0.08 E_2 &= 0
\end{align*}
\]

Solving for \( E_2 \) can be done by multiplying equation (1A) by 2/3 and adding the product to equation (2A) to give:

\[
E_2 = 12.5
\]

Substitution of \( E_2 \) into equation (1A) gives:

\[
E_1 = 1.50/0.06 = 25
\]

The preceding straightforward mathematics becomes impractical for models with many nodes. Note that the subscript rules of table 2 are different than the example just given. A slightly different matrix arrangement is actually used.

**Fundamental Properties of Matrices**

Mechanization of the solutions requires a matrix in two dimensions having \( N \) rows and \( N+1 \) columns, \( N \) being the highest node number in the model. The first subscript is the row, and the second is the column position. The rightmost column is used only for signal sources.

Figure 3 shows the example represented in figure 2.

The mathematical matrix form and the simultaneous equations form are identical. Mechanizing the solution will require parts of both forms. Admittance subscripts will depend on node numbers (in the branch list) and follow certain rules depending on type. Those rules are given in table 2.
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BASIC-E Compiler

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Especially suited to educational applications, EMPL is an adaptation of APL, using the ASCII character set. This 8K version occupies the first 5376 bytes of memory and operates in two modes. The Execution Mode permits all instructions to be executed immediately. The Definition Mode permits the user to enter functions. EMPL on Tarbell Cassette with manual is $15.00. (Copyright 1977 Erik Mueller).

SPOOLER

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**CP/M is a trademark/tradename of Digital Research.
by an array of two rows (maximum node number is 2) by three columns. Variable name M has been used for any matrix position. At the beginning of a solution all Ms are set to 0. The branch list is then inspected, values calculated and added or subtracted into the matrix array positions according to the rules of table 2.

The variable N is used to denote a numerator value. D denotes a denominator value of a multiplying factor. A circle indicates that the array variable is multiplied by the factor; an arrowhead indicates that the product is subtracted from the array position. Only arrowhead marked positions are changed; all others are extracted and held in temporary storage.

Numeric values in figure 3 are the same as our simple example. The forward operation has these steps:

\[
\text{Multiplication factor} = \left( \frac{M_{2,1}}{M_{1,1}} \right) = -0.66667.
\]

\[
\text{New } M_{2,2} = M_{2,2} - (\text{MULT.FACT} \times M_{1,2}) = 0.05333
\]

\[
\text{New } M_{2,3} = M_{2,3} - (\text{MULT.FACT} \times M_{1,3}) = 0.66667
\]

Note that the steps are equivalent to finding \(E_2\) by conventional mathematical operations. The back operating steps are the same as those for finding \(E_1\) and are:

\[
\text{Final node voltage solutions are indicated by numbered subscript } N_s \text{ and } D_s \text{, where the subscript stands for the node of solution.}
\]

We have used a slightly different number handling scheme and have arrived at the same solution. This technique can be expanded to larger arrays in order to provide an algorithm that solves all node voltages. It should be noted that solutions provide node voltages with reference to circuit ground; modeling techniques allow finding the voltages between nodes.

A consideration for programming is array size. The array consumes \(2 \times NMAX \times (NMAX + 1)\) floating point variables with NMAX referring to the maximum number of nodes allowed in any circuit. The actual physical size of the array is twice as large since both real and imaginary parts of the complex number must be stored. The example showed only real parts.

Final Matrix Solution Algorithm

A flowchart for the MATRIX solution algorithm is shown in figure 4. The routine assumes that all admittance values of a circuit have been calculated using the formulae in table 1 and have been entered into an initially 0 matrix at positions according to the rules of table 2. Figure 5 is a pictorial of a 4 node solution sequence using the same symbology as figure 3. The pictorial assumes that the optional tests in figure 4 are not performed. This will give voltage solutions to all nodes.

IBM's venerable ECAP program yields all node voltages at each frequency. While useful, it can be difficult to interpret. A better way is to command the program for a specific node of solution (NS in the flowchart). The matrix must be solved at each frequency, so including the optional tests will reduce the number of back solutions to a minimum. A solution printout can then be made of all node voltage data at one node for the desired frequencies.

Calculation speed is increased by inverting the denominator in the outer loop. Division is invariably one of the most time-consuming functions; the inverted denominator allows multiplication instead of time-consuming division.

Another timesaving technique, not shown, is to include a 0 test of numerator
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M(K,J) in the optional section. A 0 numerator will have no effect on inner loop variables, so a bypass could occur on Os. (Remember to check both the real and imaginary parts of Os.) Many circuits will have only about one half array positions nonzero, so this test will help running time.

A similar test can be made by bypassing the inner loop if M(J,I) is equal to 0. This helps reduce running time on large node circuit models; at 20 nodes or less, the help is arbitrary. All such tests take time, so it is worthwhile to perform these tests outside the inner loop since the inner loop iterates the most.

It is interesting to note where the node voltage solution numerators and denominators are located. Numerators are always in the righthand or generator column. Denominators are always in the main diagonal from upper left to lower right. Row position is equal to node of solution. Highest node numerators and denominators are always found; back solution is required only for nodes less than the highest node. The back solution algorithm is called the Gaussian elimination or Gauss-Jordan method of solution.

Complete Frequency Solution

The flowchart shown in figure 6 is the ANALYSIS routine. This routine assumes that the admittance of each branch, Y, is already calculated. Before the matrix branch values can be calculated, the entire matrix is set to 0. Zeroing the matrix will allow simple addition and subtraction in the matrix fill section.

Variable W is the frequency in radians per second. Variable W1 is the negative inverse of W. These simplify admittance calculations. An often used constant is 2π which should be stored as a single variable. Variable F is the solution frequency.

Variable Y is the calculated complex admittance for passive branches but is the stored value of current for generators. Variable M is the two-dimensional complex matrix array used in figure 3, and variable S is the solution matrix, which is capable of storing complex values. Variable L is the subscript value for array S.

Most of the flowchart involves an examination of each branch, calculation of the admittance, and addition or subtraction of that value into the matrix. Positioning tests seem to be rather complex, but they do follow the rules of table 2. The flowchart and table 2 can be expanded to fit a special branch type.

Current flow of a generator branch is determined by node number entry order. This will be illustrated further under modeling techniques. A generator with one node set to zero will enter the matrix at only one position. If both nodes are nonzero the generator will enter the matrix at two positions.

Passive branches can have arbitrary node ordering. The test flow allows for this. One node specified as 0 will cause calculated admittance to add at only one matrix position. If both nodes are nonzero, calculated admittance will add at two positions and subtract at two other positions.

To check the node test flow, go back to the example of figure 1 and the matrix values shown in figure 4. Remember that admittance, matrix and solution arrays of figures 4 and 6 require handling two floating point values per complex number. There is no way around this fact.
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Branch Types and Passive Calculations

Small systems need simple rules, so it is probably easier to identify branch types in storage by integer numbers. One is sufficient. The number of different types should be considered in terms of calculation code and analysis needs.

Multicomponent branch types are strongly recommended since they reduce the number of nodes required in a model. Multicomponent branches are given in table 3 in terms of ohms, farads and henries stored in the branch list. List array storage positions should be considered in regard to the calculations.

Radian frequency, \( W \), and its inverse negative, \( W_1 \), are from the single frequency analysis routine. All of the parallel combinations are calculated as impedances first and then inverted. Series combinations should require less coding if calculated as impedances first; this can be seen by comparing table 3 with the complex values given in table 1.

Direct admittance calculations may be slightly faster for series combinations. The choice is determined by the amount of memory, possibly by external memory control. All analysis matrices should be in main memory when ANALYSIS is called.

Passive Branch Values at DC

Direct current (DC) analysis can be considered as analysis at 0 Hz. Resistances remain the same but capacitors have 0 susceptance. Their susceptance (imaginary part) is effectively bypassed. Single inductors should have their susceptance value replaced by a low resistance, say a hundredth of an ohm (100 mhos susceptance), to avoid calculating difficulties. In actuality, inductors have finite resistance at DC.

Series combinations can be bypassed for certain types. A series resistor-capacitor (RC) or inductor-capacitor (LC) branch will have 0 admittance. In a series RL branch calculation, the susceptance calculation can be omitted and only the conductance calculation performed. Parallel combinations are also modified. A parallel RC branch requires only the conductance calculation. Parallel RL or LC branches would have the nominal values.

Table 3: Calculations showing how a multicomponent branch admittance calculation is performed. The three series calculations (RL, RC, CL) are actually impedance calculations since they are so much easier to perform. To obtain the admittance, perform the complex inversion \( Y = 1/(R+jX) \).
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ANALYSIS

SET MATRIX TO ZERO

W = F x 2πm
W1 = -1(W1)
K = L

PI = PLUS NODE
NI = MINUS NODE

GET TYPE INDICATOR

PASSIVE TYPE

YES

P2 = NMAX+1
Y = GENERATOR ADMITTANCE

NO

SUBTRACT Y FROM M(P1,N2)

P1 = 0

NO

P2 = 0

YES

ADD Y TO M(N1,N2)

NO

P1 = 0

YES

ADD Y TO M(P1,P2)

NO

P2 = 0

NO

SUBTRACT Y FROM M(N1,P2)

K = K+1

NO

K > NMAX

YES

MATRIX

MATRIX SOLUTION

S(L) = M(N5,NMAX+1)/M(N5,N5)

RETURN

SERIES TYPE

YES

CALCULATE Z INVERT FOR Y

NO

CALCULATE Y

N2 = 0

YES

NO

Figure 6: The ANALYSIS routine, which performs the setup for the MATRIX solution routine. ANALYSIS checks what type of branch is under analysis and calculates the admittance according to the formula of table 1. This value is then inserted into the matrix according to the rules of table 2. When all the nodes have been checked, MATRIX is called to perform the solution.
The Electric Pencil II is a Character Oriented Word Processing System. This means that text is typed in as a string of continuous characters and is manipulated as such. This allows the user enormous freedom and ease in the movement and handling of text. Since line endings are never delineated, any number of characters, words, lines or paragraphs may be inserted or deleted anywhere in the text. The entirety of the text shifts and opens up or closes as needed in full view of the user. The typing of carriage returns as well as word hyphenation is not required since lines of text are formatted automatically.

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<td>VIO</td>
<td>Diablo 1610/20</td>
<td>$300</td>
</tr>
<tr>
<td>NS-1</td>
<td>SOL</td>
<td>NEC Spinwriter</td>
<td>$275</td>
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<tr>
<td>NV-1</td>
<td>VDM</td>
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<tr>
<td>SSN</td>
<td>SOL</td>
<td>Hellos/TTY</td>
<td>$250</td>
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<tr>
<td>SNN</td>
<td>SOL</td>
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<td>$250</td>
</tr>
<tr>
<td>DSH</td>
<td>SOL</td>
<td>Hellos/Diablo</td>
<td>$300</td>
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</tbody>
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UPGRADING POLICY: Any version of The Electric Pencil may be upgraded at any time by simply returning the original disk or cassette and the price difference between versions plus $15.00 to MSS. Accept only original media at time of purchase.

Electric Pencil I is still available for non CP/M users:

<table>
<thead>
<tr>
<th>Vers</th>
<th>Video</th>
<th>Printer</th>
<th>Cassette</th>
<th>Disk</th>
<th>Drive</th>
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<td>SS</td>
<td>SOL</td>
<td>TTY or similar</td>
<td>CUTS</td>
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<td>VTI</td>
<td>TTY or similar</td>
<td>Tarbell</td>
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<td>$100.</td>
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<td>SV</td>
<td>VDM</td>
<td>TTY or similar</td>
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<tr>
<td>SNN</td>
<td>SOL</td>
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<td>North Star</td>
<td>$175.</td>
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Figure 7: The SWEEP routine, used to perform a number of analyses on a particular circuit over a frequency range. Two types of sweeps are possible: linear and logarithmic. The variable DELTA is used as an increment and also as an indicator of which type of sweep analysis is to be performed. If DELTA is negative, a logarithmic analysis will be performed; if DELTA is positive, a linear analysis will occur.

100 mhos conductance specified above. In all branches at 0 Hz the susceptance would be 0.

Frequency Sweeping

For this analysis, minimum and maximum analysis frequencies must be specified plus an increment. Most solutions over a narrow range will have a small increment but it is often useful to have a logarithmic frequency sweep with wide bandwidths. The main program should have a command point to which all major routines return. Frequency range can be selected at this command point with a minimum (MINF), a maximum (MAXF) and an increment (DELTA).

A choice between linear and logarithmic sweep can be done by simply checking for a negative or positive DELTA. A positive DELTA is the incremental change for a linear sweep, and a negative DELTA can be the frequency interval multiplier. The multiplier can be precalculated for the number of frequencies per decade:

\[ \text{DELTA} = - \left( \exp \left( \frac{2.302585}{\text{NFD}} \right) \right) \]

which reduces to

\[ \text{DELTA} = -10^{\left( \frac{1}{\text{NFD}} \right)} \]

where NFD is the number of frequencies per decade and \( \exp \) is a function to raise \( e \) (the base for the natural logarithms which is approximately 2.71828) to the power of the following argument. For example, twenty

<table>
<thead>
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<th>Row</th>
<th>Column</th>
<th>Enter into Array by</th>
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<tbody>
<tr>
<td>Plus node</td>
<td>Dependent branch minus node</td>
<td>Addition</td>
</tr>
<tr>
<td>Plus node</td>
<td>Dependent branch plus node</td>
<td>Subtraction</td>
</tr>
<tr>
<td>Minus node</td>
<td>Dependent branch plus node</td>
<td>Addition</td>
</tr>
<tr>
<td>Minus node</td>
<td>Dependent branch minus node</td>
<td>Subtraction</td>
</tr>
</tbody>
</table>

Table 4: Turning a dependent branch into a dependent current source. The source is entered into the matrix by the stated rules. Remember that any row and column combination with a zero node will not enter the matrix.
frequencies per decade would have a DELTA equal to -1.122018.

Figure 7 is the flowchart for a frequency sweep analysis routine. The option of storing results or printing them directly depends on the operating system and memory. Subscript L is used only for solution matrix purposes.

There is a caution to be observed with solution storage: the number of frequencies to be analyzed must not exceed the storage matrix size. Other storage matrices may be written over if no check on the total number of frequencies analyzed is made. This is a very easy error to make.

Branch Switching

Implementing this function is useful for circuit modeling. In effect it allows you to disconnect or reconnect a branch from analysis and yet retain it in the branch list. It is the same as removing or replacing a component in a breadboard. If removed, it is still on the bench and can be installed later.

There are two easy ways to implement switching. Since we are using a numeric value to designate the branch type, we can define a positive value as a connected branch and a negative value as an open branch. Another method is to devote one byte per branch with a numeric value of +1 if connected and 0 or -1 if open. Another test can be inserted in the ANALYSIS routine of figure 6, just before the passive type? test. An open condition would bypass any calculations and go on to the next branch.

Dependent Current Sources

This branch type, not mentioned before, enables a model to duplicate transistors or operational amplifiers. It is a current source dependent on the voltage across another branch and is specified by a gain factor called transconductance. The symbology and matrix entry rules are given in table 4.

Transconductance is specified in mhos and is equal to the current divided by the voltage. Branch value entry is the transconductance, and admittance calculation for solution takes this as the stored value for the real part with an imaginary part of 0. You can think of transconductance as a current gain factor. A transconductance of 0.1 with a dependent branch voltage of 24 V produces a dependent source current of 2.4 A. A transconductance of 1.0 gives 24 A.

You do not have to be concerned about the dependent branch voltage. The matrix entry and solution will determine the current from the specified transconductance. The direction of electron flow is another

---

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factor and is determined by node number entry order of both the source and dependent branch. Reversing plus and minus node numbers of the source will reverse the source's flow; reversing node numbers of the dependent branch has the same effect; and reversing both source and dependent nodes returns electron flow to the original direction in the source.

One node of either source or dependent branch may be 0. Inspection of matrix entry subscript rules will show this. The only problem left is to allow the program to identify the dependent branch for subscripting.

Dependent Branch Identification

All passive components and generators may be entered into the branch list in any order. The ANALYSIS routine of figure 6 scans the entire list in order to fill the matrix for solution. A dependent source should be allowed to enter the list either ahead of or behind its dependent branch.

Two options come to mind. The extra integer byte mentioned under branch switching can be used to identify the dependent branch number in the list. Since transconductance is specified as the real part only, the second value storage might be used to hold the dependent branch number. Make sure that the particular floating point storage method that you are using will not change the value of the integer slightly. If there is
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Book 3: Half adders and full adders; subtractors; serial and parallel adders; processors and arithmetic logic units (ALUs); multiplication and division systems.

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any doubt about whether your floating point to integer conversions are totally accurate, use the extra integer per branch for both switching and dependent branch identity. A dependent source can be switched by signing the extra integer. This method will be assumed for all further discussion.

Entering branch data in the list requires an extra entry for dependent sources to identify the dependent branch. The ability to print out a branch list should also include printing the dependent branch number.

Modification of the ANALYSIS routine to handle dependent current sources is shown in figure 8. This modification also includes the switch function with the extra integer SW acting as the switch and identifier of dependent branch list number.

Impedance Analysis

All analysis procedures have so far given only voltage solutions. The last analysis we will consider is readily determined by disregarding all generators, placing a value of unity in the proper generator column position and then solving the matrix as before.

This may seem too simple. To understand it, consider once again the circuit of figure 1 and the position of solution numerators and denominators. Denominators always lie in the main diagonal and numerators always lie in the generator column. Impedance analysis will have only one generator column entry since all other generator branches automatically bypass any entry into the matrix.

A unity current is simply \((1.0 + j0)\), 1 A with no phase shift. This is the condition of figure 1 if an impedance is desired at node 1. The resistance of the total figure 1 circuit looking into node 1 is simply 25 ohms. In the model all generators are pure current sources; that is, they have no admittance themselves and can therefore be disregarded.

Addition of impedance analysis is shown in figure 9, a modification of figure 8. A flag variable must be held in the main program to identify analysis type. It is considered to be on for impedance and off for voltage analysis. It can be logical, integer or a single bit, but must be available if both types are desired.

Implementing impedance analysis requires a solution at only one node. It is best to use the optional tests in the flowchart of figure 4 and have all solutions at only one node. Direct printouts of impedance will be in rectangular form but the polar form can also be printed at the same time by using temporary variables and form conversion. Both forms are useful in studying analysis.

REFERENCES


Text Editing System
This is the most complete and versatile editor available for the 6800 or 8080 micro. The system is line and content oriented for speed and efficiency, and features such commands as block move and copy, append and overlay, as well as string manipulators. The 6800 version requires 5K beginning at 0 hex, the 8080 needs 8K starting at 1000 hex. Both should have additional file space as required.

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Figure 7: The author's algorithm for solving the eight Queens problem, in which eight Queens are to be placed on a chessboard so that no Queen attacks any other Queen. (In chess, the Queen can capture any piece that is in direct line with it horizontally, vertically, or diagonally.) The method consists of placing the first Queen on the lower left-hand corner square. Markers are placed on all squares that the Queen can attack (a). Moving one column to the right, another Queen is placed on the first empty square from the bottom. Markers are again placed (b). The process is repeated. Eventually, either the problem will be solved or there will be no more spaces for one or more Queens; (c) illustrates the latter situation where corrective action is taken by altering details of the trial solution.

Solving the Eight Queens Problem

The eight Queens problem is a chess related puzzle, the object of which is to place eight chess Queens on an 8 by 8 chessboard in such a way that no Queen can take another. (For the benefit of nonchessplaying readers, the Queen can capture any piece that is in direct line with it horizontally, vertically, or diagonally. No detailed knowledge of chess is required in order to understand the rest of this article. . . .CM) 8 is the maximum number that is not obviously impossible, since 9 would force one Queen to be in at least one other Queen's row or column. I will explain how I solved this problem using a computer, since a look into the mind of a problem solver from start to finish might help you with your own problems.

The First Method

The first method I tried was to place the Queens at random on the board and check the board for a proper position. There are 64! / 56! or 1.7846289 x 10^14 such permutations. I would never have thought about this except that I grossly overestimated the speed of the IBM 370 (the machine on which I was working). Even 370s have their limits, I was to discover. If the 370 evaluated 10,000 positions per second, it would have taken 565 years to find all the answers, and then only if I could have written a program that would create all the permutations one after another with no duplications. This is very difficult. I tried writing one and failed. If you can actually do this, I'd like to see it.

The Second Method

I then divided the board into eight columns and placed one Queen at random in each column and realized that with one Queen in each column, I could represent any permutation with an 8 digit number, each digit representing the position of one Queen in its column. Since no two Queens could have the same column position (for example, if the leftmost Queen was at 1 or the bottom, obviously no other Queen could also be at the bottom), what I needed was a list of permutations of all numbers from 1 to 8. With this method I would have to check only the diagonals; much of the work would already have been done. This also reduced my problem to 8! or 40,320
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Circle 271 on inquiry card.
10 DIM A(8,8),A$(10),F(8)
11 FOR T=1 TO 10
12 READ A$(T)
13 NEXT T
14 DATA "0","1","2","3","4","5","6","7","8","9"
20 C=0
30 C=C+1
40 IF C=9 THEN 250
50 FOR E=1 TO 8
60 IF A(C,E)=0 THEN 220
70 NEXT E
80 GOTO 330
89 F(C)=E
90 A(C,E)=0
91 D=1
92 GOSUB 100
93 GOTO 30
100 FOR X=-1 TO 1
110 FOR Y=-1 TO 1
120 IF X*Y+X+Y=0 THEN 220
130 FOR Z=1 TO 8
140 A=C+Y*Z
150 B=E*X+Z
160 IF X=8 TO 1 STEP -1
260 FOR Y=1 TO 8
270 IF A(Y,X)=-1 THEN 290
280 PRINT A$(A(Y,X)+1);;
281 GOTO 300
290 PRINT
300 NEXT Y
310 PRINT
320 NEXT X
321 PRINT
330 REM NO SPACES, NOW WHAT?
340 C=C-1
350 A(C,F(C))=0
360 E=F(C)
380 D=-1
390 GOSUB 100
391 IF E=8 THEN 340
400 FOR X=E+1 TO 8
410 IF A(C,X)=0 THEN 440
420 NEXT X
430 GOTO 340
440 A(C,X)=1
441 F(C)=X
450 D=1
451 E=X
480 GOSUB 100
470 GOTO 30
480 END

Listing 1: A BASIC program for solving the eight Queens problem.

1.7846289 x 10^14 or even 8^8. But a program to create all these numbers? Much later I discussed this with some friends whom I consider to be software experts. They shook their heads saying, "This is a difficult task." They were right, for it turned out, I had to give up. An easy solution just wasn't going to work.

Final Method

A determined human, after trying permutations and finding the problem is not trivial, would get a set of pawns to represent Queens and, using pennies for markers, attempt to find a solution by placing a Pawn (to represent each Queen) on a chessboard and a penny on each square that comes under that Queen's influence. By inspection (s)he would determine where to put subsequent Queens. A methodical procedure would be as follows (I have shown in parentheses the line in the program which is relative to the step in the manual solution):

Place a Queen in the lower lefthand corner of the board (line 90) and then, on all the squares that would come under that Queen's influence, place one penny (GOSUB 100, D=1). Then moving one column to the right (line 30), place a Queen on the first empty square from the bottom. This entails having to move up two squares. Place a penny on each square (even the ones already marked) in this Queen's domain. You'll see why in a minute. Continue moving right and repeating this algorithm until you hit a column that is all pennies (line 80). You use a lot of pennies here. If you run off the righthand edge of the board (line 40) you have solved the problem. However, you probably won't find one the first time. Three columns from the end you will have to stop, having run out of spaces. Now you remove the latest Queen (line 350) and then remove one penny from each of its dominion squares (line 380, GOSUB 100 D=-1). This is why you placed pennies on already covered squares because if you didn't, you wouldn't know if the penny there was the subject Queen's or not. Continuing from the subject Queen's square (line 400) look up the column for a new blank spot (line 410) to place a new Queen and continue. If there are none or if your last Queen was at the top of the board (I check for the top first, line 391), move back one column (line 340 again). Remove that Queen and remove her pennies, and check for blanks above, etc. If you are trying this by hand now you will have noticed how slow and messy it is. It was only the feelings of frustration from the manual simulation that kept me moving on this seemingly hopeless computer simulation.

The final program started off at half its present length and I spent three days repairing it by adding one line after another as it failed time and again. I added line 391 to eliminate a subscript error.

I was beginning to get worried because the program was twice its original size and I was no longer capable of understanding it at a glance. I typed RUN for the 100th time and waited for the next error. My method of repair depended on my being able to comprehend the program. I added several GOTOs and I knew I couldn't keep it up much longer.
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Suddenly to my amazement, the printer started to hammer out the solutions as fast as it could! I peeled off the paper to check the first one by hand and it was right! I include the final program exactly as it was written, a blow to the cause of structured programming and a glorious victory for dumb luck. If you want to try it, go ahead, but be forewarned that only on the Humber College VM370-135 CMS system was the solution instant. On a Heathkit H8 it took 20 minutes for the first solution and 5 minutes for the next. There are 92 solutions of which 23 are discrete. So beware! I feel this is the most efficient algorithm possible. (Using brute force to generate and file all those 40,320 8-digit numbers, and having the computer run through them probably qualifies for the epithet "inefficient.")

The eight Queens problem was a challenge, and the pleasure of beating it was tremendous. I feel the approach described here demonstrates a good heuristic for general problem solving, which is: don't check all the other situations in search of a solution, but custom design your own situation to match your specifications. I think now I'll see if I can place eight Maharajahs (a piece combining the Queen and Knight moves) on a board. Excelsior!

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Assembling the H9 Video Terminal

Photo 1: The most exciting part follows the construction of a good portion of the chassis, power supply, high voltage circuits and the character generators: the terminal is fired up for the first time, and the pleasant aura of success is evident in the display. The deflection yoke has yet to be aligned to produce horizontal rows of characters, but just the fact that characters appear at all is exciting.

Photo 2: Several steps later in the manual, the deflection yoke has been carefully twisted around the neck of the cathode ray tube to produce horizontal rows of null ("?") characters.
I have just completed one of the more satisfying electronic experiences in my life. I think a lot of the feeling is a result of everything working the first time. Everyone should have such an experience at least once every ten years. More often is preferable, but Murphy's Law usually prevents it. I have just finished assembling the Heathkit Model H9 video terminal.

At first I thought that everything worked the first time because of my great skill as an assembler. However, as a long time Heathkit builder (automotive testers, amateur radio equipment, and now microprocessor equipment), I have sensed something better about this kit and its construction manual. While they appear in the familiar and efficient format of past Heathkits, there is something which made them easier to follow, and therefore help to contribute to the "works the first time" result. First, the printed circuit boards are clearly and legibly marked. Double and triple referencing of all components by manufacturer's part number, Heathkit part number, and reference designation made part location much easier, faster, and more accurate. The only place where something might go wrong is in the placement of integrated circuits and diodes (correct placement of pin 1 and band). Second, each printed circuit board is electrically checked as soon as it is completed. It is much easier to check each board as it is completed (there are six printed circuit boards to build) than to troubleshoot the entire finished unit. Each check assures that the board is functioning in a go or no go sort of way. Generally, you can be assured the unit is working up to the point of inserting the last printed circuit board. If something does not work, you can assume it was the last board added. This cuts down troubleshooting time. Resistance checks at each board completion (before applying power) further assure that you will not do severe damage to a board because of shorts or integrated circuits installed backwards.

The entire building procedure took me about 18 hours [but reports from other builders, such as yours truly, indicate that it can take as long as 40 hours. . .CH]. Sometimes you just get hooked and can't quit. This also contributes to the little mistakes which cause things not to work the first time. As Heathkit advises, if you get tired, quit and go rest. I might mention that this is the prime reason previous Heathkits, which I assembled, did not work. At 2 AM diodes and integrated circuits can go in backwards very easily and wires can get soldered to the wrong places.

The chassis took about two and a half hours to set up. A lot of mechanical as-
Photo 3: One of the most tedious tasks when assembling the H9 is manually checking each switch of the keyboard. Here, two metal cake pans are used as input (background) and output (foreground) of the process of checking each switch with an ohmmeter.

Photo 4: After soldering the switches to the keyboard printed circuit board, each switch must be individually tagged with a preprinted self-sticking key identification. The key identification fits into a recessed flat area on the upper side of the keytop.

Photo 5: Eventually all the keys are marked properly and the completed keyboard is ready for installation.

assembly, as opposed to electrical assembly, is required. I hardly used my soldering iron, except to make the occasional small cable assembly. The major cable assemblies are already assembled and supplied in the kit. I thought I would never run out of plugs to put into the chassis, and interconnect. There seemed to be a lot of them. All are necessary to support and interconnect the seven printed circuit boards, and to interface to the outside world.

The power supply circuit card was the first electrical assembly. It went very fast, half an hour, and after resistance checks, it fired up and regulated beautifully. The tests at this point check the regulators on the circuit card, and also check the power wiring on the chassis.

The character generator circuit card was also quickly assembled. The testing at this point was a resistance check, and voltage measurement after power on. The video circuit card must be completed before you can be assured that the character generator board is working. The video circuit card took just a little longer, but then it was just a little bigger.

The next part of the assembly was one of the most enjoyable (enjoyable only if it works; remember Murphy). Even though less than half of the circuit cards were assembled and installed, there were enough to fire the terminal up to see how it worked. The cathode ray tube was installed, more mechanical work. Not too hard, but a little time consuming, as well it should be. It is not wise to be careless with a cathode ray tube. It can implode and must be handled carefully, as noted in the manual. Temporary jumpers, supplied with the kit, are used to set up the character generator and video cards. If all is going well, when you turn the power switch to on, twelve rows of 80 "7" characters with underlines appear magically on the screen (see photo 1 and photo 2). I couldn't believe it when it worked just as the manual said. It was 3:30 AM and I went to bed a very happy person.

Next day started with the keyboard circuit card. This was the most time consuming board to assemble, with lots of pushbuttons to test and install (see photo 3, photo 4 and photo 5). There were also a large number of jumpers to install. I would almost pay a few dollars more for a double sided printed circuit board rather than put in all those jumpers. The pushbuttons have a much better feel to them than what I had expected. My wife contributed significantly by inserting the logos onto the top of each key. The keyboard resistance check was made and power applied. Behold, I could make
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letters and numbers appear on the screen (photo 6).

The memory and counter circuit card was next, the board with the most integrated circuit sockets to solder in. As in all sub-modules of a Heathkit, the assembly process begins with a parts tally (see photos 7a and 7b). It takes a while. However, look at the positive side; I personally would rather solder in sockets than try to remove even one soldered in integrated circuit. Sockets for each and every integrated circuit on every board are supplied.

The final board to be assembled is the IO circuit card. It does not take too long to build, but the most impressive thing here is the schematic. Working professionally with microprocessor systems, one of the biggest problems I've run across is interfacing. Heathkit has designed one of the most flexible IO cards I have ever seen. Serial RS-232, TTL, and 20 mA loop are all jumper selectable. Parallel IO is also included.

The timing and processing unit circuit card is preassembled, tested, and calibrated by Heathkit. It is simply plugged in. The final adjustments are easily accomplished. A good VOM or VTVM is all that is required through the whole procedure, with ranges of 10, 100 and 1000 ohms for resistance measurements.

One final electrical note: there have been reports of blown Darlington transistors because of insufficient current limiting. While this fix was not in the manual when I assembled the H9, the friendly guys at the local Heathkit store provided both the information and the components to effect it. Readers with H9 kits should check to make sure that this fix is present.

Reflecting on the H9 design, I found two things I do not like. 12 rows of data does not seem sufficient. Anyone writing software and needing to see more than the last 11 statements will feel limited. This is offset a bit by the short form mode which creates four columns with 12 rows and 20 characters. Now 48 statements, rather than 12, can be displayed at once if they are all less than 20 characters long. The second thing I found disconcerting was that the characters displayed on the video screen were slightly blurred on the left and right edges of the picture. After playing with the adjusting magnets, and other adjusting controls, this was minimized. It is barely noticeable through the front protective screen.

Other controls include page or scroll selection, independent cursor controls, erase page, erase to end of line, automatic line carry over selection (automatic return to next line after 80 characters), controls for timeshare (half or full duplex, transmit page, break). Serial and parallel interfaces, adjustable to rates between 110 and 9600 bps, are very flexible and functional. Un-
fortunately, few of the standard ASCII formatting commands are decoded: if you want to clear the screen from your computer, 12 line feeds in a row is about the only way to do it, in spite of the fact that an equivalent key is available.

After searching for several months, I was very pleased to find an 80 character per line terminal with so many functions. I saw units that cost 50 to 70 percent more which did not have the features of the H9. The documentation is equal or better than past Heathkits. Physically, it looks professional and is clean and neat. It would be hard to find a unit so flexible for the investment. I use mine with a modem for timesharing as well as using it as a terminal for my home microprocessor system. And what’s more, it worked the first time.

Photo 7a: A good practice when assembling complicated kits is built into the Heathkit manuals: a parts check off. In this photograph, the parts for the “RAM and counter circuit board” have been unpacked from the paper bags, with loose parts placed in the baking pan at the left.

Photo 7b: As the parts are checked off against the parts list, they are moved from the pan at the left into the pan at the right, and arranged in order for access later during assembly. In this photo, the circuit board for the new module and a conductive foam pad with the integrated circuit parts are both placed at the back of the two pans.
Maze

Robert J. Bishop
1143 W Badillo St
Covina CA 91722

Here is an interesting novelty program that you can leave running on your video display whenever you are planning to have guests over to see your computer. The program automatically generates and displays a different maze about once a minute on an Apple I computer. Each maze is 11 squares high and 19 squares wide, and has only one path through it. The size, 11 by 19, was chosen so that a display with 24 lines of 40 characters each would just fill the screen.

Basically, here's how the program works. The entrance and exit points are randomly chosen first. Next, a random walk is performed from both of these points until the two paths cross. This determines the one, and only one, way through what will become the maze. As each "cell" is visited via these random walks, the location of the cell is placed in a queue. A queue is simply a list of items in which all insertions are made at one end, and all accesses are made from the other end, i.e., it’s a first-in-first-out (FIFO) list. When either of the walks runs out of places to go (gets stuck in a corner, or gets boxed-in), it goes back to the queue and restarts from the node indicated by the next item in the queue. This restarting process continues until the queue becomes empty, at which point the maze is complete. The resulting maze is then displayed, and the whole process starts over again.

The program is written in Apple BASIC and requires less than 2 K bytes of memory; an additional two pages (512 bytes) are required for the queue and grid array. Along with the BASIC interpreter the whole thing easily fits in 8 K bytes. In order to conserve space, the grid array and the queue are accessed via PEEK and POKE functions. The queue, indicated by the variable Q in the program, is located starting at decimal location 768; the grid array G starts at decimal location 1024. These values are set in line 100 of the program. Each of these

Figure 7: Two typical mazes as generated by the program of listing 1. A series of these will entertain you for hours and furnish you with another response to that age old question, "What do you do with it?"

Here is an interesting novelty program that you can leave running on your video display whenever you are planning to have guests over to see your computer. The program automatically generates and displays a different maze about once a minute on an Apple I computer. Each maze is 11 squares high and 19 squares wide, and has only one path through it. The size, 11 by 19, was chosen so that a display with 24 lines of 40 characters each would just fill the screen.

Basically, here's how the program works. The entrance and exit points are randomly chosen first. Next, a random walk is performed from both of these points until the two paths cross. This determines the one, and only one, way through what will become the maze. As each "cell" is visited via these random walks, the location of the cell is placed in a queue. A queue is simply a list of items in which all insertions are made at one end, and all accesses are made from the other end, i.e.: it's a first-in-first-out (FIFO) list. When either of the walks runs out of places to go (gets stuck in a corner, or gets boxed-in), it goes back to the queue and restarts from the node indicated by the next item in the queue. This restarting process continues until the queue becomes empty, at which point the maze is complete. The resulting maze is then displayed, and the whole process starts over again.

The program is written in Apple BASIC and requires less than 2 K bytes of memory; an additional two pages (512 bytes) are required for the queue and grid array. Along with the BASIC interpreter the whole thing easily fits in 8 K bytes. In order to conserve space, the grid array and the queue are accessed via PEEK and POKE functions. The queue, indicated by the variable Q in the program, is located starting at decimal location 768; the grid array G starts at decimal location 1024. These values are set in line 100 of the program. Each of these
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F10
arrays requires one 256 byte page of memory.

If you have a random access display (if your hardware lets you change displayed characters without having to regenerate the complete display), you might want to modify the program to become an interactive game. After the maze is displayed, let players try to move some type of cursor through it before a set time limit is reached.

Listing 1: An Apple I BASIC listing of the maze program. This program should be easy to convert to any BASIC language which uses PEEK and POKE functions.

10 DIM A(3), B(3), C(3), E(4), N(2)
20 E(1)=1; E(2)=2; E(3)=4; E(4)=8
100 P=768; G=1024; R=-1; F=-1; M=0; L=2
120 FOR K=1 TO 209: POKE G+K-1,0: NEXT K
140 N(1)=3+ AND (7) ; N(2)=205-RND(7)
160 POKE G+N(1),2; POKE G+N(2),24
180 P=N(1); GOSUB 1000; P=N(2); GOSUB 1000
200 L=3-L; P=N(L)
250 GOSUB 3000: IF P<0 THEN 350
300 GOSUB 1000; GOTO 400
350 GOSUB 2000: IF P<0 THEN 500
400 FOR K=1 TO 24: PRINT: NEXT K
350 GOSUB 1000; IF P<0 THEN 500
500 FOR K=1 TO 24: PRINT: NEXT K
510 FOR K=1 TO 11
520 FOR L=1 TO 19
540 T=PEEK (G+19*(K-1)+L-1)/2
560 O$="": IF T=2*(T/2) THEN O$="":""
590 PRINT "":RETURN
600 NEXT L: PRINT "":RETURN
620 FOR L=1 TO 19
640 T=PEEK (G+19*(K-1)+L-1)/4
660 O$="": IF T=2*(T/2) THEN O$="":""
680 PRINT O$;"":""
700 NEXT L: PRINT "";
720 NEXT K
740 P=PEEK(G+1):T=P-19*P/19
760 FOR K=1 TO T:PRINT "+";: NEXT K:PRINT "+";
780 FOR K=T+2 TO 19: PRINT "+";: NEXT K:PRINT "+";
800 GOTO 100
1000 R=R+1: POKE Q+R,P: RETURN
2000 F=F+1: P=-1: IF F<=R THEN P=PEEK(Q+F): RETURN
3000 K=0
3100 T=P+1: IF T/19#P/19 THEN 3200
3150 S=1: GOSUB 4000
3200 T=P-19: IF T<0 THEN 3300
3250 S=2: GOSUB 4000
3300 T=P-1: IF T/19#P/19 THEN 3400
3325 IF T<0 THEN 3400
3350 S=3: GOSUB 4000
3400 T=P+18: IF T>209 THEN 3500
3450 S=4: GOSUB 4000
3500 IF K=0 THEN 3600: P=-1: RETURN
3600 K=1+RND(K):C(K)=T
3610 IF PEEK(G+T)<>0 THEN M=1
3620 IF M=0 THEN B(K)=B(K)+16*(PEEK(G+P))
3630 POKE G+P,PEEK(G+P)+A(K)
3640 POKE G+T,PEEK(G+T)+B(K)
3650 P=T: RETURN
4000 IF PEEK(G+T)=0 THEN 4300
4050 IF M=0 THEN RETURN
4100 IF PEEK(G+P)+16*PEEK(G+T)+B(K) THEN RETURN
4300 K=K+1: C(K)=T: A(K)=EIS
4400 S=S+2-4*(S+1)/4: B(K)=EIS
4500 RETURN

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Converting North Star’s Deletion Characters

I own a North Star floppy disk operating system and have patched in my own IO routines. I found that attempting to correct a single error by using the DEL (or RUB OUT) key doesn’t work. Or if I try to cancel a complete line with the ESC key, nothing happens. The problem is that North Star’s disk operating system uses the BASIC commands of the at symbol “@” for canceling a line and the back arrow (or underline) for correcting a single character. All my other programs, monitors, assemblers and so on use the ESC key to cancel a line and the DEL (RUB OUT) key for deleting the previously typed character.

The solution is fairly simple and is shown in listing 1. Since I had to write a set of IO routines anyway, I incorporated a section to look for ESC and DEL input. When either is found, the byte is changed to the corresponding value needed by the operating system. The extra 16 bytes will readily fit into the space allocated to the user.

Of course, the original correction characters, at sign and arrow, can still be used.

Listing 1: 8080 assembly language listing of the changes to the North Star disk operating system to allow usage of DEL and ESC key codes for deleting characters and lines.

Circle 4 on inquiry card.
A Simpler Digital Cassette Tape Interface

To our department at Ohio University, "Saturation Recording's Not All That Hard" by David M Allen, page 34, January 1977 BYTE, was a sleeper until we happened to visit Abex Corporation here in Athens OH. While we were there, Dave Weeks showed us a direct digital interface which he was building from an old cassette deck. Bernie Hutchins in the Electronotes Applications Note No 32, March 25 1977, published a short item on the 555 used as a window comparator. Putting the two ideas together results in the interface of figure 1, where the 555 performs the function of upper and lower limit comparators with adjustable threshold along with a flip flop to recover the serial data stream. It even supplies an extra open collector output to drive a read indicator LED.

A cassette deck by Western Auto was obtained at the local surplus store for $10 and was modified by removing all the original audio electronics, but saving the wire motor control and power on and off switching features. An evening of bench tests indicated that the head would provide a 10 to 20 mV peak to peak output on direct saturation. Installation of a single Darlington transistor (SE4022) provided 40 db gain to bring the read level up to a volt or so, which fires the 555 comparators by pulling down the 555 control point threshold with an adjustable resistor to ground. That is about all there is to the unit except for a 4049 buffer inverter driver.

In our department, Larry Eichman fabricated a neat packaging of the system for a senior lab project. The recorder works fairly well over the range of 100 to 1200 bps. At 2400 bps, though, the tape recorder drive is somewhat erratic because of the motor speed drive mechanical on and off control. Some users of similar older tape machines have modified the drive motor by bending the regulator spring such that power is always applied to the motor with a regulated power source, rather than depend on the centrifugal rotating regulator mechanism. The same kind of machine has been used on a homebrew 808 system, and Larry Eichman has used it with a COSMAC 1802 processor. Photos 1 and 2 illustrate the front panel controls and IO indicators, as well as the circuit board wiring for the electronics.

The older style rotary switching deck is not suited to more complex software start and stop controls, but it does provide a quick serial data IO system for those who are willing to cannibalize an existing audio cassette recorder.

Ralph W Burhans
Ohio University
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Photo 1: The author's tape recorder as modified for direct digital recording. IO switch is at bottom left; LEDs are at bottom right.

Photo 2: Interior view of digital cassette unit showing additional circuitry on perforated circuit board.
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**Figure 1: Circuitry to modify a standard cassette recorder for direct digital recording.**

During the write process a DC current of approximately 1 V is passed through the record head, which saturates the tape. The polarity of the saturation recorded signal depends on the polarity of the DC current going through the head winding. During the read cycle, a voltage is induced in the head winding only when a transition between two oppositely polarized zones moves past the head. The 555 circuit (IC1) is used as a combination level detector and flip flop to recover the serial data.

**Table:**

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<th>IC Number</th>
<th>Type</th>
<th>+5 V</th>
<th>Ground</th>
</tr>
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<tr>
<td>IC1</td>
<td>555</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>IC2</td>
<td>4049</td>
<td>8</td>
<td>1</td>
</tr>
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</table>

**IC**

Number Type +5 V Ground
IC1 555 8 1
IC2 4049 8 1

**Circle 2 on inquiry card.**
Souping Up Your SwTPC 6800

One of the design economies in the SwTPC 6800 is the use of the same clock to set data transfer rate and to control processing speed. It avoids the need to build a separate processor clock and reduces the processing speed by only 10 percent. For most applications, this speed loss is unimportant, but it can become important if you are interested in heavily processor based activities such as process control or robotics. It is also inconvenient if you use timing loops frequently, since it is more difficult to calculate timing loops which are based on a slightly more than 1 µs period rather than on an even 1.0 µs period for the processor states. Therefore, I decided a little "souping up" was in order.

The 10 Percent Solution

The processing speed of the SwTPC 6800 is governed by the data rate generator clock, which is based on a 1.7971 MHz crystal timebase. A 7474 flip flop is used to divide the data rate generator timebase down to provide the processor clock with its 1.11 µs clock period. By replacing this 7474 with a socket into which you can plug a 2 MHz crystal oscillator, you can provide the desired 1 MHz signal source. This oscillator can be built cheaply and simply on a small piece of perforated circuit board (see photos 1a and 1b). It provides a separate source for the processor clock without interfering with the data rate generator or the action of the 7474.

Memories used with a 1 MHz processor must have access times of no more than 500 ns. This means that, although all factory supplied memories should run at the increased processor speed with no difficulty, other memories may not. For example, 2102-2s will not work reliably at the higher speed. To simplify confirming that your memories are fast enough, I've included a table of access times for the more commonly available types of 2102 memories (see table 1).

One advantage of making this improvement in your system is that you are no longer limited to one unchangeable clock speed. If you want to use the 1.5 MHz or 2.0 MHz versions of the 6800 processor, ACIA (Asynchronous Communications...
Figure 1: Simple custom circuit that modifies the SwTPC 6800 computer so the user can change the processor clock speed by plugging in different crystal oscillators. The entire circuit can be mounted on a small perforated circuit board (see photos 1 and 2) which plugs directly into the SwTPC 6800 board in place of the existing 7474 data rate generator timebase divider.

Table 1: Some commonly used memory integrated circuits (ICs) and their compatibility with a 1 MHz processor speed.

<table>
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<tr>
<th>Memory Number</th>
<th>Access Time</th>
<th>Usable at 1 MHz?</th>
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<tr>
<td>2102</td>
<td>1000 ns</td>
<td>No</td>
</tr>
<tr>
<td>2102-1</td>
<td>500 ns</td>
<td>Yes</td>
</tr>
<tr>
<td>2102-2</td>
<td>650 ns</td>
<td>No</td>
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<tr>
<td>2102A</td>
<td>350 ns</td>
<td>Yes</td>
</tr>
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<td>2102A-2</td>
<td>250 ns</td>
<td>Yes</td>
</tr>
<tr>
<td>2102A-4</td>
<td>450 ns</td>
<td>Yes</td>
</tr>
<tr>
<td>2102A-6</td>
<td>650 ns</td>
<td>No</td>
</tr>
<tr>
<td>2102AL</td>
<td>350 ns</td>
<td>Yes</td>
</tr>
<tr>
<td>2102AL-2</td>
<td>250 ns</td>
<td>Yes</td>
</tr>
<tr>
<td>2102AL-4</td>
<td>450 ns</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Figure 2: Simple test rig to verify that the oscillator circuit (shown in figure 1) is working. Both LEDs should light up when connected to pin 5 of IC2.

Building the Oscillator Card

The schematic shown in figure 1 indicates how the oscillator card works. This is one of the most common circuits of its type and was chosen for its simplicity. The parts as shown in photo 1a are mounted on top of the board and the connector (a 14-pin DIP [dual in line package] header) mounts underneath with its upper pins sticking through the top of the board. The reverse of the board is seen in photo 1b.
All the components of the oscillator fit nicely on a 2 3/8 inch by 1 1/2 inch (6 cm by 4 cm) piece of perforated circuit board, but the components must be carefully placed to avoid conflict with the components on the processor board to which it is attached. One satisfactory arrangement is shown in photos 1a and 1b. The wiring arrangement on the card is not critical so long as the wires are correctly connected to the connector pins. Capacitance values also are not critical. Any value from 0.001 µF to 0.1 µF will probably work. The entire board then plugs into the SwTPC 6800 board in place of the existing 7474 (see photo 2 for a side view of the DIP plug).

This is largely a foolproof card and should work as soon as it is assembled, but testing can do no harm and provides additional certainty that all is well. A simple test rig using two resistors and two LEDs, such as the one shown in figure 2, lets you verify that the oscillator is oscillating.

Conclusion

The increased processor speed which results from this modification offers benefits in any heavily processor based application. The circuit shown on the card is also convenient as a 1 MHz source for any other development work you may be doing. As an inexpensive way to solve processor speed problems, it's hard to beat.
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Continued from page 6

it had only the usual audio tape cassette interface for mass storage, and television for display purposes. (I have since ordered and received a floppy disk drive, which was plugged in and working within five minutes of setup.)

The immediate spur to writing this practical program was the need to analyze the editorial preferences section of the BYTE 1978 reader survey. This section, like the monthly BOMB analysis of articles in BYTE, gave a number of entries for which the respondent to the survey indicated a preference on a scale of 0 to 10. In the case of the survey, my goal was to find out what readers were interested in, so there was a list of 38 categories of interest to be rated 0 to 10. Each respondent's individual scale differs, but the idea here is to average the ratings of a large number of individuals and thus approximate an overall preference ranking. In the case of the survey, 2457 people responded out of 5000 subscribers picked at random from our mailing list.

In our monthly BOMB analysis, the ratings are acquired by the time-honored method of tallying with strokes on paper in groups of five strokes. Thus when Wai Chiu Li takes a monthly break from his normal job of "final paste" preparation for BYTE in order to tally the BOMB cards on a large sheet of paper, he accumulates strokes, thus:


In the survey analysis, with 2457 forms returned, our data processing contractor, Systemetrics, performed the keystroking of data and produced a report giving a count for each rating 0 to 10 in the 38 different categories of the preference survey.

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But this raw data is not the desired result. For the monthly BOMB analysis and for the survey analysis, I need a program which produces the following derived data from the input of ten counts (I exclude the 0 rating case) in n categories:

- Weighted sum total rating for each category.
- Mean and standard deviation over the field of ratings.
- Sorted rankings of each category by weight.
- Deviations for each category in units of one standard deviation.

The previous method of analyzing these results was to use a Commodore PR-100 programmable calculator, which has a mean and standard deviation calculation built into it. But this suffered from a number of awkward disadvantages. The procedure was essentially manual, with minimal automation through the use of the programmability of the calculator. The calculator has no way to enter enough data for the whole analysis, or to edit that data if a mistake is made, or to verify that data by examining details. Use of a calculator required an "expert" who knew the process, in order to accomplish the goal: calculation of mean, standard deviation, sorting of the categories by weight, and calculation of relative deviation from the mean for each category. With only 10 to 15 items I had put up with this procedure for a long time, but the prospect of 38 items and no way to verify the detail entries was not encouraging.

Thus I proceeded to create a program. Since the Apple II was the computer available to me in my office, I wrote the program using the Applesoft BASIC interpreter (Microsoft's product in Apple II clothing) as the high level language. It took me all of about five hours on July 11 1978 to go from the intention to a working BASIC program. If I had had the floppy disk accessory at the time, the result would have been even quicker since I would not have had to put up with the relative inconvenience of the audio tape mass storage system. Since this program was the first extensive one I have written in the Microsoft dialect of BASIC, I had to read the manuals as part of that process of creating the program. (Apple II's Applesoft interpreter is essentially identical to the Radio Shack Level II interpreter, the Commodore PET interpreter, and interpreters available for OSI and MITS Altair machines. All were written by Bill Gates and his associates at Microsoft Inc.) As many readers no doubt know, the language
was more than adequate to the task. Pascal it is not, but any high level language is better than no high level language.

So, with all the preparation carried out, and a program verified, I was able to analyze the 38 categories of preferences included in our survey, and proceed to begin analyzing BOMB results the same way.

Let's take a look first at what readers of BYTE found of interest based on our survey. The task presented to our survey participants was the following:

The following list contains a selection of topics drawn from computer science, mathematics, science and engineering. Please give your personal rating from 0 (no interest) to 10 (high interest). If a particular field within this list is your professional or occupational specialty, please record a check mark in the "Primary Interest" column to the left of the line. If you have already used a personally owned system for at least one nontrivial application in the field, please record a check mark in the "Have Implemented" column for that line.

The complete list of 38 topics is presented in table 1, ranked according to weighted total count, along with the actual weighted total counts and a fraction representing the number of standard deviations away from the mean of 38 categories. The mean weighted count total of the 38 categories was 8579.5, and the standard deviation calculated was 1977.9.

The top ranked category was rather nebulous: "applications to everyday life." Thus its 2.2 standard deviation rank may be less than significant. If the survey had asked for a ranking of "motherhood and apple pie" the result might have come out the same. I tend to think that the whole motivation for having a personal computer is to use it in everyday life, and it is always a great ego trip to have such an appraisal measure out at the top. Household automation with computers is one way to accomplish such a task, and is also a fitting subject for the experimenter. Personal data base design is a natural, ranging from the oft mentioned kitchen recipe file to the record collector's inventory to the maintenance of tax records. The latter of course overlaps on the application of personal computers to personal business.

In the experimenter's corner, there is a high interest in voice recognition by computers. But no pattern matching and recognition of sounds is possible without heavy emphasis on the art of programming, a topic which turned up as the sixth ranked item.

modem / 'mo • dem / [modulator + demodulator] n - s : a device for transmission of digital information via an analog channel such as a telephone circuit.
Once the "compleat" home computer experimenter has mastered the voice recognition and programming arts, what more natural test application than some of the neat logical games ranging from computer chess and the game of Go, on downward in complexity.

In the top ten, the last three items are perhaps a trio of related interests (which also are related to the other members of the top 10 set). Voice synthesis by computers complements voice recognition, yet is an easier task than voice recognition and perhaps less of a challenge as a result. The art of hardware design is required in any event for work in the more action oriented real time applications of computers such as voice experiments, household automation and control of mechanisms.

And of course, the general interest in robotics enters into the top 10 category in the form of computer control of mechanisms. Most of the challenging but little understood topics enter into the picture in the second ranked ten categories of the survey. Here we find graphics topics, the first entry of artificial intelligence topics into the ranking, etc.

A surprise (in view of this issue's chess theme) was the slightly negative rating of chess relative to the mean. The bottom ranked item (related to chess) is the artificial intelligence category of theorem proving. Also included in the bottom ten interest areas were other topics related to abstract artificial intelligence. What is surprising, though, is the fact that for people to be practically interested in robots, this relatively abstract theory of knowledge and its representation is absolutely essential. Perhaps we have here the indication of a need for some good tutorial articles about these quite essential fields—to say nothing of some practical demonstrations of concepts which can be exercised by the personal computer user.

In summary, the program worked out just fine for measuring the data of the survey. Although not covered in any great detail at this point, the BOMB analysis figures beginning in the September 1978 BYTE were created using this program. And now that I've completed the editorial and the floppy disk is working, I'll think of some other tasks for my intellectual servant to do.
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Bit Pad is the low-cost digitizer for small computer systems. Better than a joystick or keyboard for entering graphic information, it converts any point on a page, any distance into its digital equivalents. It's also a menu for data entry. You assign a value or an instruction to any location on the pad. At the touch of a stylus, it's entered into your system.

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South African Computer Club

We have heard from the Transvaal Amateur Computer Club, a South African club founded in June 1977. They currently have 120 members and publish a monthly newsletter called Tac2 which they would be pleased to exchange for newsletters from clubs based in the US. The club project is the design of a M6800 microcomputer that can be manufactured locally. This club meets every first Wednesday at 8 PM, Senate House, Witwatersrand University, Johannesburg SOUTH AFRICA.

Help Wanted

A group of computer enthusiasts from Singapore need some assistance in starting a computer club in that area. They are requesting advice from existing clubs about how to get a club started and would like suggestions about a meeting format. Additionally, they would welcome technical information in the form of manuals, brochures and catalogs from manufacturers. Write to Steven Goh, 3 Bristol Rd, Singapore 8, SINGAPORE.

Washington Area KIM Enthusiasts

Formed in January 1978, the Washington Area KIM Enthusiasts meet monthly at the McGraw-Hill Continuing Education Center in Washington DC. Meetings are scheduled for the third Wednesday of every month to discuss items of interest to KIM owners and users. To receive a copy of the current WAKE newsletter, send a stamped, self-addressed envelope to WAKE, c/o Ted Beach, 5112 Williamsburg Blvd, Arlington VA 22207, (703) 538-2303.

Attention: Xitan/TDL Owners

A user's group for owners of Xitan/TDL hardware and software has recently been formed. A bimonthly newsletter is available on a $5 annual subscription basis, and its contents include application programs, hardware and software modifications, classified ads, technical articles and software exchange. For further information, write to Xitan User Group, c/o Bill Machrone, 121 N Av, Fanwood NJ 07023.

The New York Amateur Computer Club

The New York Amateur Computer Club meets on the second Thursday of every month at Bernard Baruch College, 17 Lexington Av (corner 23rd St), New York, room 903 at 7 PM. For further information, write The New York Amateur Computer Club, POB 106, Church St Station, New York NY 10007.
Digital Group User's Organization in Chicago

A Digital Group user's organization was formed in the Chicago area in February of this year to provide a forum for the exchange of ideas, software, fixes, etc. by owners of Digital Group computer systems. They meet on the last Tuesday of the month in the meeting room of Consumer Systems, 2101 Swift Rd., Oak Brook IL at 7:30 PM. Membership dues are $5 annually which includes a newsletter. The newsletter is currently running about four to six pages and contains news of activities of club members, announcements of Digital Group computer hardware and software, articles and reviews by members of the club. Prospective members may write to The Digital Group Group of Chicago, c/o W L Colsher, 4328 Nutmeg Ln, Apt 111, Lisle IL 60532.

TCH IMP-16 Users Group

TIPS is a fairly new publication which follows the TCH IMP-16 system. To date, this newsletter has informed its readers of the status of the system including what is available and from whom, where parts of interest are available, basic knowledge about building the system and additional hardware details. Frederick Holmes, editor of TIPS, has also mentioned that the upcoming issues of the newsletter will be expanded to support SC/MIP based systems. Subscriptions to TIPS numbers 5 thru 14 are available for $1.00 and three SASE; back issues are $.50 and 1 SASE for each issue desired. Write to Fred Holmes, 101 Brookhead CT, Mauldin SC 29662.

Utah Computer Association

The µco is a monthly publication of the Utah Computer Association, an association dedicated to hobbyist interaction and public education about minicomputers and microcomputers. The club meets the second Thursday of each month at 7 PM in room 131, Murray High School, Salt Lake City UT. The membership fee is $5. For more information about this club, call (801) 278-1907.
October 5, Minicomputer and Microcomputer Seminar, Bluefield State College, Bluefield WV. This 1 day seminar and exhibition will feature business and engineering applications of minicomputers and microcomputers. The seminar will be conducted in the morning and afternoon and exhibits in the afternoon and evening. Contact Dr. Alvin Hall, director of continuing education, Bluefield State College, Bluefield WV 24701, (304) 325-7102.

October 5-8, Midwest Personal Computing Show, Apparel Center's Exposition Center, Chicago IL. More than 200 displays featuring the full spectrum of the latest personal computing developments are expected to be presented by manufacturers and distributors. The comprehensive program includes seminars, forums and practical application classes. Contact Midwest Personal Computing Exposition, ISCM, 222 W Adams St, Chicago IL 60606, (312) 263-4866.

October 9-13, Microcomputer Workshop, Carnegie-Mellon University, Pittsburgh PA. This intensive 5 day course is for individuals interested in applying microprocessor systems to a practical problem. Theory as well as practical experience will be emphasized in order to learn the capabilities and limitations of microcomputers and what it takes to apply them on the job. Contact Gerry Cohen, Post College Professional Education, Carnegie Institute of Technology, Carnegie-Mellon University, Schenley Park, Pittsburgh PA 15213, (412) 578-2207.

October 25-27, International Computer Retailers Conference, Chicago IL. The main purpose of this conference is to provide existing and future computer dealers with an in-depth look at the opportunities and pitfalls for developing sales and profits in computer retailing. For more information contact registration manager, Management Research Associates, 60 East 42nd St, New York NY 10017, (212) 687-2560.

October 27-29, BizComp '78, Marriott Motor Hotel, Atlanta GA. BizComp '78 will highlight the small budget necessary for the independent business operator to be able to purchase an in-house computer system. All facets of the small business computer industry will be on display from the latest innovations in computers to business software and word processing, supplies and services. Contact Felsburg Associates Inc, 12203 Raritan Ln, POB 735, Bowie MD 20715, (301) 262-0305.

October 31-November 3, Tulsa Computer Conference, Skipline Sheraton East, Tulsa OK. Contact Tulsa Chapter Association for Systems Management, 4110 S 100 East Av, Suite 128, Tulsa OK 74145.

November 3-5, Third West Coast Computer Fair, Los Angeles Convention Center. This is a conference and exposition on personal computers for home, business and industry. For more details about this computer fair, write for a free copy of the Silicon Gulch Gazette. Contact Computer Fair, POB 1579, Palo Alto CA 94302, (415) 851-7075.

November 5-8, Computer Applications in Medical Care, Washington DC. This IEEE sponsored symposium on computer applications in medical care is designed to inform physicians and health care professionals about current and potential applications of computer technology to patient care; and to identify areas of future research and development that need to be addressed. Contact Abund O Wist, PhD, general chairman, Medical College of Virginia, (804) 770-4957.

November 6-8, Asilomar Conference on Circuits, Systems and Computers, Asilomar Hotel and Conference Grounds, Pacific Grove CA. This conference, sponsored by the IEEE Computer Society, will delve into areas such as circuit theory and design, communication and control systems, computer systems, computer aided design, etc. Contact Donald E Kirk, Electrical Engineering Dept, Naval Postgraduate School, Monterey CA 93940.

November 13-16, COMPSAC, The Palmer House, Chicago IL. The IEEE Computer Society's second international computer software and application conference. This conference will bring together computer practitioners, users and researchers to share their ideas, experiences and requirements for applications software, management techniques, and software development support, including automated techniques. Contact Wallace A Depp, executive director, Processor and Computer Software System Division, Bell Laboratories, Naperville IL 60540, (312) 690-2111.
November 19-22, The 11th Annual Microprogramming Workshop, Asilomar Conference Ground, Pacific Grove CA. This workshop will provide a forum for the discussion and comparison of design techniques for firmware and for the supporting hardware. Informal interaction between groups working in similar research and application environments will highlight the topical session. For more information contact Dr Alice G Parker, Micro-11 program chairman, Dept Electrical Engineering, Carnegie-Mellon University, Pittsburgh PA 15213, (412) 578-2472.

November 27-December 1, Micro Programming Workshop, Lafayette IN. This 5 day hands-on advanced programming workshop is for individuals interested in developing skills required to plan, prepare, test and document 6800/6801 microprocessor applications software. Contact Jerilyn Williams, Wintek Corp, 902 N 9th St, Lafayette IN 47904.

November 28-30, 9th Annual Canadian Computer Show, International Centre, Toronto CANADA. Products displayed at this show will include: computer and data processing equipment, supplies and services, including minicomputers, peripheral hardware and software, keypunch services, consulting and contract programming and timesharing. Contact Industrial Trade Shows of Canada, 36 Butterick Rd, Toronto Ontario M8W 328, (416) 252-7791.

December 3-5, Ninth North American Computer Chess Championship, Sheraton Park Hotel, Washington DC. The 1978 annual meeting of the Association for Computing Machinery will be the site of this chess championship. This will be a 4 round Swiss style tournament with participants restricted to computers. Two rounds will be played on December 3 (1 PM and 7:30 PM), one on Monday (7:30 PM) and the last round on Tuesday (7:30 PM). Deadline for entries is October 20. Contact Prof M M Newborn, School of Computer Science, McGill University, Montreal Quebec H3A 2K6 CANADA.

December 12-14, Midcon/78, Dallas Convention Center, high technology electronics show and convention. Contact Electronic Conventions Inc, El Segundo CA, (800) 421-6816 (toll free).

December 13, Computer Networking Symposium, Sponsored by the IEEE Computer Society’s Technical Committee on Computer Communications and the Institute for Computer Sciences and Technology of the National Bureau of Standards. This symposium will highlight papers of practical and research experiences concerning both computer and communication networks. Contact Dr George Cowan, Computer Sciences Corp, 6565 Arlington Blvd, Falls Church VA 22046.

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Cartoon by K N Lodding
A TALL ORDER, BUT IN PRINCIPLE DOABLE...

I am an experimental psychologist and have purchased a Radio Shack TRS-80 microprocessor for research purposes. I've run into some of the following problems. First and foremost I am having difficulties in setting up the following as an experiment. I would like to present either a letter, word or object on the screen for 100 ms or more. This is an easy thing to do in Radio Shack BASIC. The observer's task is to respond as quickly as possible by pushing one of two keys (either a 1 or 0) based on what was presented. I am having trouble computing the reaction time, the interval of time lapsing between stimulus presentation and the response. The program should be able to measure the reaction time in ms and record which response was made. Could you offer some assistance on developing such a program?

My second problem is how to convert my TRS-80 so that I can use a television instead of the Radio Shack video screen. This would allow the use of an S-100 bus and the Cromemco Dazzler for color video.

A third problem I've run into is the following: research-wise I am into workload measurement or dual task analysis. Using a normal television I've hooked up a pong game. I would like to present simultaneously by means of the TRS-80 a list of words for the observer to memorize and recall while the pong game is on. How can one go about doing this?

Fourth, I believe the cassette transfer program for the TRS-80 is limited in that I must transfer all the information on the tape into memory. Is there no way to run a search and only transfer part of the information on the cassette tape into memory?

Finally, I am interested in determining why one needs to buy the Radio Shack interfaces for memory expansion purposes. Why can't one buy an S-100 bus and mother board and additional static memory and accomplish the same thing at a lower cost?

If one of your readers can help me with these matters, please let me know.

Asst Prof Joseph Dalezman
New College of USF
Division of Natural Sciences
5700 Tamiami Tr
Sarasota FL 33580

TIMELY COMMENTS ON KIM

I just tried Robert Baker's KIMER (KIMER: A KIM-1 Timer, July 1978 BYTE, page 12). The clock operated but the calibration was not wide enough for my crystal.

Since the BIT instruction (line 0220) is used to test the timer status, the timer is not being used in the interrupt mode even though memory location 170F was loaded. The status of PB7 in this case has nothing to do with the timing. The major time delay is determined by the JSR SCANDS command which takes several milliseconds to perform. The timer status is tested on each return from SCANDS and so will always be some multiple of this time delay. The 1 ms calibration resolution cannot be obtained.

Here are a few ways the program could be fixed:
- The clock could be written as an interrupt routine. SCANDS would then be interrupted at any point in the subroutine.
- The number of JSR SCANDS commands could be counted in a loop which would be exited before the timer times out.
- The calibration could be reduced to 0F or 0E and a longer fine adjustment used.

There have been several programs in the KIM-1 User Notes which illustrate the use of the timer. My version of a clock using the interrupt mode was printed in the March 1977 User Notes and also in The First Book of KIM. When using the program in the latter publication, go by the detailed listing since line 036A is incorrectly printed in the HEX DUMP.

I hope this is of help.

Charles H Parsons
80 Longview Rd
Monroe CT 06468

A SwTPC 6800 FIX

Here is a problem with the SwTPC 6800 and a fix that I haven't seen published before:

You can't reset the 6800 from a wait-for-interrupt state!

On the SwTPC MP-A board, the reset signal is transmitted to the MCM6800 chip via a DM8098 hexadecimal inverting three state buffer that is disabled when the processor enters a hold condition, as occurs after the execution of a WAI (3E hexadecimal) instruction. Once the 6800 is in the wait state, the reset signal generated by pushing the front panel reset button is stopped at the 8098 and never gets to the 6800 chip.

A hardware fix is to break the traces to pins 2 and 3 of the 8098 (labeled IC15 on the SwTPC schematic and parts layout) and reroute the signal through a new, permanently enabled 8098.
permits the reset signal to reach the 6800 and you can then recall your 6800 after performing a WA.

Perhaps some comment is in order.

First, I certainly do not wish to characterize a distributed communications network as anything less than highly complex. However, I do believe that in principle these complexities can be managed with a combination of sophisticated software and straightforward hardware. What makes the problem difficult is that it is not isolated in the same way that the development of a language processor or operating system can be isolated. The first step in the creation of complicated software interfacing to a myriad of systems is to have communication in general. In that spirit I welcome Mr. Newcomb's comments.

A second large point is made by Mr. Newcomb that the network structure I have discussed is workable, but I do know that it can never work without a beginning. I am slowly working toward such a beginning, and I hope that others will as well.

Jeff Steinwedel
715 Reseda Dr, Apt 2
Sunnyvale CA 94087

PERSONAL COMPUTERS REQUIRE INSURANCE, TOO...

In shopping around for insurance on my house (renewal due in August), I discovered that none of three large insurance firms in this area would cover—specifically—a personal computer of any significant value. None of the three would add any rider or offer any separate insurance coverage. The general consensus was that personal computers were considered no more than "hi-fi" equipment.

The specific area of insurance on a personal computer does not affect me yet since I am just starting to collect the components for a fairly large system. Medium to large microcomputer systems can run from $3 K to $8 K, the price of a new or nearly new auto.

Auto insurance is commonplace and there is a good reason for it. Only part of such insurance is devoted to the auto itself. Home insurance covers only parts of personal property within a dwelling and is generally covered as half the amount of the dwelling itself. With the increase in overall prices, replacement of personal property will probably not cover a system of $3 K or greater. This is especially true in a household having expensive relatives such as children.

Perhaps some reader might comment on insurance for such expensive devices?

Leonard H. Anderson
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REGIONAL BASIC CONTEST NOTES

Thank you for the nice article in the July 1978 issue of BYTE about the regional BASIC contest. I would like to make a couple corrections. First, Scott Parker is really Scott Porter, and the second man was Newton B White Jr of St Louis MO. Mark Grundler, the advisor, was unable to make the trip.

If the truth must be known, it was Newton, and not Porter, who led the team. He spent the weekend teaching BASIC to Scott, a situation which was a major handicap to the team's effort. I am happy to report that next year Grinnell will be able to field a team of four BASIC programmers.

White and Porter were members of Grinnell's FORTRAN team, which took second in this year's Midwest Regional FORTRAN contest and competed in the national FORTRAN contest. The other two members of the team were Bruce Albrecht and Steve McKelvey. Both Albrecht and McKelvey had strong per­manences to help the Grinnell team to a second place in its first outing. An interesting side note: at the FORTRAN regional, Porter taught White how to program in batch FORTRAN. Porter was a batch FORTRAN programmer and White was an interactive BASIC (redundant, but anything for a parallel construction) programmer, and both had the faults of each style. This last summer White was working in some batch environments and, likewise, Porter is working mostly with interactive BASIC.

Since Grinnell is a liberal arts college without an applied math or computer science major, it was necessary to go looking among the other majors for programmers. The makeup of the team was a math/philosophy double major, a physics major, and a chemistry/math major. The blend of that group's problem solving ability was its major asset.

Scott Porter
Office of Computer Services
Grinnell College
Grinnell IA 50112

SOME ACES NEED ENGINEERING

After reading your magazine avidly for a couple of years we felt we could write to you and request the assistance of you and your readers. First a few words about our aims: the Awareness, Consciousness and Energy Studies Group (ACES Group) is devoted to the scientific study of the various manifestations and attributes of consciousness. Today the "consciousness explosion" is well under way and more and more people are practicing some sort of technique to bring about an expansion of their awareness. Success becomes apparent through the subjective experience of joy and well-being. However, our society has long been indoctrinated with the need to provide objective proofs of every experience. We reasoned, as other groups have done, that an increase in awareness or a change in one's state of consciousness should have some corresponding effect on the body's physiology and therefore be physically detectable.

Research during the last eight years shows that this is indeed the case. Stress is apparently the biggest hindrance to increased awareness. A reduction in stress shows itself in such ways as an increase in galvanic skin resistance (GSR), normalization of the blood pressure and increased alpha activity of the brain (to mention but a few). In order to study the effectiveness of different methods of reducing stress the ACES Group has developed its own equipment. Digital monitoring of EEG, GSR, heart rate and body temperature is possible.

The outputs from our present monitoring equipment are eight analogue voltages which we wish to sample at not less than 100 times per second. This information should then be passed to our microprocessors for storage and analysis. For this purpose we have purchased two processors, one being the Digital Group Z-80 and the other the OSI Challenger; both have VDUs, four digital tape drives and in excess of 20 K memory.

Our main problem is interfacing the analogue monitoring equipment to our processors. Perhaps some of your readers with experience in analogue to digital conversion could offer us some helpful suggestions. We welcome contact with anyone (professional or hobbyist) who has experience in biomedical monitoring systems and we are constantly on the lookout for methods of increasing the speed of computation. Another problem we have not yet resolved is that of designing a simple but accurate noninvasive method of monitoring blood pressure for use in a non lab environment. Ideas, anybody?

Thank you for a most informative and interesting journal.

Graham Else, Ian Wales
ACES Group
Koenigsberger Straße 10
6107 Reinheim/Odenwald 1
WEST GERMANY

9900 DOWN UNDER

Living as we do on the other side of the world from where it is all happening on the microcomputer scene, we depend very heavily upon what we can read in the pages of BYTE and the other magazines. We can hardly tell you with what avid interest each issue of BYTE is per­used (we get it shipped out to us airmail in order to get it as early as possible). Keep up the good work.

We ourselves use TMS-9900 based equipment, so every mention of this rare but wonderful beastie in your pages...
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evokes a heightened response of interest. I would like to get in touch with users of 9900-based systems in the States so we can exchange notes, ideas, etc.

B Ward Powers
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AUSTRALIA

A FEW NOTES FROM A CANADIAN READER

1. Items move faster through our mail system if you include the postal code. This is that funny series of letters and numbers that appear above, after the province. My postal code is V6S 1B2.

Note that the format is letter, number, letter, space, number, letter, number. Although this may not be quite as simple as your ZIP code, it does mean that a letter addressed:

Andrew Bates,
Canada V6S 1B2

will be delivered to me. The postal code pinpoints the side of the street in a residential block or even the floor of a building in a business district. How’s that for precision!

Software writers take note: we Canadians need at least six characters for the postal code and four characters for the province (state). And if you are going to check the ZIP for all numbers, please put the check in a subroutine so we can replace it with a suitable check for our postal code.

2. WATS lines do not cross international borders (at least that is what the telephone operator told me). This means that we people in Canada can’t phone you for free like everyone else in the United States can. How about letting your people accept collect phone calls from Canada, only so we can use A G Bell’s famous invention, instead of having to spend hours slugging away at the typewriter and then waiting for what is an erratic mail service on both sides of the border?

3. Another small request for software writers who are mailing things to Canada: if your package costs $75 and is distributed on North Star diskette, for instance, please mark the customs declaration as:

    DISKETTE $6
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If you mark the price as $75, we end up paying duty on the diskette as though it cost $75. Printed matter comes across the border duty free and there is no duty on an item of less than $10 value.

Andrew Bates
3261 W 18th Av
Vancouver BC
CANADA V6S 1B2

EROM CONFUSION: THE 2716

Elaborating on David Marke’s letter (July 1978 BYTE, page 11), it seems to me that Intel bears the blame for the 2716 single voltage versus 3 voltage supply EROM confusion.

Intel gave their new generation 16 K part an old generation number. They have essentially acknowledged the confusion by introducing the 2758, a 1 K EROM like the 2708, but single I suggest we use the Texas Instruments part number, 2516, when referring to either the TI part or the Intel 2716.

Al Anway
Poly Micro Systems Inc
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There are some things that retard communication between people having no contradictory interests, eg: vendor and customer. Vendor has something to sell. Customer finds something to purchase.

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Technical Description

Our Paperbyte™ bar code reader consists of three parts: (1) an old turntable set at 33 RPM on which sits the page to be read, attached to a 48 ounce juice can; (2) a read head with light source which is attached to a parallelogram assembly to allow the head to be moved up and down while remaining level; (3) an interface that brings the output of the phototransistor in the read head up to a 5 V digital level.

The Turntable and Juice Can

A juice can with one end removed supports the page while the turntable (a junked one obtained for free) rotates the page. For purposes of this contest we simply taped the page to the can. However, for everyday use some sort of clip-on system would be reasonable. Even four small magnets should work to hold the paper on the can. Centering the juice can on the turntable was no problem since the plastic record mat on the turntable platter has a series of raised concentric circles on it. On turntables lacking this feature it is an easy matter to draw a circle on a piece of cardboard placed on the turntable to indicate the proper position. In use, we found that the can did not tend to wander as the turntable went around.

Photo 1: The authors’ bar code reader entry. The page of bar code is shown taped to a fruit juice can sitting on a phonograph turntable. The reading arm, shown at bottom left, features two small lamps and a focusing lens. Light reflected from the rotating bar code energizes a phototransistor at the other end of the reading arm. The signal is then translated into binary voltage levels and sent to the computer's input port.
Listing 1: Walter Banks’ “Blabberwacky.” The output was produced on a printer that does not respond to ASCII control characters, so the line feeds were printed as lower case ws.

The Read Head

The read head consists of a 2N5777 phototransistor, a lens and two penlight bulbs. These items were mounted on a block of wood. The lens we used was a 25 mm lens from an 8 mm movie projector, but any lens of similar focal length can be used because color rendition and edge focus are of no concern. The phototransistor was mounted on its side rather than vertically so that the lens effect of the TO92 package would tend to pick up more of one particular bar rather than picking up adjacent bars. It was also covered with black tape on all sides but the front, to exclude stray light.
The phototransistor was mounted peeking through some translucent tape which served as a focusing screen. The entire assembly was covered on the top and sides with a cardboard hood to exclude ambient light. The block of wood on which the read head was assembled was attached to two strips of wood, which were in turn attached to a base. This allows us to move the read head up and down while keeping it level.

The system was focused by moving the base plate back and forth. A pair of type 222 prefocused penlite bulbs were mounted on either side of the lens and angled toward the bar being read. These bulbs are rated at 2.25 V; when wired in series they ran fine from the +5 V used for the logic, and drew 250 mA. A strip of ordinary black tape was wrapped around each bulb to prevent stray light from reaching the lens.

The Interface

The interface consists of a 500 k trimpot and a 74C04 CMOS hex inverter, as shown in figure 2a. Since the input port on our computer accepts CMOS logic, no further buffering was required. In order to drive standard TTL logic, the remaining CMOS inverters can be used or a transistor and two resistors (see figure 2b). This interface owes its simplicity to the high gain of the 2N5777 and the very high input impedance of the CMOS chip.

Calibration and Use

The calibration and use of this system are simple. Once physically assembled, the read head is moved close to the page to be read and is adjusted to bring the page into focus on the screen. This requires some experimenting at first. The phototransistor is positioned about 3 inches behind the lens, which provides a magnification of about 2. To adjust the sensitivity, focus the head and then, with the turntable turned off, turn the platter until the read head faces plain white paper. Observe the voltage at the collector of the phototransistor at point A in figure 2a. With a lot of light from the white paper on the phototransistor, and the potentiometer set to its highest value, this point is pulled low by the transistor. The potentiometer is adjusted until it just pulls the line high and then it is backed off just enough to let the line go low. This completes the sensitivity adjustment. While spinning the turntable by hand, you can watch the output of the transistor alternate. In our case we had a voltage swing of about 4 V at point A.

In order to actually read the lines, the output of the CMOS interface is hooked to a single bit of an input port on the computer. The computer then waits for a line to start, times the light and the dark times, and decides if the bit is a one or a zero. The computer program itself is straightforward, if somewhat long-winded. The computer we used is an MCM/800 manufactured by Micro Computer Machines, Kingston, Ontario. The processor is a discrete bipolar affair that has
the same instruction set as the 8008, with a few enhancements.

Notes and Conclusions

Because this reader was produced and documented within a period of 48 hours, we did not have time to go through many revisions. From our experiences we gained a considerable amount of information that could be applied to the development of an improved reader.

When we set out to build the reader, we assumed that the mechanical portion would be easy and that most difficulties would be with the electronics. This was not the case. Although the entire electronic portion of our reader turned out to be extremely simple, (it cost under four dollars), it performed flawlessly. We have had no difficulties with it and we do not suggest any modifications. In one test performed while checking the reader, we read a single line 255 times without glitches.

The mechanical portions of the reader, however, could stand some improvements. Our most serious problem was keeping the read head focused on the page. The juice can was not perfectly round, particularly at the end with the top removed, and minor variations tended to put things out of focus at one end or the other of the line. The can had to be centered exactly on the turntable or similar problems would arise. Anyone seriously considering this approach might use a full unopened juice can, remove the turntable spindle and glue the can (after careful centering) to the turntable.

Probably the weakest link in the design is the head support mechanism, which we do not recommend. Given some sort of reasonably round support for the page, it would be nice to have the head permanently mounted on a slide arrangement so it could be focused once and then slid back and forth in front of the page being read. If you standardize on a fixed spacing for the lines, it would be possible to add a detent mechanism so that the head would stop only in the middle of lines. It would be reasonably easy to add some automatic method of advancing the head.

We feel we should also mention something that we discovered in the course of testing our reader. It applies to bar code readers of our type and to wands as well. As Keith Regli points out in his article “Software for Reading Bar Codes” (December 1976 BYTE, page 18), readers will tend to read light and dark areas of equal width as being somewhat different. Our reader was no exception, and in fact the amount of bias shifted from one part of the line to another as the focus changed a bit. This caused quite a bit of jitter in the light time to dark time ratios, which are, in theory, what is used to separate 1s from 0s. However, we also observed something that is of considerable use: while the light to dark ratio jittered a lot on our reader, the timing of a full bit (light time plus dark time) was very stable. This suggests an improved software decoding routine in which you can compare the total time (light plus dark) for the current bit with the total time of the previous bit. Since you know if the previous bit is a 1 or 0, you can determine what this next bit is by appropriate comparison. This automatically compensates for the jitter in the light to dark ratio introduced by the reader, and also allows tracking on wands where the time will tend to wander a lot.
The Data-Scan bar code scanner is designed for reading bar codes such as those presented in BYTE. The scanner can read degraded bar codes (such as Xeroxed patterns) as well as black bars on a gray background or gray bars on a white background without adjustments.

Functionally, the scanner specifications include: a scanning rate of 10 to 40 inches (25.4 to 101 cm) per second, power supply requirements of +12 V at 50 mA, and a transistor-transistor logic (TTL) compatible output in the form of a serial bit stream suitable for application to an input port.

The scanner consists of a light source, a phototransistor and the signal conditioning circuitry shown in figure 1. The light source, an infrared light emitting diode (LED), illuminates the surface of the paper through an aperture slightly smaller than the area of a unit width bar. Viewing this same surface area through the aperture is a phototransistor. The transmitted and reflected light either passes directly through the aperture or travels through a bifurcated fiber optic cable as described in my article, "Signal Processing for Optical Bar Code Scanning," December 1976 BYTE, page 77.

As reflected light impinges on the photo surface of the detector, a light induced current of several hundred nanoamperes flows into the collector. This minute current is amplified, converted to a voltage, and applied to one input of the voltage comparator. Simultaneously, the average of the peak to peak output voltage is applied to the reference input of the comparator. Those voltages in excess of the reference voltage (corresponding to the white areas between the bars) cause the output of the comparator...
to conduct, resulting in a logic zero at the interface input. Those voltages below the reference (corresponding to black bars) cause the comparator output to turn off, resulting in a logic one at the interface input. The process of using the average of the peak to peak voltage as the reference input to the comparator is known as adaptive thresholding.

As the line of bar coded data is scanned, a string of 1's and 0's is serially applied to the optics cable. These variations represent a interface input. Those voltages below the reference (corresponding to black bars) are turned on every time a bar is detected. Also available, as an option, is a beeper to signal the operator when a line of bar codes is scanned successfully.

I mentioned earlier that the transmitted and reflected light passes either through the aperture directly or first through a fiber optics cable. These variations represent a number of scanner models I have designed and developed for sale. For further information on the bar code scanner write to Micro-Scan Corp, POB 705, Natick MA 01760.
Figure 1: White to play. This example illustrates some of the basic problems of strategy and tactics that must be evaluated by any chess playing computer in a typical position. The computer (White) must evaluate a variety of possibilities: two good first moves for White include 1 R-B7 and 1 BxN ch. 1 R-B7 threatens BxB. Therefore Black must either exchange Bishops or gain time by the counterattack 1...B-K4. If 1...BxB, White must complete the exchange by playing 2 RxR or 2 BxN ch, and so on. The position is analyzed in detail in the game tree shown in figure 2.

A Computer Chess Tutorial

On February 20 1977, the Minnesota Open chess tournament was won by a computer program, Northwestern University’s Chess 4.5. This was a far better result than any program had previously achieved, considering that all the other entrants in the tournament were human beings. An improved version, Chess 4.6, went on to wrest the world computer chess championship from the Soviet program KAISSA (see “The Second World Computer Chess Championships” by Peter Jennings, January 1978 BYTE, page 108). Professional chess players are beginning to worry about the competition from machines. They would seem to have little to fear at the moment, however. The consensus is that Chess 4.5’s tactical skill is impressive but its strategy is weak.

Against such competition, what can a personal computer experimenter expect to accomplish? Perhaps a great deal. There have been few new ideas in computer chess since Claude Shannon (see references) outlined the basic principles in a paper published in 1950. (The superiority of Chess 4.6 is due primarily to faster hardware.) Experimenters can participate in the search for the conceptual breakthroughs that will be needed before computer programs can be a match for the best human players. With that thought in mind, this article deals with the questions: What is a good structure for a chess program? What are the major functions that it must perform? In what directions can we seek innovations?

The Game Tree

To get a notion of what a chess program must do, let’s look at a position from an actual game (see figure 1). First we must grasp the important features of the position. White has an extra pawn, a passed pawn far from Black’s King. Black’s mobility is very limited: neither the Knight nor the Rook can move. Black’s Bishop is attacking White’s Rook and, indirectly, the Bishop behind it. Of less importance, because of Black’s lack of mobility, is the fact that two of White’s pawns are unguarded. White’s task is to save...
his Rook and to profit from Black's lack of mobility. White should win if he can find satisfactory solutions to these problems.

Next we calculate variations — sequences of moves that we would visualize in an actual game before deciding on a move to play. We will follow a systematic procedure that will serve as a first approximation to a computer program. We construct a tree whose nodes represent positions and whose edges represent moves. The variations are the paths from the root to the leaves. Initially, the tree will consist of one node representing the given position. We expand the tree as follows:

Expansion — Choose a leaf that has not been marked as final. (If one cannot be found, the expansion phase is ended.) Either mark it as final or select a set of legal moves in the position represented by the node. To the leaf attach sons representing the positions reached by the moves. Repeat from the beginning.

This procedure might yield the tree shown in figure 2. The size of the tree has been limited somewhat for illustrative purposes. Some of the variations I considered and rejected are not included. Most programs generate much larger trees since it is hard to build into a program the chess knowledge needed for rigorous selection of moves. The length of paths in the tree is expressed in plies (half-moves). A move consists of a play by one player and a response by the other; a ply is a move by one player alone. Because the term move can be confusing (the chess literature speaks of looking three moves ahead for example, but are two or three moves by the opponent meant to be included?), in discussions of chess program-

In the expansion procedure, no rule was given for deciding whether to expand a node or for selecting the moves. To gain insight into the way human players make these choices, let us consider the variation that runs down the right side of the tree. In the initial position, Black threatens ... BxR. White can either make a counterthreat or move his Rook to guard the Bishop. Thus the possible moves include 1 BxN ch, 1 R-B7, and 1 R-R5. I rejected the last alternative because the Rook would have less mobility on R5 and it seemed unimportant to keep it on the fifth rank. 1 R-B7 threatens BxB and moving the Bishop to another diagonal allows B-K3, attacking Black's Rook. Therefore, Black must either exchange bishops or gain time by the counter-attack 1 ... B-K4. If 1 ... BxB, White must complete the exchange by playing 2 RxB or 2 BxN ch. The latter move was omitted because the reply 2 ... RxR leads to the position at node 13 (see figure 2), already seen to be unsatisfactory for White. After 2 RxB White threatens R-R6 followed by the exchange of all the pieces and the triumphant advance of the Queen's Rook pawn (QRP). Black must play 2 ... K-N1 or 2 ... K-R1. The square closer to the center was chosen on general principles.

Figure 2: A game tree developed from the position in figure 1. Each node represents a position; the root, the initial position. The move leading to the position is written in the top of the box, the evaluation of the position in the bottom. The number above the box identifies the node. A node's ply number is its distance from the root.
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Free of threats at last, White can move in pursuit of his goals. White could play 3 R-N7, preparing to position his Rook behind the passed pawn; 3 K-Q2, bringing his King toward the center; 3 P-R5, advancing the passed pawn; or 3 R-R6, to force the exchange of Rooks. Somewhat arbitrarily, I included in the tree only the two moves that seemed best. 3 R-R6 forces the Knight to move. Obviously it should approach the passed pawn, but it is not immediately clear which square is best. After 3 ... N-K2 4 R x R P x R the assessment is clear: having two passed pawns in a minor-piece ending, White should win easily. There is no need to consider other Knight moves, because the effect on the evaluation of the position would be too small to affect White's choice of move in the initial position.

From this brief discussion we can see some of the factors that determine the selection of moves. When there is a definite threat, it is necessary either to answer the threat directly or to make a counter-threat. Otherwise you must decide which goals are most important and choose the moves that best advance these goals. When two moves have similar effects, not much is learned by including both in the tree, particularly at a deep level.

We can also see some of the reasons for terminating a node (that is, choosing not to expand it). In this example, a node is terminated when the position can be evaluated sufficiently well or when the previous move was not forcing and the side to move has no forcing move that accomplishes anything. At node 14, for example, it is already clear that White doesn't have a won position, and it follows that one of his moves must have been a mistake. Thus we can evaluate the position sufficiently well (but not accurately: further analysis would lower the estimated evaluation given in the figure). At node 5 White has the forcing move 3 B-K3, but after 3 ... R-R1 his position hasn't improved. We consider these moves but don't add them to the tree, because the resulting position is merely compared with the position at node 5, not evaluated.

Once the tree is complete, the next step is to evaluate the terminal positions:

Evaluation — Label each leaf with the value of the position from the point of view of the player whose turn it is to move in the initial position. Positive values mean the player has the advantage; negative values mean the player's opponent does. A value of ±1 means an advantage...
barely enough to win; a value of ±2 means an easy win (see figure 2).

In the present example, material, mobility and pawn structure were the most important factors in making the evaluation. In a middle game position, King safety would also be taken into consideration.

The final step is a completely mechanical procedure called the minimax algorithm, which is guaranteed to choose the best move provided the evaluations are accurate and that the best move at each node is included in the tree.

Backup — Select an unevaluated node, all of whose sons have been evaluated. If the node is at even ply, label it with the maximum of the sons’ values; at odd ply, choose the minimum. Repeat from the beginning until all of the nodes have been evaluated. Then choose the move leading to the ply-1 node with the greatest value.

This method of assigning evaluations to non-terminal nodes is based on the assumption that each player always makes the best move. The minimax algorithm will not always choose the move that affords the best winning chances against a weak opponent.

Our 3 part procedure for generating a game tree is somewhat unnatural. For one thing, a person analyzing a position would return to the expansion phase if the moves originally selected didn’t work out as well as expected. Also, the evaluation phase reflects the human assessment process poorly. No provision is made for recording degree of confidence in the evaluation. Human players make relatively coarse absolute evaluations: they judge which of two similar positions is better, but do not attempt to assign slightly different values to them.

In chess programs, expansion, evaluation and backup are carried out simultaneously. One reason is that time can be saved by using backed-up values to demonstrate that some nodes need not be expanded at all. For example, the variation 1 BxN ch RxB 2 RxP ch gives White a great advantage; we see that 2 RxP ch refutes 1 ... RxB. Once one refutation is found, it is pointless to look for another: 2 R-B7 need not be considered if not considered already. What does this mean in terms of the minimax algorithm? Once node 3 has been assigned the value +1.4, we know that the value of the minimizing node 2 will not be any greater. Similarly, once node 7 has the value +2.4, we know that the value of the maximizing node 6 will not be any less. Therefore the minimax algorithm will not choose the value of node 6, and it
**Figure 3:** A routine to choose a move. A ply table (so called because it is indexed by the ply number, \(i\)) is used to choose moves. (A ply is a move on the part of one player; two plies equal one chess move.) The entries in the ply table correspond to nodes in the game tree (see figure 2). Each entry contains three fields: \(L(i)\), a pointer to the list of moves selected at each node; \(M(i)\), the move currently being processed; and \(E(i)\), the evaluation. Most of the subroutines are written as functions in order to show which data areas they use and affect. Only those data areas that play a central role are indicated. \(\infty\) refers to a number which is larger than any returned by subroutine \(\text{VALUE}\). Its additive inverse, \(-\infty\), is used as the initial value of \(E(0)\).

Programs that generate a large tree generally use a depth-first search and have an overall structure similar to that shown in figure 3. The inflexibility of the depth-first search is a significant disadvantage, though. For example, suppose that shallow analysis of the first ply-1 move casts doubt on its
value. Time might be saved by proceeding at once to the other moves and returning to the first move only if they seem no better. But in a depth-first search, the decision to terminate a variation cannot be changed on the basis of later information. Consequently, programs that generate small trees usually maintain the entire tree in programmable memory. Then it is possible to skip around in the tree, expanding those nodes that look most promising. Although such programs aren't structured like depth-first programs, they perform many of the same functions, and so the following discussion of the subroutines partially applies to them.

The BACKUP Routine

The movement of values up the tree is controlled by BACKUP, which also prunes refuted nodes. The procedure is shown in detail in Figure 4. The minimax part of the procedure manipulates the fields E(i), which can contain initial values, provisional values, and final values. The initial values are $-\infty$ for even ply and $+\infty$ for odd ply, where $\infty$ is a number larger than any returned by VALUE. E(i) is always set to the initial value when the table entry is not being used. The values produced by VALUE are final values. Whenever a final value E(i) appears in the ply table, BACKUP compares it with the value E(i-1). E(i) replaces E(i-1) if i is even and E(i-1) is greater than E(i) or if i is odd and E(i-1) is less than E(i). E(i-1) then contains a provisional value. A provisional value becomes final when the move list at its ply becomes empty. Whenever E(1) replaces E(0), M(0) is saved in M. As a result, M ultimately contains the first move in the list L(0) that produces a maximum final value in E(1).

The Alpha-Beta Algorithm

The elimination of refuted moves from the tree is accomplished by a procedure called the alpha-beta algorithm. The alpha-beta algorithm is discussed in Slagle and
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The LIST Routine

The decisions that determine the size and shape of the game tree are made by LIST. It has three main functions: termination of nodes, selection of moves and the sorting of the list of moves. If the program is to play under a time limit, LIST must also monitor the elapsed time and modify its decisions accordingly. Existing programs handle these functions in widely differing ways. Their selection and termination procedures range from trivial to complex. It's discouraging that the trivial methods have so far yielded the best results, for surely a sophisticated LIST routine will be needed for first-rate chess.

Most chess programs condition termination primarily on depth and the availability of certain types of forcing moves. The simplest method would be to terminate always at some fixed depth. Then VALUE would have to give special handling to positions with an exchange in progress, lest material be reckoned incorrectly. Consequently, many programs use two depth limits. Beyond the first limit are selected only certain forcing moves, typically checks and captures. Termination occurs, of course, when there are none. At the second depth limit termination always occurs.

Other criteria for termination have been tried. The Ostrich program (developed on a Data General Supernova minicomputer at McGill University in Montreal, Canada) terminates variations in which material is sacrificed and not recovered within three plies. Several people have suggested that termination should occur only if the position can be accurately evaluated. The
Newell-Shaw-Simon program used this philosophy. When the entire tree is maintained in programmable memory, termination decisions as such need not be made at all. For example, the program COKO expands those nodes that promise the greatest yield of information, no leaf being permanently excluded from consideration.

For selection and sorting, LIST might assign to each legal move a plausibility rating designed to indicate the probability that the move will prove best. Many programs don't explicitly assign a rating; nevertheless, it is convenient to imagine that their decisions are based on an implicit rating. Selection and sorting can then be done as follows: select all moves with ratings greater than some threshold. If too few moves are selected, add highest-rated moves to make up the minimum number. (The threshold and number of moves might depend on depth.) Sort the selected moves by rating.

For sorting, the requirements on the rating procedure are not stringent. It suffices that moves good enough to cause cutoffs often appear early in the list. Occasional inaccurate ratings will merely increase the processing time, not cause a blunder. The number of cutoffs can be markedly increased by simply assigning high ratings to a few easily defined categories of moves: captures, checks, moves by attacked pieces, etc. Another simple rating method is to assign a high rating to moves that have proven to be good in other parts of the tree. For example, the "killer" heuristic assigns to a refutation found at one node a high rating at its brother nodes. This heuristic works well in positions containing threats, because all moves that ignore the threat can be refuted by the same reply.

For selection, the plausibility rating must be more accurate. A best move markedly better than the second best move must only rarely receive a rating low enough to cause its rejection. Simple criteria that are adequate for sorting are bound to fail. The rating must be based on all of the move's important effects, which can in turn be determined only by elaborately tracing the relationships of the pieces. For this reason, programs that use selection generally maintain a tactical description of the position. In the program we are considering, it is the responsibility of the MOVE routine to keep such information current.

The VALUE Routine

The evaluation is usually computed as a sum of numerical scores, each representing one aspect of the position. Chess programmers tend to include only those aspects that...
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are easiest to program. Unfortunately they are not always the most important ones. The traditional chess literature is more explicit about evaluation than about selection and termination. The books in the bibliography are particularly helpful.

The evaluation of a position depends mainly on material, mobility and vulnerability. The calculation of material is straightforward, although experts disagree about the exact values of the men. Chess 4.6 uses the values: $P=100$, $N=325$, $B=350$, $R=500$ and $Q=900$. Like most programs, it adjusts the material score to encourage the exchange of pieces when ahead in material. The values of the pieces vary with the strategic character of the position: Rooks are better when the opponent has weak pawns, Knights are better in blocked positions, and so on. Such considerations are important, but I know of no program that takes them into account.

The assessment of mobility is more difficult. Counting the legal moves of each man is easy but inaccurate. It is necessary also to take into account the exclusion of men from squares controlled by the opponent and the immobilization of men by defensive functions, such as the shielding or guarding of a man or important squares. Detecting these factors is complicated and may involve tracing the relationships between several men.

Under vulnerability we have to consider unguarded pieces, the safety of the King, weaknesses in the pawn structure and pieces exposed to attack by less valuable men. Pawn weaknesses are easy to detect, and most programs take them into account. Measuring danger to the King is more complicated, but it is easy to detect some of the relevant features, such as disturbances of the King's pawn cover or the absence of friendly minor pieces nearby. Detecting unguarded and exposed pieces seems to be relatively simple, but oddly it is often neglected.

The MOVE Routine

Because of the rapid expansion of the game tree with depth, most of the processing time is spent in selecting and evaluating the terminal positions. It is therefore desirable for MOVE to maintain, along with the current position, information helpful to the LIST and VALUE routines. For example, it is more efficient for MOVE to keep track of changes in the material score than for VALUE to scan the board to do the same thing. Also, some programs maintain lists of the locations of each side's men to facilitate the generation of moves.

We have seen that sophisticated LIST
and VALUE routines would have to detect relationships between the men. Since each move changes only some of the relationships, it is more efficient to compute them in MOVE than to compute them all from scratch in LIST and VALUE. In general, the features needed for selection are the same as those needed for evaluation. For example, a backward pawn affects the evaluation and also suggests moves for both sides. The possessor of the pawn will try to advance it or protect it, while his opponent will try to prevent its advance and win it. Likewise any advantage suggests moves to maintain and exploit it; any disadvantage, moves to eliminate or mitigate it.

Levels of Skill

The United States Chess Federation rates its members at eight levels of skill based on performance in tournaments. In descending order they are Senior Master, Master, Expert and Classes A through E. From time to time computer programs have played in rated tournaments. Until recently their performance has been in the Class C or Class D range. Against this background the strong showing of Chess 4.5 startled everyone. At the conclusion of the Minnesota Open its rating had risen to Expert. It is still too early to assess its true strength, however. Although it is strong tactically, its grasp of strategy is well below the Expert level. The weak showing of Class A players against Chess 4.5 was caused largely by their unfortunate tendency to get into tactically complex positions, thereby playing into the computer's strength. The program may not be so successful once people learn how to play against it.

The sudden improvement in Chess 4.5 coincided with its transfer to a faster machine, enabling it to search two plies deeper in most positions. This supports the belief that chess skill depends mainly on the number of moves one can see ahead. It’s difficult to give a precise equivalence between depth of search and level of skill, though. The following rule of thumb is, I think, close enough to the truth to give some idea of the design requirements for strong programs. Let a search depth of four plies correspond to Class C, and assume that each additional two plies yields an increase of one level of skill. Thus, play at the Expert level would require a 10 ply search.

The Exponential Explosion

The depth of search is limited by the increase in the size of the game tree with depth. Suppose that B moves are selected
Search Depth | Number of Terminal Nodes
--- | ---
2 | 59
3 | 929
4 | 1,800
5 | 27,900
6 | 54,000
7 | 837,000

Table 7: Tree size as a function of search depth (D), assuming exhaustive search and the maximum possible number of alpha-beta cutoffs. The branching factor (B) is assumed to be 30. The number of terminal nodes is $2^{D/2} - 1$ when D is even and $\left(\frac{(D+1)/2 + B}{2}\right)$ when D is odd.

at each node. This number is called the branching factor or fanout. If D represents the depth of search, the tree has $B^D$ leaves; the tree grows exponentially with depth. A typical position might have 30 legal moves, and if no selection is exercised, the tree will have 27,000 leaves at a depth of three plies. This is probably already too large a tree to examine with a microcomputer in a reasonable time. We have not, however, yet taken alpha-beta pruning into consideration.

The effectiveness of the alpha-beta algorithm depends on how well the move list is sorted. The greatest possible reduction in tree size is achieved when the best move is always first on the list. Table 1 shows the tree size under this condition, assuming a branching factor of 30. Clearly, exhaustive search beyond six plies is impossible for a small computer. To play

strong chess a microcomputer will have to use selection. The question is: how much?

To derive a relationship between the branching factor and the depth of search, we have to make some assumptions. Let us assume that we must limit the size of the tree to 10,000 leaves, and that the alpha-beta algorithm reduces the effective branching factor from B to $B^{2/3}$. Then table 2 gives the desired relationship. Although much guesswork went into this table, it seems safe to conclude that an Expert-level program must be very fast or very selective.

The TECH Program

How simple can a program be and still play reasonable chess? The TECH program was developed in order to answer that question. It would be a good model to follow if you want to have a running program in the shortest possible time. Despite its simplicity, or perhaps because of it, TECH placed higher in computer chess tournaments than some of the more complicated programs. It is good enough to defeat only inexperienced human players, but that is true of most programs. For the newcomer to chess programming, the design of a TECH type program would be a good way to gain experience.

TECH considers all moves to a fixed depth, beyond which it considers only captures. The evaluation of terminal positions is based only on material. Hence there is no need for a VALUE routine; the evaluation is computed on the run whenever captures occur. When the program has an advantage of two pawns or more, it reduces the value of its own pieces slightly so that exchanges are favored. TECH sorts moves for two purposes: to increase the frequency of alpha-beta cutoffs, and to bring factors other than material to bear on the choice of a move. At ply 2 and lower, captures are considered first and the killer heuristic is used. The positions at ply 1 are assigned a rating that includes such factors as the number of legal moves, the advancement of the center pawns, and the proximity of the pieces to the center, to the enemy King, and to passed pawns. The program expands the ply-1 nodes in descending order of the rating, which thus breaks ties in the backed-up evaluation.

Because TECH does very little processing at each node, it is able to generate a relatively large tree. Cutoffs are frequent; basing the evaluation only on material ensures that the alpha-beta comparison will often give an equal result. The ply 1 rating procedure could be made more elaborate.

<table>
<thead>
<tr>
<th>Branching Factor</th>
<th>Depth of Search</th>
<th>Tactical Skill</th>
</tr>
</thead>
<tbody>
<tr>
<td>31.6</td>
<td>4</td>
<td>Class C</td>
</tr>
<tr>
<td>15.8</td>
<td>5</td>
<td>Class B</td>
</tr>
<tr>
<td>10.0</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>7.2</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>5.6</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>4.6</td>
<td>9</td>
<td>Class A</td>
</tr>
<tr>
<td>4.0</td>
<td>10</td>
<td>Expert</td>
</tr>
<tr>
<td>3.5</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>3.2</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>2.9</td>
<td>13</td>
<td>Master</td>
</tr>
<tr>
<td>2.7</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>2.6</td>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>
without slowing down the program noticeably. It would be interesting to see how much the program’s play could be improved in this way.

New Directions

Chess programming is still a young field. There are many ideas that have never been tried or never been developed sufficiently to determine their value. Experimentation by computer enthusiasts could play a major role in developing the innovations that will be needed for a Master-level chess program. Some of the less successful chess programs use ideas worth further consideration. Papers describing some of these programs are listed in the bibliography. Additional ideas can be found by comparing the behavior of programs and human players.

Some Ideas for the Future

Chess games between computers are often dull because the programs don’t follow any plan. They pursue general goals such as development and control of the center, but don’t formulate goals specifically appropriate for the position at hand. Goals are represented in the evaluation and rating procedures. Setting a specific goal is accomplished by making changes in these procedures. For example, the general goal of center control might be implemented in part by a term in the evaluation polynomial for the number of pieces bearing on the center. A routine for setting specific goals might add a term for the number of pieces bearing on a center square that the routine had determined to be particularly important.

Here are some of the types of specific goals that occur frequently:

- Get control of a key square.
- Attack an area of the board where the opponent is weak.
- Free an immobile piece.
- Save an attacked man.
- Maneuver a particular piece to a square where it will have a strong influence.

It should be fairly easy to determine how to modify the evaluation and rating procedures in such a way as to set these goals. However, it might be difficult to devise a procedure for choosing the specific goals.

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Each algorithm would use the results of the previous ones in the list. The program would contain much chess knowledge, which would best be represented in a form both compact and easily alterable.

**Prerequisites**

How good a chess player do you have to be to tackle some of these problems? Most people need only a basic understanding of chess strategy and the ability to find simple combinations. Far more important than chess knowledge is the ability to teach what you know to a very dull, nonhuman pupil.

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You will have to be able to state explicitly the reasons for the choices you make while analyzing a chess position. It’s not as easy as it sounds. Above all, it’s important to keep in mind that writing a chess program is a big project. A methodical approach, using structured programming and careful documentation, is absolutely essential.

Concluding Remarks

In this article I have tried to cover the basic ideas of chess programming and indicate some new directions for experimentation. I hope that many of you will be stimulated to get involved in this growing field of research.

BIBLIOGRAPHY


Creating a Chess Player

An Essay on Human and Computer Chess Skill

In a recent *Time* essay (see references) Robert Jastrow, director of NASA's Goddard Institute for Space Studies, predicted that history is about to witness the birth of a new intelligence, a form superior to humanity's. The pitiful human brain has "a wiring defect" that causes it to "freeze up" when faced with "several streams of information simultaneously." Jastrow suggests that "the human form is not likely to be the standard form for intelligent life" in the cosmos. Even on our own small planet, a new day is near at hand: "In the 1990s, . . . the compactness and reasoning power of an intelligence built out of silicon will begin to match that of the human brain."

We have always been fascinated by the idea of a machine that is capable of rational thought. Jastrow is neither the first nor the last person who is betting on rapid improvements in machine intelligence. His expectation that computers will rival humanity within 15 years seems optimistic to anyone who has watched half-a-dozen excited technicians flutter about for several hours trying to bring a crashed system back to life. This prophecy seems even more fanciful to those who have attempted to program machines to cope with pattern recognition, language translation or a complex game such as chess.

The chess environment, in fact, provides a particularly good example of the difficult problems which still need to be solved before silicon intelligence can become a reality. More than 20 years ago, Herbert Simon, a recognized expert in the field of artificial intelligence, predicted that within a decade, the world's chess champion would be a computer. This prognostication has not come to pass. Why was an informed scientist like Simon so wrong in his assessment of computer capabilities? A major factor is that computer scientists have often failed to appreciate the level of knowledge which is required to play master-level chess. They have also commonly underestimated the tremendous information-processing capacity of the human brain. Even though chess is a game of logic in which all legal moves can be precisely specified and in which nothing is left to chance, several centuries of intensive analysis have not exhausted the perennial challenge and novelty of the game. Psychologists have been actively studying the human brain for several decades and have discovered a fascinating mystery wrapped within an enigma. The more we learn about the brain, the more we are aware of our lamentable state of ignorance.

The Mind of the Chess Player

At a general level of knowledge, we have several provocative insights on the nature and structure of human chess skill. We know, for example, that the skilled chess player does not examine hundreds of possible continuations before selecting a move. We also know that superior chess players are not formidable "thinking machines" but in fact display a normal range of intelligence scores. Strong chess players, as a group, do not even appear to have special retention abilities such as having "photographic" memories. In most respects, top-flight chess players have the same intellectual capacities as the rest of the population and, in the technical details of move selection, seem to engage in the same type of information processing that is observed in much weaker players.
Our knowledge in these matters is based on the early work of Binet in France and that of de Groot in Holland and on more recent investigations by other scientists in the USSR and the United States. In the late nineteenth century, Binet was surprised to discover that masters did not have a vivid image of the board when playing blindfolded chess. Instead, they seemed to remember positions in abstract terms such as by specific relations among pieces. Interviews with masters clearly indicated that a photographic memory was not a prerequisite for being able to play many simultaneous games of blindfolded chess. In the 1930s and 1940s, de Groot worked with a number of strong chess players (from Grandmasters to strong club players) and had them verbalize their thought processes while selecting a move in a complicated position. His research indicated that the Grandmasters' general approach was highly similar to that of weaker players. They analyzed a similar number of moves (about four) from the initial position, a similar number of total moves (about 35), made a similar number of fresh starts (about six), and calculated combinations to the same maximal depth (about seven plies or half-moves, where a move is defined as a play by one side and a response by the other). The only clear measurable difference was that the Grandmasters invariably chose the strongest move while the weaker players did not. Thus de Groot concluded that Grandmasters play better chess because they pick better moves. Unfortunately, this conclusion is not very informative since it is obviously circular. The fact that de Groot's extensive study did not uncover any prominent differences in the move-selection strategies used by strong and average players implies that the analysis procedure itself is not the critical factor which determines chess skill.

An important clue to the difference between skilled and unskilled players was discovered by de Groot when he displayed an unfamiliar chess position to his subjects for a few seconds and then asked them to recall the position from memory. He found that masters recalled almost all the pieces while club players remembered only about half of them. Recent work in this country by Chase and Simon at Carnegie-Mellon University has indicated that novice players recall only about a third of the pieces. Chase and Simon also added an important control procedure. They demonstrated that the differences in recall ability completely disappear if the pieces are positioned randomly. This outcome indicates that the superior memory of the chess master is chess-specific and not a general trait.

Simon and Gilmartin have proposed that skilled chess players learn to recognize a large number of piece combinations as perceptual chunks and perform well in the recall task because they remember four or five chunks rather than four or five pieces like the novice. If the average chunk size is
three to four, the skilled player will recall 16 to 18 pieces.

On the basis of this analysis, skill in chess depends on a learned perceptual ability which is highly similar to that acquired by every schoolchild as he or she slowly builds up a large repertoire of words. Initially the child learns to read each word character by character and often does not understand the meaning of the word. The novice chess player perceives the chessboard in a similar way, assessing a position piece by piece and failing to recognize the meaning of common piece configurations. The adult reader recognizes words and phrases as basic units (chunks) rather than individual characters and has a recognition vocabulary of approximately 50,000 words. The skilled chess player, in a similar vein, recognizes a very large number of piece configurations (chunks) and understands what they imply both individually and in combination.

The critical aspect of move selection occurs in the first few seconds of the task. Based on his assessment of the position, the skilled player immediately recognizes appropriate long-term and short-term goals and has a good feel for the specific moves which are compatible with these goals. For this reason, only two to four moves on the average are given serious consideration. The difference between the Grandmaster and the expert lies in the fine distinctions which are made in the first few seconds of their analysis. Skilled chess players can play a remarkably strong game when they are given only five seconds for each move. In this short time, it is not possible to make a careful analysis of many different continuations. The player must have an "instinctive" feel for the correct move and be able to recognize key features and to understand both their immediate and long-term implications.

Human chess skill, therefore, is based on two highly refined capacities, pattern recognition and rapid information retrieval. The latter ability depends on the fact that human memory is content-addressable rather than location-addressable like that of a computer. Computer systems often have to search for a specific item of information in memory by conducting an exhaustive, linear search of an entire file. Human memory however is organized in an amazingly complex fashion such that most of us can easily recall a specific fact on the basis of a completely novel retrieval cue. For example, name a flower that rhymes with nose. In this case, your quick response demonstrates that words are grouped together on the basis of their phonetic similarity (ie: sound). Your ability to quickly recall words which are similar in meaning to the word fat (such as obese, chubby, rotund, flabby, plump and stout) demonstrates that human memory is also organized by semantic similarity (ie: meaning). When a person is given a retrieval cue which does not elicit an immediate response, he or she can usually find the correct information after a brief search of related ideas or concepts. This facility contrasts sharply with the extremely limited linear searches which are generally conducted with large computer based storage systems. Even sophisticated computer retrieval strategies which arrange the data base in multilinked lists with elaborate tree structures presently lack the large system efficiency displayed by their biological counterparts.

Pattern recognition and rapid information retrieval are not only key capacities for chess, but are also essential for a wide range of important human problem solving skills. Whether your field is medicine, engineering, plumbing or computer programming, you would be a complete failure at your job without these essential abilities. Jastrow's claim that machine intelligence will soon equal man's intelligence seems to
overlook the important points made in BYTE by Ernest Kent (see references). Kent emphasizes the fact that biological information processors have a vastly different architecture than their silicon imitations. In fact, he suggests that our lack of success in building a thinking machine stems from our attempts "to make a wrench do a screwdriver's job." Our modern high-speed computers were designed to do important tasks which men are not very good at, such as complex mathematical calculations.

The human brain evolved, in contrast, on its ability to identify important environmental events and to quickly recognize their significance. Natural selection has never placed much emphasis on our ability to multiply or our ability to compute the inverse of a matrix. Kent also reminds us that organic evolution worked with a very different kind of hardware than that which is available to the modern computer engineer. Biological information processors have an incredibly slow cycle time, less than 100 operations per second. The basic unit, the neuron, operates in milliseconds rather than in nanoseconds. The brain, however, makes up in quantity and in structural complexity what it lacks in speed. Computers, on the other hand, have many fewer components and a much simpler gating architecture, but are orders of magnitude faster.

It may be that present machine hardware configurations are simply inappropriate for efficient pattern recognition or semantic recall. An analysis of the history of computer chess is instructive. Although there have been numerous advocates for chess programs which imitate human playing methods, only a few have been attempted, and none of these have played reasonable chess. The earliest paper on machine chess, written by Claude Shannon in 1950 (see references), proposed a mechanical algorithm which was not modeled on human chess play. Shannon suggested a workable procedure for representing the board and piece locations, specified simple mathematical algorithms for generating the legal moves of each piece and gave an example of a straightforward technique for evaluating a position (see Chess Skill in Man and Machine, chapter 3). The key feature of Shannon's proposal was the adoption of the minimax technique as described by von Neuman and Morgenstern in 1944. The basic idea of the minimax technique is to assume that the player whose turn it is to play will always choose the move which minimizes his opponent's maximum potential gain. Hence, the name minimax.
The superior memory of the chess master is chess-specific and not a general trait.

The Type B Strategy

One of the difficulties of this approach is that a complete analysis of all possible continuations (type A strategy) very rapidly leads to an overwhelming number of potential positions. The look-ahead tree grows at an exponential rate and with an average, according to de Groot, of 38 legal moves at each position, a search involving three moves (three half-moves for each player) produces over 3 billion \((38^6)\) terminal positions. You may recall that de Groot's research indicated that human players regularly searched a tree to seven plies and sometimes much deeper. Because of this, Shannon concluded that it would not be possible for the machine to consider all possible legal continuations at each node of the game tree. Instead, he proposed a type B strategy in which only reasonable (ie: plausible) moves are pursued at each branching point. If the program considered only five continuations at each node instead of all 38, a 6 ply look-ahead would involve only 15,625 \((5^6)\) terminal positions.

The attractiveness of the type B approach seems overwhelming when the number of terminal positions increases exponentially with depth. The fact that skilled human players explore only a limited number of continuations at each choice point is additional evidence which favors the adoption of this strategy. It is not surprising, therefore, that most programmers have used Shannon's type B strategy in designing a chess program.

Sometimes our understanding of the real world, however, is not always as accurate as we presume. In selecting a type B strategy in preference to a type A strategy, the programmer does not necessarily simplify the problem. This approach was competently implemented in 1967 by Greenblatt at MIT. His program played reasonable, and at that time, fairly impressive chess. The major design problem in a selective search is the possibility that the look-ahead process will exclude a key move at a low level in the game tree. The failure to consider an important move can lead to a very serious miscalculation. A chess game can be lost by a single weak move. For this reason, it is of critical importance that a necessary move not be missed. The type B programs place a critical dependence on the accuracy of their plausible move generator. Chess is an extremely complex game and in many situations a move which at a superficial level seems unlikely, is, in fact, the best one. Grandmasters find these moves while lesser players, including machines, fail to see them. For a decade, several dozen individuals have tried to create a plausible move generator that is superior to Greenblatt's. The evidence is fairly clear, however, that type B programs have improved very little since 1967.

As strange as it may seem, recent progress in computer chess has come by abandoning the type B strategy. Shannon's logical analysis was made in a "stone-age" hardware environment and without knowledge of several important algorithms. Today, the type A strategy is not as ridiculous as it seemed in 1950. In addition, very few individuals anticipated the immense difficulty involved in constructing a competent plausible move generator. To become a chess master, a man has to study chess intensively (20 hrs or more a week) for at least 5 years. During this time he acquires an immense amount of detailed knowledge about the game of chess. Subtle features of a particular position are recognized immediately and suggest both short-term and long-term goals as well as specific moves. This kind of knowledge is sufficiently abstract that most players find it impossible to verbalize the relevant thought processes. The one factor which stands out clearly, however, is that the chess master has acquired a tremendous library of factual information which can be retrieved quickly and applied in apparently novel situations. No chess program has been able to duplicate this facility and, without it, the creation of a workable plausible move generator is next to impossible.

When a type A strategy is employed, however, this problem can be bypassed. By making all the moves plausible, the program never overlooks a subtle but important one. In fact, by reverting to a brute force search
of all possible continuations, the program often finds interesting combinations that are commonly missed even by strong human players. It seems ironic that the brute force approach (full width searching) produces many more brilliant moves than the smart approach (selective searching). This important discovery was made independently by Slate and Atkin at Northwestern (the authors of the current world champion chess program, Chess 4.6) and by the Russian KAISSA team.

Minimax and the Alpha-Beta Algorithm

Slate and Atkin's work has demonstrated that a full width search can be conducted considerably more efficiently than anyone had previously suspected (including Slate and Atkin; see references). There are a number of important developments which are responsible for this reassessment. The most important discovery was made in the late 1950s by Newell, Shaw and Simon as well as by Samuels. Because of the basic logic underlying a minimax search, it is not necessary to search the entire look-ahead tree before selecting the best move. Consider a simple 2 ply search (one move for you and one for your opponent). First you examine one of your possible moves and the 38 or so terminal positions which result from each of your opponent's legal replies. You select the one reply which is best, according to your evaluation function, for your opponent (i.e., the one which minimizes your own maximum potential gain). Next, you consider a second move for yourself and the 38 or so replies that your opponent can make to this move. In considering these moves, you discover that the third reply you examine would give your opponent a better outcome than his best reply to your first candidate. Immediately you realize that it is a complete waste of time for you to analyze any more of his replies to your second candidate. Since you are already guaranteed a worse position after the second move than after the first, it is reasonable to reject the second one and turn to your third candidate. This decision eliminates the need for evaluating 35 of the potential replies to your second candidate. A very tidy savings.

Historically, the score for the best move so far for White has been designated as \( \alpha \) and the score for the best move so far for Black has been called \( \beta \). Thus the name alpha-beta (\( \alpha-\beta \)) algorithm. When the tree is both wide and deep, this algorithm can reduce the number of terminal nodes to a small fraction of the number which would be examined by a complete minimax search. The beauty of this procedure is that it always produces the same result as the full minimax search.

An important factor in determining the efficiency of the alpha-beta algorithm is the order in which the moves are examined. If White's best moves and Black's best replies are considered first at each choice point, the search of the uniform game tree of height \( h \) (number of plies deep) and width \( d \) (number of successors at each node) will involve approximately \( 2 \cdot d^{h/2} \) terminal positions instead of \( d^h \) (see references, Knuth and Moore). The potential magnitude of this saving can be appreciated by considering our previous example with a 6 ply search: \( 38^6 \) is more than 3 billion while \( 2 \times 38^3 \) is about 110,000. Shannon might have given more consideration to the type A strategy if he had been aware of the alpha-beta algorithm and some of the other technical improvements which were to follow.

General Strategy

To maximize the benefit of the alpha-beta procedure, it is necessary to devise an efficient strategy for generating the moves at each node in an order which is likely to produce a cut-off, such that searching can be terminated at that node. There are several general heuristics which have proven their value time and time again. One is extremely simple and powerful: try capturing moves first. Because a full width search includes many ridiculous moves, a reply which involves a capture will often remove a piece which was "stupidly" placed en prise (i.e., attacked and insufficiently defended).

![Figure 1: Portion of a game tree for the opening game in chess. Square nodes indicate that White is to play; round nodes that Black is to play. Techniques such as alpha-beta pruning and minimax strategy are used to optimize the use of trees like this.](image)
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Captures also have the beneficial effect of reducing the number of potential offspring. An additional important characteristic of a capturing move is that it will generally have to be examined sooner or later in order to insure the quiescence of the terminal position. Because of this, every capture that is examined early generally reduces the amount of work which will have to be done later. In practice, investigators have reported a speed-up in search time of as much as 2 to 1 by simply putting all the captures at the beginning of the move list.

In addition to captures, there is another class of moves which is also effective for producing cut-oﬀs. These are called killers because they are moves which have produced cut-oﬀs in the immediate past and have been specifically remembered for that reason. A short list of killers is maintained by the program and whenever the legal capturing moves fail to produce a cut-oﬀ, each of the killers (if legal in the given position) is then examined. This killer heuristic is quite effective in producing a move order which enhances the probability of a quick cut-oﬀ.

The general features of the alpha-beta algorithm and its important servants, the capture and killer heuristics, were reasonably well-known late in the 1960s. In recent years, several important refinements have been added to this list. One of the most important is the staged or iterative alpha-beta search. For example, instead of conducting a 5 ply search all at once the search is done in stages, first a 2 ply search, then a 3 ply search, then a 4 ply search, and finally a 5 ply search. Superficially this might appear to be wasteful since the staged search requires the full 5 ply search eventually anyway. This is not at all the case. As each search is completed, the principal variation (best moves for each side at each depth) is used as the base for the next (1 ply deeper) search. The 3 ply search therefore starts with a move at ply 1 and a reply at ply 2 which has already been proven to be reasonable (from the machine's limited perspective). The 4 ply search therefore starts with a move at ply 1 and a reply at ply 2 which has already been proven to be reasonable (from the machine's limited perspective). The 4 ply search starts with reasonable moves at its first three plies. The 5 ply search has the benefit of reasonable moves at its first four plies. Because the efficiency of the alpha-beta algorithm is tremendously sensitive to move ordering, the spill-over in information from one iteration to the next has a surprisingly powerful effect. A single 1 stage 5 ply search might require 120 seconds of processor time. The last segment of the staged 5 ply search might require only half as much time (i.e.: 60). Since each iteration requires about five times as much processor time as its predecessor (the exponential char-
acter of the look-ahead tree is diminished somewhat by the alpha-beta algorithm), the staged 4 ply search would take about 12 seconds, the staged 3 ply search about 3 seconds, and the 2 ply search about 1 second. The total time for the iterative search would be approximately 76 seconds 

An added benefit of the iterative search, and, incidentally, the reason for its discovery in the first place, is that it provides a useful mechanism for time control. In tournaments, a move must be calculated within a fixed time limit such as 90 to 120 seconds. If one decides to do a 5 ply search in a single stage, it is possible to find oneself tied up in calculation after 120 seconds with no idea of how much more time will be needed to complete the search, and without a move to make until the search is completed. In some complex situations the search might take as long as 10 minutes — a disaster for time control. An iterative search allows one to predict the probable duration of the next iteration and to make a decision whether it is cost effective to initiate the next one. If this decision is a go and the search, for some reason, fails to terminate in the anticipated time, the machine can abort and play the move selected by the last iteration. This provides relatively neat and tidy time control. The iterative search was first mentioned by Scott in 1969 and was apparently discovered independently several years later by Jim Gillogly at Carnegie-Mellon, by Slate and Atkin at Northwestern and by the Russian KAlSSA team.

Refinements to the Type A Strategy

Several other refinements have also made the type A strategy more manageable. One of the time intensive activities involved in tree searching is move generation. This can be minimized by generating only one move at a time and seeing if it produces a cut-off before generating the next move. If a cut-off occurs and the node is abandoned, one can avoid generating a large number of potential moves. With the n-best approach, it is customary to generate all moves at each node and then invest time attempting to decide which ones are worthy of further consideration. Thus the smaller tree, obtained by selective searching, has to be partially paid for by an additional time investment in plausibility analysis.

Another time-intensive activity in the tree search is the repeated use of the evaluation function. Since many thousands of terminal nodes have to be evaluated in each move selection, any refinement that reduces the work of the evaluation function will pay rich dividends. There are three important

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One of these is called incremental updating. In order to make an evaluation of a node, it is necessary to have certain key facts available, such as which squares are attacked by each piece, which pieces are present, etc. This information can be newly calculated at each terminal node or can be incrementally maintained by updating the appropriate tables as the tree is generated during the search. This latter procedure is more complex to program but tremendously more efficient in terms of computing time because neighboring terminal positions are highly similar. They usually differ in respect to only a single piece, and therefore the updating procedure requires about 10 percent of the computations that would be expended if the evaluation data base were recalculated from scratch for each evaluation.

A second refinement in this category is the use of serial organization in the evaluation function. In order to assess the relative merit of a chess position, most programs place heavy emphasis on the material balance (i.e., the relative number of pieces for each side). This tradition is founded on the idea that winning or losing is strongly correlated with being ahead or behind in material. An additional rationale is that this information is readily available and easily updated.

In most programs material factors are so dominant that the other evaluation terms, such as mobility, pawn structure, King safety, area control, etc., taken together almost never account for more than two pawns. Because of this, it makes sense to compute the material balance factor first and then determine if the result is within two pawns of the target value. If not, there is no need to assess the other factors, because the final decision will be independent of their value.

This simple idea encourages one to organize the evaluation function in strict serial order such that influential (heavily weighted) terms are analyzed first and the result examined to see if a decision is possible based on this initial information. If not, the next most influential term(s) are examined and another determination is made. This process is repeated until an escape condition occurs or until all terms have been examined. In most cases, the evaluation will be terminated long before the list of potential terms has been exhausted. This technical refinement can save a significant amount of time.

A third procedure for speeding the evaluation process is to remember past evaluations. For instance, one should avoid re-assessing the same position two or more times. In chess, there are many pathways by which one can reach identical positions. In a 3 ply sequence in which the middle move remains constant, for example, the first and third moves can be interchanged and the resulting position will be the same. Transpositions such as this occur frequently in the end game where the King may have literally hundreds of 4 move pathways that end on the same square. Rooks, Bishops and Queens also have a special facility for reaching a particular destination square in multiple moves rather than in one or two.

A full width search (i.e., type A strategy) greatly accentuates this foolishness. By creating a large table of past positions which have been already evaluated, and using a hashing procedure to check if the present position is in the table, the programmer can completely eliminate a portion of the eval-
evaluation effort. In most middle game positions, this technique will produce a 10 to 50 percent saving. In certain end game positions, however, the transposition table can eliminate more than 80 percent of the evaluation effort. This idea seems to have been implemented first by Greenblatt in 1967.

An extension of this idea is to use the table to store likely moves as well as evaluations. By remembering a move which previously produced a cut-off, the table can facilitate move ordering decisions. In addition, the use of the same reply at a familiar position may have the added benefit of increasing the number of transpositions which will be encountered at later nodes. Additional details on the use of a transposition table are discussed in chapter 4 of Chess Skill in Man and Machine.

One of the most difficult challenges for a chess program is the end game. A machine which calculates a move for each position has difficulty competing with humans who "know" the correct move on the basis of their own or someone else's past experience. There are a huge number of end game situations in which a specific and highly technical strategy is required. Strong chess players study these intricacies at great length and use this knowledge at the chessboard to avoid unnecessary calculations. For example, a King and a pawn against a lone King is a win in some positions, and a draw otherwise. The same is true for a King and two pawns against a lone King and a pawn. If a Rook or minor piece is added to each side, the situation changes dramatically. Unfortunately our present day programs are oblivious to these subtleties. For this reason they can find the correct move only by engaging in prodigious calculations. Their human counterpart, on the other hand, "knows" the correct move after a cursory glance at the position.

Newborn (see references) has introduced a useful technique for reducing this knowledge gap. The main idea is to categorize familiar end game positions as wins or draws. Many games end with a King and a pawn fighting a lone King. Skilled players usually terminate the contest before it runs its inevitable course because the outcome is not in doubt. Newborn has shown that it is feasible, taking advantage of the symmetries of the chessboard, to make a bit map that indicates either a win (1) or a draw (0) for each potential square on which the lone King might reside for each of the potential locations of the opposing King and pawn. This knowledge can be encoded in approximately 300 bit boards of 64 bits each (see chapter 5 of Chess Skill in Man and Machine).

Although a tremendous amount of work and chess knowledge is required to complete this task, the end result is well worth the effort. When a position involving two Kings and a pawn is encountered anywhere in the look-ahead tree, it can be immediately scored with 100 percent accuracy as a win or a draw. This extends the look-ahead horizon of the program by as much as 12 to 15 plies for these specific situations, and eliminates all the tree searching effort which would normally be required. Furthermore, it permits accurate evaluations at the end points of a deep search, which allows the program to select a continuation which leads to a favorable end game. If this approach were extended to a wider range of situations, the machine's present knowledge deficit with respect to the end game would be greatly reduced.

These programming refinements, together with rapid hardware advances, have made the Shannon type A strategy feasible if not particularly elegant. For this reason it is possible to program a machine to play a game of chess which is free of gross blunders and which sometimes even contains an innovative move or two. Although this approach is clearly not a final solution, it does provide a solid base which can be used as a reliable starting point for future developments.

REFERENCES


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Microchess 1.5 for the Radio Shack TRS-80 microcomputer has been announced by Personal Software in conjunction with Peter Jennings of Microware Ltd. Microchess is a 4 K byte Z-80 machine language chess playing program described in "Microchess 1.5 versus Dark Horse," March 1978 BYTE, page 166. The program has three separate levels of play designed for beginners, intermediate players and experienced players.

The program is available in both Level I and II BASIC versions for the TRS-80. Standard algebraic notation is used to describe the moves to the computer. Every move is verified for legality to prevent user error, and a simple command allows temporary numbering of the squares to assist in move entry. The chessboard is displayed using the graphics mode available on the TRS-80.

Microchess 1.5 is being offered at a temporary introductory price of $19.95. Microchess 1.0 was described in What's New, February 1978 BYTE, page 200. Contact Personal Software, POB 136, Cambridge MA 02138. If you have questions on Microchess call (617) 783-0694. For Visa and Mastercharge credit card orders dial toll-free (800) 325-6400; in MO dial (800) 342-6600.

Boris is a recently developed chess computer that can flash messages to its opponent such as Illegal move, Congratulations, Stalemate, and I expected that. It is designed for all levels of ability from the beginner to the master player.

The electronic position programming permits the player to set up any board position desired. This programming flexibility is designed to allow advanced players to set up board situations and practice specific strategies. Also, beginners can use the feature to remove pieces at any time during a game for handicapping. Boris displays each rank electronically so the player always knows where the pieces are.

Boris will play either black or white or even play itself. If a player is unsure of what move to make, Boris is programmed to suggest the best possible move. When Boris gets his opponent into a corner, you can change places with it and see how it battles its way out of its own trap.

All the classic chess moves are in the computer's programs, such as castling, capturing en passant and queening, and Boris will solve all mate-in-two problems. Players will not get the same game twice since the computer is programmed for random play.

Boris costs $299.95 in a solid walnut case along with a compact chess board plus a set of pieces. Contact Chafitz Inc., 1055 First St, Rockville MD 20850.
Star Wars Simulation Now Available

The Star Wars simulation game, an adaptation of the end of the movie battle against the Death Star, is a real time simulation. Under player control, ships move in three dimensions to create a realistic simulation of actual space flight. Objects increase in size as they pass, weapons, deflector screens, and a directional control joystick are implemented in each ship. Ships of the rebel forces must pass through Imperial defenses and Tie-fighters to enter a channel on the Death Star.

The game requires the high density graphic display provided by Objective Design's programmable character generator. Written in 14 K bytes of 8080 assembly language, the program code is offered on Tarbell and CUT5 tape. Game rules and instructions for assembling the required ship control boxes are included in the total price of $7.50. The game is available from Objective Design Inc, POB 2032S, Tallahassee FL 32304.

Air Conditioner Selection Program in North Star BASIC

An Air Conditioner Selection Program (ACSP) written in North Star BASIC has been developed by HSC Computer Services Ltd, POB 43, Brooklyn NY 11236. The package allows the calculation of the necessary capacity of an air conditioner in BTUs per hour, taking into account the heat gain through windows, walls, ceiling, floor, electrical equipment, number of people in room and heat loss through doors and arches. The program applies a correction factor depending on locality in the United States. Also available are North Star error messages and their meaning.

Price of the ACSP package on diskette with a user's manual is $19.95, and the North Star Error Message Summary is $5.00.

SOFTWARE

Palo Alto Tiny BASIC Extended for North Star

California Software has made available Palo Alto Tiny BASIC Extended (PATB) for use with the North Star DOS. According to the firm, all save and load functions are available for disk storage and loading of programs. Programs are said to be automatically sized, typed and saved without leaving PATB, even the disk directory can be accessed while still in PATB. The extended version of the software allows string handling along with other advancements. Although originally designed as a memory saving interpreter, it provides an alternative language of North Star users at an affordable price. The product is available on diskette for $30 (plus 6% sales tax for California residents), including user's manual. Contact California Software, POB 275, El Cerrito CA 94530.

Circle 605 on inquiry card.

Software for North Star Disk Systems

The following software programs have been announced for the North Star Micro-disk System: Mailist is a general purpose mailing label program. It is said to be capable of producing formatted lists for tractor fed or Xerox type labels. Mailist will also sort lists for any field, name, address, city, state or zip. DOS In-Out Driver Version 4.0 is designed to set up mapped memory video boards with its driver located at C700H and a terminal at port 1. Register is a flexible cash register and inventory control program which records transactions, writes sales receipts and flags items which fall below prespecified reorder quantities. Prices are $39.95 for Mailist, $12.95 for In-Out Driver, and $299.95 for Register. Contact Alpha Data Systems, POB 267, Santa Barbara CA 93102.

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Air Conditioner Selection Program in North Star BASIC

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Price of the ACSP package on diskette with a user's manual is $19.95, and the North Star Error Message Summary is $5.00.

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SOLOS Tied to North Star DOS and BASIC

Microcomputer Resources Inc has announced a software package which is said to tie the North Star disk operating system (DOS) and North Star BASIC to the SOLOS 10 routines and allow the use of the CUT5 tape 10 port for archive storage of data. The tape routines are accessed as 10 devices. The cursor control keys on the SOL are interfaced to BASIC, allowing most edits in the line editor without the use of control keys. The package is said to allow the user to list the directory of a disk while in BASIC. Documentation for the software is included on the disk.

The package sells for $10 for the diskette and program, and a $2 shipping and handling charge. Contact Microcomputer Resources Inc, 3000 Medical Park Dr, Suite 107, Tampa FL 33612.

Circle 610 on inquiry card.

PDP-8 Simulator for 8080

The Simul8tor is said to be a complete PDP-8 simulator for the 8080. Simul8tor enables 8080 owners to utilize the thousands of PDP-8 programs available both commercially and through the Digital Equipment Corporation User's Society (DECUS). DECUS software such as ALGOL, BASIC, FOCAL, SNOBOL, FORTRAN, LISP, assemblers, editors, debuggers, floating point, etc, is readily available. The simulator is available in two formats: Intel paper tape and Intel Tarbell cassette. It comes complete with a user's manual, PDP-8 programming tutorial, PDP-8 loader, DECUS library information, and a source listing of its IO routines for users who wish to modify them. Prices are: one to three, $20 each; four to ten, $18 each; and 11 and up $15 each. Discounts may be applied to any format combination. Add $3 for each cassette ordered. Contact The Amide Corp, POB 600, Sag Harbor NY 11963.

Circle 611 on inquiry card.
The "Pro" fully encoded ASCII Keyboard by Cherry, Auto Repeat feature, 5 special function keys. 380mA/5V, (shown as mounted in "The Case", Below) $195.00, 3/98.00, 10/89.00

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"The Case" Beautiful and sturdy anodized aluminum case in deep black designed to contain the ESAT 200A, and with a bezel cut out for the Cherry "Pro" keyboard, (installed as shown above) Choose deep brown, light yellow, or crimson to accent or color code your installation. The only choice for hard-use institutional and educational applications. $699.00, 10/ 99.00

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RCA DOTS expandable to 64K microcomputer w/HEX keyboard input and voice output for graphics. Just turn on and start loading your program using the resident monitor on ROM. Pulsation selection of all four CPU modes, LED indicators of current CPU mode and four CPU states, Single step op. for program debug. Built in write protect. 4K ELF Expansion Board Kit with Cassette U/F $79.95

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DC clock with a 50" displays. Uses National MA-102 module with alarm option. Includes light dimmer, crystal timebase PCB boards, Fully regulated, comp. instructs. Add $3.50 for beautiful dark gray case. Best value

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What's New?

Personal Software Catalog Offers Large Selection of Software Packages

This new catalog is filled with software ranging from entertainment and self-education to personal finance, home information management and a variety of hobbies. A sampling of some of the software available includes: Stimulating Simulations, a set of ten games that simulate a situation that may be realistic or fanciful; Microchess, which enables the user to play chess against a TRS-80 computer; assembler in BASIC to make it possible to write programs in assembly language for the 6502 processor and have them translated to machine language for direct execution on the PET; and a word processing package available for PET owners who would like to compose and edit letters, articles and manuscripts at the computer and obtain corrected output at high speed. For a catalog containing these and other software packages, PET and TRS-80 owners should write to Personal Software, POB 136, Cambridge MA 02138, giving their serial numbers, memory size, and describing their most wanted software products.

Computer Chess Program Available in Assembly Language

Software Specialists, POB 845, Norco CA 91760, have announced a computer chess program for 8080 and Z-80 based microcomputers. This assembly language program conforms to all rules and conventions including castling, en passant captures, and promotion of pawns. The entire program, including input/output (IO) routines, will run in 8 K bytes of programmable memory. The user can select one of two board sizes for display, large for 24 by 80 inch videos, or small for television type writers and Teletypes. A level of difficulty between 2 and 5 is selected, with level 3 playing an average game. Both the user's and the computer's moves are displayed in standard chess notation.

For users with a North Star disk system, the program is available on disk and uses the DOS IO routines. The program is also available on paper tape with a 256 byte block reserved for the user's IO routines. Instructions are provided for loading the program and patching the IO routines. The program is available in either form for $50. A deluxe version which allows presetting of the board to any playing situation is available on North Star disk only for $50. The standard starting addresses are 2A00H for disk and 0000H for paper tape. Other starting addresses are available on request at no extra charge.

Attention Readers, and Vendors...

Where Do New Product Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the new new whiz-bang gizmo or save the world software package is of interest to the personal computing experimenters and homebrewers who read BYTE, we print the information in some form. We openly solicit such information from manufacturers and suppliers to this marketplace. The information is printed more or less as a first in first out queue, subject to occasional priority modifications.

Software Publication

A publication called The Software Exchange has been announced by its publisher Alan Bartholomew. Intended as a sort of "want ad" publication devoted to software produced by individuals, the plan is to put out six issues per year at a $5 per year subscription fee. For further details contact The Software Exchange, POB 55056, Valencia CA 91355.

System Monitor for 8085 Microprocessor

The Micro Mate-85 is a hardware connected system monitor for the 8085 processor. When operating in conjunction with a terminal or video display, it provides a means of examining and modifying memory locations and microprocessor registers at any point in an operating program through the implementation of addressable traps. The operating program may be started or stopped at any location, similar support may be stepped one location at a time. The monitor provides a means of loading or punching a paper tape of memory data for microprocessor systems not containing conventional peripheral IO.

Contact Spectrogram Corp, 385 State St, North Haven CT 06473.

Timeshare Disk BASIC System for North Star

A timeshare disk BASIC system is now available for users of the North Star floppy disk system. Designed to operate with microcomputers using the 8080 or Z-80 processors, Northshare provides up to four independent users with selectable memory partitions and buffered terminal outputs.

Minimum memory requirements for operation are 24 K bytes. There are no special hardware requirements other than additional terminals and IO ports to support the multiple users.

System includes one diskette with release 3 of North Star BASIC and DOS with Northshare supervisor and documentation package. Price is $3 per run from the Byte Shop of Westminster, 14300 Beach Blvd, Westminster CA 92683.

Assembly for Microprogramming of Bit Slice Microprocessors

The Signetics Micro Assembler is a software package designed to be used for the complete microprogramming cycle including defining microinstructions, writing and assembling programs, and generating paper tape output for real-time memory programming. The assembler permits flexible editing for debugging and program alterations through iterated loops, updates, and replacements, and includes a built-in test program to check system accuracy. The assembler is written in ANSI FORTRAN IV and can be run on any 16 or 32 bit computer with FORTRAN capability.

The microassembly language provides direct support for the 3002 and 2901-1 bipolar processors and the 8X02 Control Store Sequencer. Through the inclusion of explicit definitions, similar support can be obtained for the 3001 Microprogram Control Unit, as well as other bipolar processing elements and sequences.

The Micro Assembler is available in source form on 9 track tape for $775. Contact Signetics Corp, POB 9052, 811 E Arques Ave, Sunnyvale CA 94086.

Software Exchange, POB 55056, Valencia CA 91355.

Circle 642 on inquiry card.

System includes one diskette with release 3 of North Star BASIC and DOS with Northshare supervisor and documentation package. Price is $3 per run from the Byte Shop of Westminster, 14300 Beach Blvd, Westminster CA 92683.

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Whatis New?

A New Appliance Computer from Pertec

Sometimes a few surprises happen. A recent case in point is the appearance of a new computer from Pertec Computer Corp's Microsystems Division (ICOM and MITS). This new computer, called Attache, is a surprise because it fits the functional definition of the "appliance" computer: it can be purchased off-the-shelf in a ready to use condition. The base price of $1449 gets an assembled and tested computer, to which (at extra cost) one must add a BASIC interpreter on a read only memory board for the internal S-100 bus.

The Attache comes with a full ASCII keyboard, upper and lower case. It has a 10 slot board capability, LED indicators for on and off status, a reset switch which returns to the programmable read only memory monitor, a monitor PROM that controls operation of the computer from the keyboard, and a 75 Ω video output jack. The video output provides 16 lines of 64 characters and a choice of black on white or white on black display. The system includes forced air conditioning over the vertically mounted cards and a power supply which provides 10 V at 10 A (regulated to 5 V on boards), with preregulated +18 V and -18 V, each rated at 2 A. A 1 K volatile memory region and extra sockets for programmable read only memories are standard. The basic configuration includes keyboard, processor board, video board, and turnkey monitor board. Contact Pertec Computer Corp, Microsystems Division, 21111 Erwin St, Woodland Hills CA 91367.

The IsBC 80/10A Single Board Computer, an enhanced version of the IsBC 80/10, has been introduced by Intel. The 80/10A gives the user up to twice the read only memory capability presently available on the 80/10, for the same price. The 80/10A sells for $495 and includes the Intel 8080A central processor, system clock, 1 K bytes of programmable memory, up to 8 K bytes of nonvolatile read only memory and both parallel and serial IO. The unit is available from Intel Corp, 3065 Bowers Av, Santa Clara CA 95051.

Ithaca Audio Boards

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Z-80 CPU Board Most powerful 8 bit central processor available. Featuring power-on-jump, provision for on-board 2708. Accepts most 8080 software.

BK Static RAM Board High speed static memory at the lowest cost per bit. Includes memory protect/unprotect and selectable wait states.

2708/2716 EPROM Board Indispensable for storing dedicated programs and often used software. Accepts up to 16K of 2708's or 32K of 2716's.

Protoboard Universal wire-wrap board for developing custom circuitry. Accepts any size DIP socket.

Quality Components

<table>
<thead>
<tr>
<th>Product</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZILOG Z-80</td>
<td>$19.00</td>
</tr>
<tr>
<td>ZILOG Z-80A</td>
<td>$23.00</td>
</tr>
<tr>
<td>Intel 2708</td>
<td>$11.00</td>
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<tr>
<td>FAIRCHEILD 2102 LHPC</td>
<td>$1.60</td>
</tr>
<tr>
<td>FAIRCHEILD 2102 LPC</td>
<td>$1.35</td>
</tr>
<tr>
<td>IMSAI 8080 Kit with 22 Slot M.B.</td>
<td>$560.00</td>
</tr>
</tbody>
</table>

HOW TO ORDER

Send check or money order, include $0.00 shipping per order. N.Y.S. Residents include tax.

For technical assistance call or write to:

ITHACA AUDIO
P.O. Box 91
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Phone: 607/273-3271
Circle 296 on inquiry card.

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**circle 297 on inquiry card.**

**BYTE October 1978 199**
Cromemco Features a Z-80 Based Microcomputer

Cromemco’s System Three is ideal for a wide range of professional work in almost any field. It consists of a 4 MHz Z-80 based microcomputer, 32 K bytes of programmable memory (two 16 K byte cards) expandable to 512 K bytes, an RS-232 interface, a parallel printer interface, a video terminal with line editing and block mode transfer capabilities, and a fast line printer with 132 columns.

System Three is available with a number of options including a programmable read only memory programmer for development work, an additional dual disk drive and additional memory. With the optional second disk drive, System Three provides a megabyte of disk storage.

It has several provisions for protection of disks including software control for ejection of disks if desired, a key switch that will disable the disk eject buttons when in the LOCK position and motor driven disk loading and unloading.

Currently available software includes a FORTRAN IV compiler, a 16 K byte Z-80 BASIC, and a Z-80 macroassembler and linking loader. All software is available on standard, IBM format, soft sector diskettes.

The System Three mainframe is available for $5990. The additional video is available in two models for either $1595 or with expanded capabilities including line editing and block mode transfer for $1995. The additional line printer is also available in two models including a 180 character per second model for $2995 and a 60 character per second model for $1495. For more information, contact Cromemco Inc., 280 Bernardo Av, Mountain View CA 94040.

Circle 601 on inquiry card.

Compucolor Introduces Series of Color Home Computer Systems

The Compucolor II is a personal computer system available in five models, with its own 8 color, 13 inch (33.02 cm) diagonal display, a typewriter-like keyboard with 3 key rollover, 8080A processor, 4 K bytes to 16 K bytes memory (depending on the model), and a built-in minidisk drive mass storage device. The Compucolor II utilizes BASIC 8001, a conversational programming language with English-type statements and familiar mathematical notations.

Games like Star Trek, Blackjack, Chess, Checkers, Othello, and educational games for youngsters are available on diskettes. In addition, there are programs available for checkbook balancing and income tax compilation.

Prices for the Compucolor II range from $795 to $1995. Further information can be obtained from Compucolor Corp, POB 569, Norcross GA 30091.

Circle 602 on inquiry card.

S-100 Microcomputer Price Reduction

Quay Corp, POB 386, Freehold NJ 07728, has announced that its Q80AI, 2.80 based, S-100 compatible microcomputer has been reduced in price. The Q80AI, formerly priced at $550, is now available, factory assembled and tested for $350. The unit includes 1 K byte static programmable memory, 1 K byte programmable read only memory resident monitor, on board programmable read only memory programmer, keyboard interface and serial (RS232C/TTY) input and output (IO).

Quay has also package priced the Q80AI, the Q80SMB (8 K byte static memory board) and the Q-TBPE-80 (Palo Alto Tiny BASIC-extended) to sell for $495.

Circle 604 on inquiry card.
This is a one time purchase of NEW surplus keyboards, recently acquired from the Telecommunications Division of the Singer Corporation. The keyboard features 128 ASCII characters in a 63 key format, ASCII encoder circuitry, "N" key rollover, lighted shift lock, control, escape and repeat functions. Slipped panel and positive feel switches make it a professional quality keyboard at an excellent buy at only 55¢ each. Limited Quantities.

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- phone orders (916)966-2208 tax
- COD requires 5% Deposit all products guaranteed

Circle 288 on inquiry card.
**NEW!**

**16K E-PROM CARD**

IMAGINE HAVING 16K OF SOFTWARE ON LINE AT ALL TIME!

**KIT FEATURES:**
1. Double sided PC board with solder mask and silk screen and gold plated contact fingers.
2. Selectable wait states.
3. All address lines & data lines buffered!
4. All sockets included.
5. On card regulators.

**PRICE CUT!**

$57.50 kit

**SPECIAL OFFER:**

Was $69.95

Our 2708's (450NS) are $8.95 when purchased with above kit.

---

**FULLY STATIC!**

**ADD $20 FOR 250NS**

**KIT FEATURES:**
1. Double sided PC Board with solder mask and silk screen layout. Gold plated contact fingers.
2. All sockets included.
3. Fully buffered on all address and data lines.
4. Phantom jumper selectable to 5V or 12V.
5. Four 7405 reglators are provided on card.

**8K LOW POWER RAM KIT - $149.00**

**2 KITS FOR $279**

Fully Assembled & Burned In

$179.00

Blank PC Board w/ Documentation

$29.95

Low Profile Socket Set... 13.50

Support IC's (TTL & Regulators)

$9.75

Bypass CAP's (Disc & Tantalums)

$4.90

---

**SALE! 16K DYNAMIC RAM CHIP**

16K X 1 Bits. 16 Pin Package. Same as MOSTEK 4116-4. 250 NS access. 410 NS cycle time. Our best price yet for this state of the art RAM. 32K and 64K RAM boards using this chip are readily available. These are new, fully guaranteed devices by a major mfg.

**VERY LIMITED STOCK!**

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memory and 3 K read only memory, the board has the following peripheral chips:
two 8255s which can be programmed to be input ports, output ports, handshak­
ing ports and a bidirectional data port. One of the ports on each chip can use bit and reset commands. Each 8255 has a total of 24 possible IO lines. One 8253 has three 16 bit counters and timers in each chip. Each counter and timer can be programmed to be a binary counter or a binary coded decimal counter, a programmable one shot, a digital delay, a pulse wave rate generator (divide by N), a square wave rate generator, a software triggered strobe and a hardware triggered strobe.

The 8251 universal synchronous and asynchronous transceiver can be pro­grammed for various clock division ratios. All the usual UART functions are available plus synchronous serial IO to 56 bps. One of the 8253 counters is dedicated to the USA RT (8251). This allows complete software program­ability of bps rates. Over 60,000 bps data rates are available.

For further information, write to Space Time Productions, 2053 N Sheffield, Chicago IL 60614.

EMM Cuts Prices on 2 K Static Memory

A major price cut on the 3539 2 K byte static programmable memory has been announced by EMM Semi Inc, 3883 N 28th Av, Phoenix AZ 85107. In quantities of 500, the price has been cut from $7.80 to $4.05.

The 3539 is a byte organized 256 by 8 static programmable memory compris­ing a small memory on an integrated circuit. It replaces the older 256 by 4 programmable memories (2101 and 2111) for many small memory applica­tions, since only one component is re­quired instead of two. For further infor­mation, contact EMM Semi Inc.
APPLE II SERIAL I/O INTERFACE

Part no. 2
Baud rate is continuously adjustable from 0 to 30,000. For any peripheral connecter. Low current drain. RS-232 input and output. On board switch selectable 5 to 8 data bits. 1 or 2 stop bits, and parity or no parity either odd or even. Jumper selectable address.

SOFTWARE

Part no. 2
Baud rate is continuously adjustable.

Part no. 6085
DC POWER SUPPLY

Part no. 6085
Tape Interface Direct Memory Access. Record and play programs without bootstrap loader. Has balanced FSK encoder/decoder for direct connections to low cost recorder.

MODEM

Part no. 106
- Parallel ASC11 (TTL) input
- Video output
- 1K on board memory
- Output for computer controlled curser
- Auto scroll

Part no. 107
- Converts video to AM modulated RF, Channels 2 or 3. Very powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple.

Part no. 109
- Type 103 - Full or half duplex
- Works up to 300 baud
- Originates or answers
- No coils, only low cost components
- TTL input and output
- Selects 8 ohm speaker and crystal mic. directly to board
- Uses XRF SK demodulator
- Requires +5 volts
- Board $7.60, with parts $27.50

TIDMA

Part no. 112
- Tape Interface Direct Memory Access
- Record and play programs without bootstrap loader (no prom)
- Has FSK encoder/decoder for direct connections to low cost recorder at 1200 baud rate.
- Direct connections for inputs and outputs to a digital recorder at any baud rate.
- S-100 bus compatible
- Board only $35.00, with parts $110.00

UART & BAUD RATE GENERATOR

Part no. 101
- Converts serial parallel and parallel to serial
- Low cost on board baud rate generator
- Baud rates: 110, 150, 300, 600, 1200, and 2400
- Low power drain
- TTL compatible
- All characters contain a start bit and 5 to 8 data bits, or 1 or 2 stop bits, and either odd or even parity.
- All connections go to a 4 pin gold plated edge connector
- Board only $20.00, with parts $35.00 with connector $3.00

8K STATIC RAM

Part no. 300
- 8K Altair bus memory
- Uses 2102 Static memory chips
- Memory protect
- Gold contacts
- Baud rate generator
- S-100 bus compatible
- Vector input option
- TRI state buffered
- Board only $22.50; with parts $160.00

RF MODULATOR

Part no. 107
- Converts video to AM modulated RF, Channels 2 or 3. So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple.

Part no. 111
- Play and record Kansas City Standard tapes
- Converts low cost tape recorder to a digital recorder
- Works up to 1200 baud
- Digital in and out are TTL serial
- Output of board connects to: mic. in of recorder, earphone of recorder connects to input on board
- No coils
- Requires +5 volts, low power drain
- Board $7.60, with parts $27.50

RS 232/TTY INTERFACE

Part no. 600
- Converts RS-232 to 20mA current loop, and 20mA current loop to RS-232
- Two separate circuits
- Requires +12 and -12 volts
- Board only $4.50, with parts $4.50

RS 232/TTL INTERFACE

Part no. 232
- Converts TTL to RS-232, and converts RS-232 to TTL
- Two separate circuits
- Requires +12 and -12 volts
- Board only $4.50, with parts $7.00

To Order:
Mention part number and description. For parts kits add "A" to part number. In USA, shipping paid for orders accompanied by check, money order, or Master Charge. BankAmericard, or VISA number, expiration date and signature. Shipping charges added to C.O.D. orders. California residents add 6.5% tax. Outside USA add 10% for air mail postage, no C.O.D.'s. Checks and money orders must be payable in US dollars. Parts kits include sockets for all ICs, components, and circuit board. Documentation is included with all products. All items are in stock and will be shipped the day order is received via first class mail. Prices are in US dollars. No open accounts. To eliminate tariff in Canada boxes are marked "Computer Parts." Dealer inquiries invited.

* Circuits designed by John Bell

Dept. B, P.O. Box 21638, San Jose, CA. USA 95151
The EW-2001 Kit: A “Smart” VIDEO BOARD at a “Dumb” Price!

A VIDEO BOARD + A MEMORY BOARD + AN I/O BOARD – ALL IN ONE!

- State of the art technology using dedicated microprocessor I.C.
- Number of I.C.s reduced by 50% for higher reliability
- Master piece of engineering
- Fully software controlled

Priced at ONLY $199.95

Basic Software Included

Special Features:
- Programmable no. of scan lines
- Underline blinking cursor
- Cursor controls: up, down, left, right, home, carriage return
- Composite video

Options:
- Sockets ................. $10.00
- 2K Static Memory (with Sockets) ....... $45.00
- 4K Static Memory (with Sockets) ....... $90.00
- Complete unit, assembled and tested with 4K Memory ......... $335.00
- Basic software on ROM .... $20.00
- Text editor on ROM ....... $75.00

Display Features:
- 128 displayable ASCII characters (upper and lower case alphanumeric, controls)
- 64 or 32 characters per line (jumper selectable)
- 32 or 16 lines (jumper selectable)
- Screen capacity 2048 or 512
- Character generation:
  - 7 x 11 dot matrix

ASCII Keyboard Kit $74.00

Additional Improvements: Double Size Return Key

- Control Characters molded on key caps
- Power: +5V 275 mA
- Upper and Lower Case
- Full ASCII Set
- 7 or 8 Bits Parallel Data
- Optional Serial Output
- Selectable Positive or Negative Strobe, and Strobe Pulse Width
- 2 Key Roll-Over
- 3 User Defineable Keys
- P.C. Board Size: 17-3/16” x 5”

Apple II I/O Board Kit

Plugs into Slot of Apple II Mother Board

- 18 Bit Parallel Output Port (Expandable to 3 Ports)
- 1 Input Port
- 15 mA Output Current Sink or Source
- Can be used for peripheral equipment such as printers, floppy discs, cassettes, paper tapes, etc.

Free software listing for SWTP PR40 or IBM Selectric

Price:
- 1 Input and 1 Output Port for $49.00
- 1 Input and 3 Output Ports for $64.00

Dealer Inquiries Invited

Shipping: Keyboard and Video Board: $3.50; California residents add 6% sales tax
A Low Cost Minifloppy System

New 4 Headed Voice Coil Floppy

This 4 headed flexible disk drive stores up to 3.2 M bytes of data in the space required by a standard size floppy drive. The new PerSci Model 299 diskette drive interfaces to microcomputers using the 8080, 6800, or Z-80 processors, as well as minicomputers.

The Model 299 is a dual headed, dual diskette drive, reading and writing both sides of two 8 inch diskettes. Data can be encoded in single or double density in IBM compatible soft sectored formats or expanded hard and soft sectored formats on IBM diskette I, II, 11D or equivalent media. The drive will store up to 1 M byte of data in IBM type format, 1.6 M bytes unformatted single density and up to 3.2 M bytes in unformatted double density encoding.

PerSci's voice coil positioning system gives the PerSci drives an average seek time of 33 ms, five to seven times faster than stepper motor positioned drives. The speed and the capacity of the drive are achieved while maintaining industry standard data reliability figures of 1 in 10^9 soft errors and 1 in 10^12 hard errors.

The Model 299 features electric auto-load and can be unloaded by remote, host software control. Optical write protect secures the file.

The PerSci 4 headed drive measures 4.38 by 8.72 by 15.4 inches (11.1 by 22.1 by 39.1 cm) so two drives can be mounted horizontally or four vertically in a 19 inch (48.3 cm) rack.

The price is $1595 from PerSci Inc, 12210 Nebraska Av, W Los Angeles CA 90025.

Circle 525 on inquiry card.

Techtran's low cost minifloppy system, the 950 Microdisk, features over 200 K characters of storage. RS-232 or 20 MA current loop plug compatibility make the 950 a reasonable addition to timesharing and minicomputer or microcomputer based systems. The unit incorporates a Shugart drive and data can be recorded in either file or batch modes with the 950 automatically entering file names into the directory for total random access. Switch selectable data rates to 9600 bps supply fast on line or off line operations. A binary mode is an additional standard feature providing for code transparent applications.

The 950 is list priced at $1395. Contact Techtran Industries Inc, 200 Commerce Dr, Rochester NY 14623, (716) 334-9640.

Circle 527 on inquiry card.

New Unbundled Floppy Disk Based Computer Systems

Two fully assembled unbundled floppy disk based computer systems have been announced by Ohio Scientific, 1333 S Chillicothe Rd, Aurora OH 44202. Both of these computer systems feature a 6502A processor, 16 K bytes of dynamic programmable memory and an 8 inch floppy disk drive and interface. Both systems have a full 8 slot backplane which will accommodate system expansion. The systems are available as C2-8SK which includes a standard RS-232 serial IO port for use with an external computer terminal and Model C2-8VS which includes a 32 by 64 (81.3 by 162.6 cm) character video display board and a keyboard. Only a video monitor is required to complete the system. Both systems come fully assembled with software and manuals but without cases or power supplies. The C2-8SK with serial interface is $1590 and the C2-8VS with video interface is $2090.

Circle 528 on inquiry card.

Floppy Disk System for SwTPC 6800

The Southwest Technical Products Corp DMAF1 is a dual drive, single density, double sided 8 inch floppy disk system. The hardware consists of a SS-50 bus (SwTPC 6800) compatible direct memory access controller capable of handling up to four drives, two CalComp 143 M double density rated disk drives, 5 3/4 by 17 1/8 by 20 1/2 inch (14.5 by 43.5 by 52 cm) aluminum chassis, regulated power supply, drive motor control board, cooling fan, diskette and interfacing cables.

The supplied software includes a disk operating system. An 8 K byte BASIC interpreter with disk file capability and string functions is also included with the system. Each diskette holds approximately 600 K bytes of data; with two drives there is over one megabyte of data online.

The system is available in assembled and kit form (the drives are fully assembled). The unit weighs approximately 45 lbs (20.4 kg) and sells for $2095 assembled and $2000 as a kit, plus postage.

Contact Southwest Technical Products Corp, 219 W Rhapsody, San Antonio TX 78216.

Circle 526 on inquiry card.
DIODES/ZENERS
1N914  100v  10mA .05
1N4007  600v 1A  .08
1N4148  75v  10mA .05
1N4733  5.1v  1W Zener .25
1N753A  6.2v  500mW Zener .25
1N758A  10v  " .25
1N759A  12v  " .25
1N5243  13v  " .25
1N5244B  14v  " .25
1N5245B  15v  " .25

Sockets/Bridges
8-pin pcb .20 ww .35
14-pin pcb .20 ww .40
16-pin pcb .20 ww .45
22-pin pcb .35 ww .95
24-pin pcb .35 ww .95
28-pin pcb .45 ww 1.25
40-pin pcb .50 ww 1.25
Molex pins .01 To-3 Sockets .25
2 Amp Bridge 100-prv .95
25 Amp Bridge 200-prv 1.95

Transistors, LEDs, etc.
2N2222  NPN (2N2222 Plastic .10)
2N407  NPN .15
2N3906  PNP (Plastic - Unmarked) .10
2N3904  NPN (Plastic - Unmarked) .10
2N2907  NPN .15
2N2905  NPN 15A 60v .50
T1P125  PNP (Darlington) .95
LED Green, Red, Clear, Yellow, Yellow
D.L.747  7 seg 5/8" High com-anode 1.95
MAN72  7 seg com-anode (Red) 1.25
MAN310  7 seg com-anode (Orange) 1.25
MAN82A  7 seg com-anode (Yellow) 1.25
MAN74A  7 seg com-cathode (Red) 1.50
FN0359  7 seg com-cathode (Red) 1.25

C MOS
4000  .15
4001  .15
4002  .20
4004  .95
4006  .95
4007  .20
4008  .75
4009  .35
4010  .35
4011  .20
4012  .20
4013  .40
4014  .75
4015  .75
4016  .35
4017  .75
4018  .75
4019  .35
4020  .85
4021  .75
4022  .75
4023  .20
4024  .75
4025  .20
4026  1.95
4027  .35
4028  .75
4030  .35
4033  1.50
4034  2.45
4035  .75
4036  .75
4037  .69
4042  .65
4043  .50
4044  .65
4045  .125
4046  .45
4050  .45
4066  .55
4098/74C04  .25
4071  .25
4081  .30
4082  .30
MC14409  14.50
MC14419  4.85
4511  .95
74C151  1.90

9000 SERIES
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9309  .35  9601  .20
9322  .65  9607  .45

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MM5318  3.50  8251  8.50
2102-1  1.45  8255  8.50
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2114  9.50  8723  1.50
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TMS4044- 9.95  8737  1.00
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8212  2.95  8710  8.50

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INTEGRATED CIRCUITS UNLIMITED

Circle 180 on inquiry card.

BYTE October 1978  209
SUP 'R' MOD II

**LHF Channel 33 TV Interface Unit Kit**
- Wide Band B/W or Color System
- Converts TV to Video, display for home computers, CCTV camera, Apple II, etc., with Computers Direct, SOL-30, RS-80, Challenge, etc.
- MOD II is preferred to Channel 33 (LHF).

**MOD II**

$29.95 Kit

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>FREQUENCY</th>
<th>CASE</th>
<th>PRICE</th>
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<td>C1A</td>
<td>1 200MHz</td>
<td>HC33</td>
<td>$5.95</td>
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<td>3 800MHz</td>
<td>HC33</td>
<td>$5.95</td>
</tr>
</tbody>
</table>

**AUTO-TEL KITS**

As Featured in August - Popular Electronics

An Electronic Warning Device
For Temperature and Oil Failure

AUTOTEL - An audible alarm indicating potential engine damage. An audible signal (70 dB pulsing) immediately warns of a malfunction or failure. There is no sound during normal operation. Features CMOS circuitry. Complete kit with all components.$4.95/ea

**DIGITAL STOPWATCH**

- 1 to 999 seconds
- Displays in seconds, minutes, and hours
- Has elapsed time function
- Auto Power Off

**NEW**

$9.95 each

**JE700 CLOCK**

The JE700 is a 2-line clock rechargeable with 115 VAC or rechargeable alkaline batteries. It is not only a clock but also a digital stopwatch.

**JE803 PROBE**

The JE803 is a probe and storage case for the JE700. It provides a convenient way to store and transport the JE700 and its accessories.

$9.95 Per Kit

**PROTO BOARDS**

**PROTO BOARD 8**

$7.95

**PROTO CLIPS**

$4.95

**MAIL ORDER ELECTRONICS - WORLDWIDE**

1021 HOWARD AVENUE, SAN CARLOS, CA 94070

Advertised Prices Good thru October.
LRC Inc, Technical Research Park, Riverton WY 82501, has announced the availability of improved versions of its 7000 series matrix impact printers. Improvements include a new drive cam for the print head which is said to result in a uniform character width at the extreme ends of the print line as well as a decreased failure rate. Available in ticket printer models as well as in roll paper models, all units have multiple copy capability with the print line capacity of 40 columns at 12 characters to the inch. Ticket printer versions are available in 22 column models. 1 line or 5 line document validation is optional on roll paper models. Prices range from $66.50 to $282 depending upon model, options and quantity.

Circle 564 on inquiry card.

Data Communications Adapter

This 80-103A Data Communications Adapter has been developed to function as a S-100 bus compatible serial interface incorporating a fully programmable modem and Telco interface. These functions are usually accomplished by the use of two separate modules: a serial I/O board and an external modem. The 80-103A combines these features on a single board. A S-100 computer and a Telco 1001D data access arrangement (DAA) are all that is needed to control the adapter and interface to the telephone network.

The price of the 80-103A is $279.95 from DC Hayes Associates Inc, POB 9884, Atlanta GA 30319. Circle 565 on inquiry card.

New Programmable UART Interface

The COM6402, a programmable universal asynchronous transceiver (UART) with high clock frequencies, low power requirements and independent programming capabilities, has been introduced by Standard Microsystems Corp. Compatible with industry standard UARTs, the COM6402 is a pin for pin replacement for Harris HD-6402 and Intersil IM6402.

CMOS/LSI technology permits operator clock frequencies up to 3.2 MHz (200 K bps) while requiring only 10 mW of power. Duplex mode, bits rate, data word length, parity mode and number of stop bits are independently programmable through the use of external controls. There may be five, six, seven and eight data bits, odd, even or no parity, and one or two stop bits or 1.5 stop bits when utilizing a 3 bit code.

COM6402 is TTL compatible and requires only a single ±5 V power supply. It is fully double buffered to eliminate the need for external timing and provides start bit verification to decrease error rate. Three state outputs are bus structure oriented.

For further information, contact Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge NY 11787. Circle 566 on inquiry card.

Put Your PET on the Bus

The PET-488 cable assembly makes the PET computer plug-compatible with any device using the IEEE 488 bus. The PET computer can become the controller for a variety of electronic test equipment and computer peripherals. The cable assembly plugs directly into the edge connector on back of the PET computer and has an IEEE-488 compatible connector on the other end. The cable meets all IEEE-488 specifications for shielding and crosstalk and is 18 inches (45 cm) long. The price of the PET-488 cable assembly is $30 (California residents add 6% sales tax). Contact Pickles & Trout, POB 1206, Goleta CA 93017. Circle 567 on inquiry card.
2708/2716 EPROM MEMORY BOARD

- S-100 BUS
- 1-32 KBYTES USING EITHER 2708 OR 2716 EPROMS
- HIGH/LOW LIMIT ADDRESS RANGE SELECTION
- MEMORY BANK SELECT OPTION
- SOL™ COMPATIBLE MEMORY DISABLE
- SELECTABLE WAIT STATES
- FULLY BUFFERED INPUTS AND OUTPUTS
- DOUBLE SOLDER MASK
- SILK SCREENED PARTS LAYOUT
- COMPLETE DOCUMENTATION

$30. BARE

$100. KIT (LESS EPROMS)

TESTED AND ASSEMBLED $130. (LESS EPROMS)

RONDURE COMPANY
2622 BUTLER ST.
DALLAS, TEXAS 75235
214-630-4621

ASCII SELECTRIC

SPECIAL SALE
$875.00

TESTED WITH NEW ASCII ELECTRONICS

NOVATION DC3102A
Used Working

$150.00

RS 232 Connection
300 Baud.

SHUGART MINI-FLOPPY DRIVE

NEW PRICE
$325.00 ea.
Model SA-400

FLAT PACK ACOUSTICAL MODEM PICK-UP
Usable with most modem chips/kits
Used $17.50 (w/prints)

ORDERING INFORMATION:
We ship the same day we receive a certified check or money order.
Texas residents add 5% sales tax. Please call if you have a question.
Write for our CATALOG of many parts, terminals, printers, etc.
All items subject to availability. Your money returned if we are out of stock.

SHIPPING INFORMATION:
Modems: $2.00 each; 2 for $4.00 UPS.
Large Items & Parts: Specify Freight or Air Freight Collect
Foreign Orders: Add appropriate freight or postage.
We now take Master Charge and Visa orders, Specify full number, bank number and expiration date.
DUAL TRACE
15 MEGAHERTZ
PORTABLE MINISCOPE

FEATURES

- Dual Trace - 2 channel: separate, chopped or alternate modes.
- 15 megahertz bandwidth.
- External and internal trigger.
- Time Base - 0.1 microsecond to 0.5 Sec/div - 21 settings.
- Battery or line operation.
- Automatic and line sync modes.
- Power consumption less than 15W.
- Vertical Gain - 0.01 to 50 volts/div - 12 settings.
- Weight is only 3 pounds.

From the originator of the Digital Voltmeter, Non-Linear Systems comes the MS-215 Miniscope. It is a fine electronic instrument with a great deal of measuring capability and excellent accuracy. Its design is modern, utilizing the latest in low-powered integrated circuits, and it is packaged into the smallest practical size. The instrument fits into many briefcases and tool boxes with room to spare.

Operating characteristics have been chosen so that the MS-215 will make all of the measurements needed in servicing most electronic equipment. It is field-portable so its use is not restricted to the bench.

SPECIFICATIONS:

- Vertical Mode:
  - CH1, CH2, CH1 & CH2 (Chopped) & CH1 & CH2 (Line)
  - The following specifications apply to each channel:
  - Y Axis
    - Vertical input: 10mV/div to 50V in 12 calibrated ranges, as follows:
      - x1: 10mV/div to 100V/div in four ranges, each continuously variable.
      - x2: 200mV/div to 200V/div in four ranges, each continuously variable.
      - x5: 500mV/div to 500V/div in four ranges, each continuously variable.
  - Input Impedance: 1 MΩ shunted by 50 pf.
  - Bandwidth: DC/DC to 15 Mhz (DC to 8 Mhz ±3 db). AC, same as DC down to 2 khz.
  - Rise Time: Approximately 23 nS ± 1 division deflection.
  - Input Voltage: 250 maximum (DC and Peak AC).
  - Coupling: AC, DC or ground, switch selectable.
  - Linearity: Internal: sweep triggered from internal trigger source (In the furnished automatic and line sync modes.).
  - External: Controls function as for internal triggering (1 Megohm input impedance).
  - Sensitivity: Selects sync to positive or negative going waveform.
  - Level: Less than 1 div for internal trigger and less than 1 volt for external trigger.
  - Internal Calibration: Frequency is approximately 1kHz.
  - Display: Gap: 4x5 in, each division is 0.25 inch. Viewing area 11 1/4x13 5/8W.
  - CRT: Brush-white phosphor, medium persistence. CRT uses low power filament for low battery drain. Instant on.
  - Power: Battery or line operation.
  - On-Board Batteries: 19000000, rechargeable lead acid "D" cells.
  - Charging Time: 4 hours.
  - Scope Operating: Typically 4 hours.
  - Operating Temperature: 0° to 40°.
  - Shock and Vibration: Designed to withstand normal shock and vibration encountered in commercial shipping and handling.

- Horizontal Mode:
  - Internal Time Base or External Horizontal, switch selectable. In the XY mode, vertical input is through CH1 and horizontal input is through CH2.
  - Input Impedance: 1 MΩ shunted by 50 pf.
  - Bandwidth: DC/DC to 15 Mhz (DC to 8 Mhz ±3 db). AC, same as DC down to 2 khz.
  - Rise Time: Approximately 23 nS ± 1 division deflection.
  - Input Voltage: 250 maximum (DC and Peak AC).
  - Coupling: AC, DC or ground, switch selectable. Low frequency point on AC at 3 Hz.
  - Input Impedance: 1 MΩ shunted by 50 pf.
  - Deflection Factor: 4x5 in, each division is 0.25 inch. Viewing area 11 1/4x13 5/8W.
  - CRT: Brush-white phosphor, medium persistence. CRT uses low power filament for low battery drain. Instant on.
  - Power: Battery or line operation.
  - On-Board Batteries: 19000000, rechargeable lead acid "D" cells.
  - Charging Time: 4 hours.
  - Scope Operating: Typically 4 hours.
  - Operating Temperature: 0° to 40°.
  - Shock and Vibration: Designed to withstand normal shock and vibration encountered in commercial shipping and handling.

- Triggering Mode:
  - Sweep triggered from internal trigger source (in the dual trace modes, the internal trigger source is CH1). Trigger source is internal calibrater frequency to be used if there is no other trigger source available to synchronize the sweep. Trigger is derived from line frequency when using the battery charger.
  - Power: Battery or line operation.
  - On-Board Batteries: 19000000, rechargeable lead acid "D" cells.
  - Charging Time: 4 hours.
  - Scope Operating: Typically 4 hours.
  - Operating Temperature: 0° to 40°.
  - Shock and Vibration: Designed to withstand normal shock and vibration encountered in commercial shipping and handling.

- Accessories:
  - Furnished: Tilt stand, battery charger. 2 input cables.
  - Optional: Leather carrying case and probes.
  - Warranty: 1 year parts and labor. Made in the U.S.A.

- MS-215 with Rechargeable Batteries and Charger
  - $355.00

- Leather Carrying Case
  - $45.00

- Deluxe Combination Probe
  - $36.00

MS-15 Single Trace version of MS-215

$318.00

PRIORITY ONE ELECTRONICS

49118 West Rosecrans, Hawthorne, CA 90250

Phone Orders welcome (213) 973-4876

Circle 306 on inquiry card.
SALE S-100 BUS EDGE CONNECTORS SALE

3 LEVEL GOLD WIRE WRAP SOCKETS

1-24 25-49 50-99 100-249 250-999 1K-5K
8 pin* 41 $38 36 32 29 27 23
14 pin* 39 $38 36 32 29 27 23
16 pin* 43 $42 39 35 32 30 30
18 pin 63 $58 54 47 42 36
20 pin 80 $75 70 63 58 53
22 pin* 90 $85 80 70 61 57
24 pin 90 $84 78 68 63 58
26 pin 1.10 $1.00 .90 .84 .78 .74 .71
40 pin 1.50 $1.40 1.30 1.20 1.04 .89

Sockets purchased in multiples of 50 per type may be combined for best price.
All sockets are GOLD 3 level closed entry *End and side stachable. 2 level, Solder Tail, Low Profile, Tin Sockets and Dip Plugs available. CALL FOR QUOTATION

NLS MS-215 DUAL TRACER MINICOPTOR $43500

LIQUID CRYSTAL DIGITAL CLOCK-CALENDAR

- For Auto, Home, Office
- Battery or 120VAC (Nurt)
- Push button for seconds release for data
- Large digital display with auto 12 double-led time in 12/24 mode.
- MICRO-ALARM
- Digital clock operates with or without batteries to better than 1 second
- National Authorized

Price: $29.95

CARD EXTENDER

Card Extender has 100 contacts-per side on .125 center .Attached connectors are compatible with S-100 Bus Systems...

14 - G3 100 for $30.00
16 - G3 100 for $30.00
50 of each for $32.00
Sockets are End & Side stachable, closed entry

SALE S-100 BUS EDGE CONNECTORS SALE
New 1978-79 General Semiconductor Industries Product Catalog

The new 1978-79 General Semiconductor Industries Product Catalog contains a complete listing of the company's entire line of Zener diodes, temperature compensated diodes, NPN switching transistors, TransZorb silicon transient voltage suppressors, and C4R high speed and high voltage switching transistors.

This 238 page publication contains detailed device characterization and applications information for many of the units listed. The catalog lists the devices numerically within specific categories. General Semiconductor's environmental facilities and equipment is also listed. Contact General Semiconductor Industries Inc, 2001 W 10th Pl, Tempe AZ 85281.

Circle 622 on inquiry card.

Surge, Hash and Transient Protection

A new flyer from Electronic Specialists, POB 122, Natick MA 01760, discusses AC power line surges and hash. Suggestions are offered for protection from microprocessor damage or malfunction. Included are protection against lightening and error-producing power line hash. When writing for this free flyer, specify flyer AEP-7. Send stamped, self-addressed envelope.

Circle 622 on inquiry card.

New Electronic Test Equipment Catalog

This new 76 page 1978 catalog features electronic test equipment from major manufacturers including B & K Precision, Continental Specialties, Hickok and Simpson. North American Electronics specializes in direct catalog marketing of name brand electronic test equipment. The free catalog can be obtained by writing to Dept AA 78, North American Electronics, 1468 W 25th St, Cleveland OH 44113.

Circle 624 on inquiry card.

New Metric Components Catalog

A compilation of metric system standardized precision mechanical components and assemblies has been produced by PIC Design, POB 335, Benrus Center, Ridgefield CT 06877.

The 208 page edition contains over 25,000 components covering 24 different product categories. Also included in the catalog are working prints, technical reference data tables, gear data, metric terms and formulas, and many other design and production aids.

Circle 625 on inquiry card.


The January thru December 1977 Periodical Guide for Computerists indexes over 2200 articles from 25 hobby and professional electronic and computer publications. Articles, editorials, book reviews and letters from readers which have relevance to the personal computing field are indexed by subject under 100 categories. An author index is included which lists the subjects that each author wrote about. The more than 60 page book is available postpaid for $5 from E Berg Publications, 1360 5W 193rd Ct, Aloha OR 97003.

Circle 620 on inquiry card.
IBM® Selectric-Based
I/O Writers

Excellent Hobby Printers
- Series 72/731
- Heavy Duty
- 8½" Platen
- All Solenoids
- BCD Code

These terminals are from a large airline reservation system. They are heavy duty and were under continuous maintenance. The units have been in storage. We make every effort to ensure that all essential parts are included. Most work when plugged in. No warranties are given or implied.

Selectric Controller

The 3S-01 is a complete controller for the IBM Model 731 I/O typewriter for both input and output operations. With this controller the 731 becomes a versatile ASCII printer with the world famous Selectric quality and an alphanumeric ASCII-encoded keyboard with the wonderful Selectric feel. An eight-bit parallel input/output port (bidirectional or separate) is all that is necessary to add the KING of the hardcopy terminals to your system. Serial RS-232C is also available for connection to a serial communications port or modem.

Power supply requirements are 5VDC at .75A and 48VDC at 1A for the basic parallel controller. Additional power needed for the serial unit is ± 12VDC.

PRICE $249.95
ASSEMBLED BOARD

Complete Terminal Unit

This unit consists of:

1. A cleaned, checkout, repainted use Selectric. This unit has been converted for upper & lower case with new ball containing all BASIC characters.
2. Selectric controller unit allowing both input and output
3. Power supply (used)
4. Terminal table (new)
5. Assembled and tested. Ready to plug in and go
6. ASCII to computer
7. Credited for shipping by motor freight (collect)

PRICE $775.00 FOB TULSA

DEALER INQUIRY INVITED

Have 10 HP 26718 card readers left at $299.95 each FOB Tulsa.

Cashier Check or Money Order
Personal check allow 3 weeks. Units shipped collect. Price Net FOB Tulsa.

3 S Sales, Inc.
P. O. Box 45944
Tulsa, OK 74145
1-918-622-1058

Circle 376 on inquiry card.
POWER SUPPLY KITS

3 Hour Assemble Time—Complete Instructions Included.

KIT A: $57.50

KIT B: $47.50

3 Hour Assemble Time—Complete Instructions Included.

KIT A: $57.50

KIT B: $47.50

You May Buy Transformers Alone:

TQ0-80 $42.00

TQ0-90 $52.00

TQ0-81 $42.00

TQ0-190 $37.00

SHIPPING CHARGES: $4.75 per TRANSFORMER

FOR EACH ORDER $5.00 per TRANSFORMER.

SUNNY INTERNATIONAL

Mail Order

P.O. Box 423

Plot 745, A-103

Telephone: (603) 889-0112

Torrance, Cali 90507

_np420-8721

Oni 24 on inquiry card.

Circle 193 on inquiry card.

Circle 373 on inquiry card.

LOW LOW COST

3 Hour Assemble Time—Complete Instructions Included.

KIT A: $57.50

KIT B: $47.50

You May Buy Transformers Alone:

TQ0-80 $42.00

TQ0-90 $52.00

TQ0-81 $42.00

TQ0-190 $37.00

SHIPPING CHARGES: $4.75 per TRANSFORMER

FOR EACH ORDER $5.00 per TRANSFORMER.

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P.O. Box 423

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Telephone: (603) 889-0112

Torrance, Cali 90507

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Circle 284 on inquiry card.

Circle 103 on inquiry card.

Circle 203 on inquiry card.
New Enclosure for Homebuilt Microcomputers and Terminals

Designed with the personal computer user in mind, this new case is now available for home built microcomputers and terminals. Constructed of molded fiberglass, the case is large enough (18 by 20 by 8 inches [46 by 51 by 20 cm]) to enclose a variety of components and sturdy enough to support a monitor or portable TV. The keyboard area will accommodate both a full-size keyboard and a hex pad (not included with case). The textured polyester finish is available in beige, white or black. Cutouts may be easily made with an ordinary sabre saw. Cast-in brackets are provided for mounting to a base plate. The price of the case is $59.95. An optional aluminum base plate is available for $15.95. For more information contact Technical Products Company, POB 12983, Gainesville FL 32604.

Circle 582 on inquiry card.

New DIP Plugs and Covers

For the personal computer user or prototype engineer who needs to make interconnection assemblies, OK Machine and Tool Corp., 3455 Connor St, Bronx NY 10475, offers 14 and 16 pin plugs that fit into standard dual in line package (DIP) sockets. Plugs feature United Laboratories recognized glass filled thermoplastic bodies, and solder legs on the top side are slotted for easy attachment of cable leads. Rectangular legs aid in the insertion into the socket. The leg and solder lug are one piece gold plated phosphor bronze. Packed two to a package, complete with slotted top-entry covers, the plugs are $1.45 for two 14 pin units and $1.59 for the 16 pin version.

Circle 583 on inquiry card.

DM-1 Design Mate Adds Power, Metering to Solderless Breadboards

The output of the DM-1 variable regulated power supply is 5 to 15 VDC at up to 600 mA for 9 W maximum of electronic drive. The 0 to 15 VDC meter and the power supply are brought out to their own binding posts on the face of the Design Mate case. The meter can then be used to set up the power supply voltage and reconnected to measure voltage parameters within the circuit being designed. Load and line regulation is better than 1%, ripple and noise are less than 20 mV full load. The package weighs 3 pounds (1.4 kg) and comes assembled with detailed operating instructions. The 117 VAC 60 Hz version is priced at $69.95. A 220 V 50/60 Hz version is available for 10% more. For further information contact Continental Specialties Corp., 70 Fulton Ter, New Haven CT 06509.

Circle 585 on inquiry card.

Let the 3rd Hand Hold Your Circuit Boards

The 3rd Hand is an aluminum circuit board holder featuring one hand operation. Clamped to the edge of the workbench it holds the board at a convenient angle for placing parts and then is flipped forward to solder parts in place. The vinyl gasket protects the board from damage while holding it securely in place. The open end design allows it to hold circuit boards of any size. The price is $9.50 and the unit can be obtained from Studio 3, POB 11184, Kailua HA 96734.

Circle 586 on inquiry card.

Combination Coding and Video Layout Form

Introduced for BASIC Users

A new coding form designed for BASIC or other line number oriented languages is available from Stirling/Bekdorf, 4407 Parkwood, San Antonio TX 78216. With grid lines lithographed in soft blue on a white sheet, Form 78C1 combines coding and interactive video layout functions into one unit. The form has 28 coding lines and retains the 6 mm by 3 mm (.02 inches by .01 inches) grid needed for comfortable writing. Developed for minicomputer and microcomputer programming, Form 78C1's paper stock is a 22# opaque sheet which will take a plastic tip marker without spreading and will accept soft pencil equally well.

According to the company, it is pure enough for magnetic ink character recognition scanning equipment. For maximum writing ease and legibility, pens with fine hard plastic capillary action points and black ink should be used. Such pens as the Pilot Razor Point, Sanford's Expresso Fine Point or Big Sig II, Berol Super Flash and Flair Ultra Fine give sharp, crisp coding. The Pentel 0.5 mm mechanical pencil using 0.5 mm HB soft lead will give good results.

The BASIC coding and video layout form is available in 3 hole punched loose-leaf style in 100 sheet packages and as 3 hole punched 50 sheet pads with chipboard backing.

Circle 584 on inquiry card.
Circle 340 on inquiry card.
WANTED: For Microtata 1600 processor (Rea~ylin magnetic tape controller, disc controller and drive, core memory boards. Jack Hardman, 140 Forest Av, Glen Ridge NJ 07028, (201) 429-8880.

FOR SALE: Apple II Game of Life. High speed, 180 generations per minute for 36 by 36 cell utilization, $180 generations per minute for 36 by 36 cell.

FOR SALE: PDP for HP-25, Sniper, Cannon, Wumpus, Wumpus 2, Artillery, Artillery 2, Golf, Hi-Lo, Blackjack, Mastermind, (including Random number generator, Roulette, Poque-machine, Parachutist, Biohymon includes 100 year calendar), Amplifier (designs simple amplifiers). $4 each, for $8, 10 for $32 or complete set for $40. Also, programs custom written to requirements and to run on any of Hewlett-Packard range (specify). $10 each. I Webber, 92 Royal Pde, St Johns Wood 4060, AUSTRALIA.

FOR SALE: A Heathkit H8 and H9 and cassette recorder, fully assembled and running with 16 K of memory, liquids limited in sound and clear versions of BASIC. Will sell for $2450 or over $100 less than the price of the kits. Price includes shipping. George Walker, 67 Wyndham St, Guelph Ontario, CANADA (519) 823-1411.


FOR SALE: Two IMSAI 44:4 static programmable memory boards. Professional construction, from an operational IMSAI 8080 system. Going to Z-80 and do not want the 450 ns slow programmable memory in the system. $200 buys both boards. K. J. Hallwell, 2373 John Smith Dr, Apt F, Schaumberg IL 60194, or call after 6 PM (312) 885-0362.

FOR SALE: RC Shack ASCII keyboard assembled and tested for $40. Like new Ti-86 programmable calculator--make offer or swap for SwTFC hardware. Dennis Doanon, 2307 Carlisle Av, Racine WI 53404.

FOR SALE OR TRADE: Stand and enclosure for chain printer. Can be modified to house a Central type printer. Would consider trading for Tele- type model 35 QO parts. James Mullen, RR 5, POB 106, Evansville IN 47711.

FOR SALE: Updating to bigger system. Must sell Digital Group Z-80 system complete with Z-80 processor, video and cassette IO board, four parallel ports, 8 bytes static memory, complete with case and full documentation. Originally $1400, will sell for $900. Ray Cote, POB 66, Peterborough NH 03458.


FOR SALE: Programs for HP-25, Sniper, Cannon, Wumpus, Wumpus 2, Artillery, Artillery 2, Golf, Hi-Lo, Blackjack, Mastermind, (including Random number generator, Roulette, Poque-machine, Parachutist, Biohymon includes 100 year calendar), Amplifier (designs simple amplifiers). $4 each, for $8, 10 for $32 or complete set for $40. Also, programs custom written to requirements and to run on any of Hewlett-Packard range (specify). $10 each. I Webber, 92 Royal Pde, St Johns Wood 4060, AUSTRALIA.

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FOR SALE: Heathkit H8-Computer system, 16 K memory, H8:8 serial IO and cassette interface. All available Heath software, assembled and working, $800. Learns Electric Key and Stop action ideal for artist. Write for free. No extra charge. 1 VDC and -6 VDC all outlets rated at 5 A. $50, $125 or trade for KIM-1 or similar system.

FOR SALE: First 16 issues of BYTE except number 11 (July 1976 BYTE). Also February, March and April 1977 Data Communications for free. No reasonable offer refused. L R Chauvet, 11 Sussex Rd, Silver Spring MD 20910.

FOR SALE OR TRADE: Hewlett-Packard Model 180E dual trace oscilloscope. Excellent condition asking $300 or trade for cassette recorder. Also power supply with 524 VDC, 102 VDC, 46 VDC and -6 VDC all outputs rated at 5 A. Asking $300. Contact Roger at (504) 651-4153.

FOR SALE: Five computer memory and IO boards (all units from Digital Equipment Corp). They are all in new condition, but I cannot guarantee any of them as I do not have the equipment. Three of the boards are core memory (nonvolatile). There is a 4 K by 12 DEC part number H203P-33, unmarked board, and a 64 by 64 by 16 IO part number CF-4. The remaining boards plug into a PDP-11. One is an 8 K PROM board G231E-P2, the other is a control and data loops board number G106C. Boards go to the highest bidder. Marty Banish, 29A Forest Acres Dr, Bradford MA 01830.

FOR SALE: 12 issues of BYTE (October 1976 thru September 1977). Best offer or trade for what have you. G F Sabin, 6022 Sage Dr, Orlando FL 32807.

FOR SALE: PDP-15 computer 24 K of 18 bit core memory, 4 DEC tapes, Teletype, paper tape reader (punch, Fotran and Fortran IV), full mainenance. Dr L K Steinauf, Dept of Biochemistry, 1 U Medical School, Indianapolis IN 46202, (131) 264-7544.


WANTED: IMSAI/COMDEBIFF owners to join European based users group for software exchange, mutual assistance; or alternatively 6P/M European users group. Contact K A Geiger, 66 Rue Rothschild, 1202 Geneva SWITZERLAND.

FOR SALE: Fine 1958 SULLIVAN pipe organ with electric key and stops. £2500 ideal for arts and hobbyist integration of micro based C as described in two articles in February 1976 BYTE. Two manuals (51 keys), 32 pedals, nine ranks, 498 pipes, chimes, pistons, shutters; suitable for home or church installation (full daily use in home now). $6200 plus optional packing and shipping. Send SASE for complete specifications and details. Phil Bergstrom, 128 Jackson Av, Madison AL 35758.

I am looking for an individual or company willing to provide on site service contracts for the metropolitan New York City area. Equipment would be microcomputers and related peripherals. Also, looking for other owners who would like to have on site service and maintenance for their equipment. B Rabinowicz, 1061 54 St, Brooklyn NY 11219.

MUST SELL: 3P+S Processor Technology IO card. Two parallel IO's and one serial IO. $100, assembled and tested. Paper tape reader, 48 hour turnaround. David Audio OF-80A, used only several times, assembled and tested, $50; all that is needed is to interface a parallel input. PerCom Electronics cassette interface, all that is needed is a serial or parallel IO and cassette recorder. Assembled and tested. $50. Godbout PROM board, holds 8 K (5204) and 48K (2704) proms. $75 as assembled board and PROMS. Larry Belmonts Jr, 176 Yale St, Corpus Christi TX 78416, (151) 855-2687 or (151) 854-2662.

PROM PROGRAMMING: From binary paper tape: 1702A ($41), 2708 ($81. From hexadecimal or octal listing: 1702A ($55), 2708 ($181. You supply the read only memory. Quantity discounts for multiple board runs. I spent a four hour turnaround. David Corbin, 11704 Ilnen Dr, Rockville MD 20852, (301) 881-7571 after 6 PM.

FOR SALE: First 16 issues of BYTE except number 11 (July 1976 BYTE). Also February, March and April 1977 Data Communications for free. No reasonable offer refused. L R Chauvet, 11 Sussex Rd, Silver Spring MD 20910.
FOR SALE: Sharp Associates Selectric typewriter with keyboard, monitor and type ball. Sell to first person with certified check for $1200 or call and make offer above. Dave Dahlberg, 4375 Weber River Dr, number 95, Ogden UT 84404.

FOR SALE: IBM 6420 computer with 16 K memory, X 16 K programmable memory, 12 K static memory, 4 K read only memory, floppy controller, real time clock, Tarbell tape controller, one magnetic drive. All sending me SASE.

HELP: Southern Connecticut New Haven area; anyone using a Tarbell disk system please contact me for mutual system support. Also need help in maintenance, fine points of CP/M; will pay James Van Peil, 25 Sagamore Cm, Branford CT 06405.

FOR SALE: HP-25 Game Programs. I have several games, including a neat golf game. Each $2 good for multiple copies. 48 hour turnaround. David Whiffen, 443 -6324 or 738 -8086.

FOR SALE:Persic model 70 8 inch floppy drive and most compatible controller. Never powered up – perfectly new, $1000. Edward Downey, 1000 W Springfield, number 242, Richardson, TX 75080, (1211) 690-1523 home or 231 9303 ext 312 work.

WANTED: Modules/parts to restore a DEC RK05 microcomputer with 4 K memory. In input is in fixed decimal format; states are similar to Motorola assembler language, most features, however, are being supported. Additionally, a system symbol table is supported, enabling symbolic reference to system addresses, and assembly of routines to concentrate memory location. All for the M6800 Motorola micro. Input is in fixed format; statements are similar to Motorola assembler language, most features, however, are being supported. Additionally, a system symbol table is supported, enabling symbolic reference to system addresses, and assembly of routines to concentrate memory location.

FOR SALE: Complete microcomputer system. IMSAI 8080/mainframe with Wunderbuss, 4 MHz Z-80 processor, 50 K bytes of static non volatile memory, 12 K static memory, 4 K read only memory; 1 K buffer, etc), one GRI keyboard (case and one carrying case. all in perfect condition. Plus a ball of wax to pay for my honeymoon: IMSAI G938 board, H604 board, two 20 V regulator cards and software. I R Peterson, 669·23 West 800 South number 1, Richfield UT 84701, (801) 896-6110.

FOR SALE: HP-25 Game Programs. I have several games, including a neat golf game, two versions of Master Mind (for Com IV), Football, Tic-Tac-Toe, Mortar Battlefield, Battle the Dive Bomber and others. $2 each or trade. Jerry Hansen, 420 West 800 South number 1, Richfield UT 84701, (1211) 431-2889.

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To get further information on the products advertised in BYTE, fill out the reader service card with your name and address. Then circle the appropriate numbers for the advertisers you select from the list. Add a 15 cent stamp to the card, then drop it in the mail. Not only do you gain information, but our advertisers are encouraged to use the marketplace provided by BYTE. This helps bring you a bigger BYTE.

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