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In the Queue

Foreground

58  A "TINY" PASCAL COMPILER, Part 1: The P-Code Interpreter
Software—Chung-Yuen

94  LET YOUR FINGERS DO THE TALKING: Scanner Applications
Software—Ciccia

102 S2L: AN ALTAIR (S-100) TO LSI-11 BUS ADAPTER
Hardware Design—Bondy

166 WADUZITDO: How To Write a Language in 256 Words or Less
Languages—Kernathy

Background

22  THE MATHEMATICS OF COMPUTER GRAPHICS
Graphics—Posdamer

40  APL AND GRAPHICS
Software—Kellerman

68  SOME WORDS ABOUT PROGRAM STRUCTURE
Software—Hearn

82  ANTIQUE MECHANICAL COMPUTERS: The Torres Chess Automaton
History—Williams

114  MATH IN THE REAL WORLD
Software—Boney

156 GRAPHIC MANIPULATIONS USING MATRICES
Graphics—Hungerford

Nucleus

4  In This BYTE

6  On Entering Our Fourth Year

10  The NCC '78 Personal Computer Show

17  Letters

54  BYTE's Bits

54  BYTE's Bugs

120 Event Queue

123 Programming Quickies: Plugging the KIM-2 Gap

124 Clubs and Newsletters Directory

145 Book Reviews

147 Technical Forum: Making an H9 Understand Lower Case

177 What's New?

206 Unclassified Ads

208 BOMB

208 Reader Service
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If you intend to use your computer for arithmetic operations it is necessary to have a floating point arithmetic package. Joel Boney's article on implementing a binary floating point package will help you implement Math in the Real World if you don't have an appropriate package at your fingertips in a high level language or program library.

A background in vectors and matrices can give you a set of powerful tools for manipulating shapes on a graphics display. Read Jeffrey L Posdamer's The Mathematics of Computer Graphics. You may find that the mathematics is not as difficult as you think.

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On Entering Our Fourth Year

By Carl Helmers

With this issue, we begin our fourth year of publication of BYTE magazine. The project remains as exciting, if not more so, than when we first put together an issue of the magazine in the summer of 1975. A lot has changed as the people involved with this publication have grown and learned about the process of magazine production. Yet a lot remains similar.

The basic goal of this magazine is not likely to change: to provide readers with a continuing stream of novel ideas and information about computers and related fields.

The assumption made about the BYTE reader is that he or she possesses curiosity combined with a willingness to experiment with and learn about topics related to computers and computing. To this end we provide a wealth of tutorials on hardware and software aspects of computer science -- as well as specific "do it yourself" items on neat projects which can be done by the reader. And all this is tied together with an emphasis on the fun which can be had through the use of computing technology in various ways.

We started out with this idea about the goals of the magazine, and no real knowledge about how far we could take it. After all, the skeptics (on occasion including myself) would ask, can there be that many people interested enough in computers to buy your magazine? But, reflecting the growth of personal computing manufacturing, we went from a 96 page black and white first issue to a 208 page typical current issue, from essentially 0 circulation as of the decision to start the magazine to a present circulation in excess of 140,000 paid copies per month. Perhaps we even played a small part in promoting that growth by providing our advertising and editorial content as a service to the industry.
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Well, the games part is true. The rest of the claims should be taken with a grain of salt. All of the personal computers will help you learn about computers and how they work in general and the kinds of things they can do for you. Only a few have the capacity to grow and handle meaningful work in a very real sense. And they don't come for peanuts.

Remember, there's no free lunch.

So before you buy any personal computer, consider Sol, the small computer. Consider it because it costs more at the start so in the end it costs less. Consider it because it can grow with the complexity of the tasks you ask it to perform and grow with your ability to use it. No, it's not cheap. But it's not a delusion either.

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In sum, all small computers are not created equal and Sol users know it to their everlasting satisfaction.

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The NCC 78 Personal Computer Show

Chris Morgan, Senior Editor

Photo 1: Complex high resolution graphics created with UCSD Pascal.

Photo 2: Color graphics being generated by Exidy's new Sorcerer personal computer.

Photo 3: 8 K content addressable memory board from Semionics. The $525 price tag is the lowest we've seen for this type of memory.

The official attendance was 57,240—that's how many people came to the National Computer Conference in Anaheim CA June 5 thru 8.

Easily the biggest computer show in history, the NCC overflowed the huge Anaheim convention center into a neighboring garage annex converted to handle the extra booths. The personal computing section of the show has grown into a major show of its own in just two years: the crowds there were no less impressive than at the main show.

A diversity of products greeted visitors to the show: everything from digitizers to compilers; Pascal to peripherals; color video systems to surplus parts; and so on. One of the most significant hardware devices on view was an 8 K content addressable memory board for the S-100 bus from Semionics in Berkeley CA. In a normal memory, the address of data is input, and the memory reads from (or writes to) its
The $6,995 DP Center.

The IMSAI VDP-80

Until now, owning real computing power meant paying unreal prices. The IMSAI VDP-80 Video Data Processor is a complete computer, intelligent terminal and megabyte floppy disk mass storage system including disk operating system (IMDOS) and BASIC software. All in one compact cabinet. All for just $6995.* A complete desk top DP center.

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- **Drives, Printers, Plotters, Terminals, Modems and Tape Drives.** Supports up to six terminals or modems, and four tape drives. Drives plotters, serial printers and line printers (up to 300 lpm).

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*Base price VDP-80/1000 $6,995, with 32K RAM memory and dual double density floppy disk drive. U.S. Domestic Price Only.
Features and prices subject to change without notice.
Photo 4: A throng of people attends the Micro Mouse Maze heat being run by James Hamblen's large economy size "mouse," shown, which traversed the maze in 4:32:28 minutes - the second best time for the show.

Photo 5: Compucolor Model 3 with optional keyboard displaying some unseasonal color graphics. The unit is undoubtedly one of the most cost-effective full color graphics systems on the consumer market. Only 117 more shopping days left.

Photo 6: Color expansion board for the RCA Cosmac VIP computer. The board costs $89 and generates eight colors as well as musical tones.

Photo 7: Homebrew 3 voice computer controlled music synthesizer built by John Pratt and Don Shertz of Monterey CA.

contents at that address. In a content addressable memory, the data being sought is presented to the memory, and the memory returns the address of that data (or a suitable code if the data cannot be found.)

The UCSD Pascal Project people were on hand with some impressive graphics displays generated using the Pascal language, and John Pratt and Don Shertz of Monterey CA displayed their homebrew computer music synthesizer which sounded very good.

Mary Ann Dugan and Hal Glicksman displayed a program designed to help Mary's 7 year old son John who has cerebral palsy. Two widely spaced keys on the keyboard are activated by John's fists to move a cursor on a screen and spell out words. For more information, write Hal Glicksman, 76 Market St, Venice CA 90291.

The first entries competed in the amazing Micro Mouse Maze contest, cosponsored by IEEE Computer and Spectrum magazines. The object was to design a self-powered electronic "mouse" that could solve a maze in the fastest possible time. The sponsors of the contest were amazed (pun intended) at the response to the contest call: over 6000 people wrote for contest kits. Maze trials will be conducted at various computer shows over the next two years before a winner is declared.

These are just some of the highlights of a tremendous show. Next year the NCC will be in New York City. If attendance figures continue to climb at this rate, they'll have to hold the show in Madison Square Garden.
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To ensure that the fun never stops, and to keep Apple working hard, we've spent the last year expanding the Apple system. There are new peripherals, new software, and the Apple II Basic Programming Manual. And wait till you see the Apple magazine to keep owners on top of what's new.

Apple is so powerful and easy to use that you'll find dozens of applications. There are Apples in major universities, helping teach computer skills. There are Apples in the office, where they can help manage the family budget, control your home's environment, teach arithmetic and foreign languages and, of course, enable you to create hundreds of sound and action video games.

When you buy an Apple II you're investing in the leading edge of technology. Apple was the first computer to come with BASIC in ROM, for example. And the first computer with up to 48K bytes RAM on one board, using advanced, high density 16K devices. We're working to keep Apple the most up-to-date personal computer money can buy. Apple II delivers the features you need to enjoy the real satisfaction a personal computer can bring, today and in the future.

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Software: Ours and yours.

There's a growing selection of pre-programmed software from the Apple Software Bank — Basic Finance, Checkbook, High Resolution Graphics and more. Now there's a User Section in our bank, to make it easy for you to obtain programs developed...
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---

**Apple peripherals are smart peripherals.**

Watch the far right column of this ad each month for the latest in our growing family of peripherals. We call them "intelligent interfaces." They're smart peripherals, so you can plug them in and run them from BASIC without having to develop custom software. No other personal computer comes close to Apple's expandability. In addition to the built-in video interface, cassette I/O, and four A/D inputs with two continuously variable game paddles, Apple has eight peripheral slots, three TTL inputs and four TTL outputs. Plus a powerful, state-of-the-art switching power supply that can drive all your Apple peripherals.

**Available now.**

Apple is in stock and ready for delivery at a store near you. Call us for the dealer nearest you. Or, for more details and a copy of our "Consumer's Guide to Personal Computers," call 800/538-9696** or write Apple Computer, Inc., 10260 Bandley Drive, Cupertino, CA 95014.

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**Introducing Disk II**: instant access to your files.

Our newest peripheral is Disk II, a high-density 5 1/4" floppy disk drive for fast, low-cost data retrieval. It's perfect for storing large bodies of data such as household finances, address files and inventories; you can find any record in just half a second. No more searching through stacks of cassettes; with a few keystrokes, your system will load, store and run any file by name.

Disk II consists of an intelligent interface card, a powerful Disk Operating System (DOS) and one or two mini floppy drives. Your Apple will handle up to seven interface cards and fourteen drives, for control of nearly 1.6 megabytes of data, with no expansion chassis. The combination of ROM-based bootstrap loader and an operating system in RAM provides complete disk handling capability, including these special features:

- Soft sectored
- Random or sequential file access
- Program chaining capability
- Universal DOS command processor works with existing languages and monitor
- Full disk capability in systems with as little as 16K RAM
- Storage capacity: 113 kilobytes/diskette

See Disk II now at your Apple dealer. Sold complete with controller and DOS at $495.1

**Peripherals in stock**

- Hobby Board (A2B0001X), Parallel Printer Interface (A2B0002X), Communication Interface (A2B0003X), Disk II (A2M0004X).

**Coming soon**

- High speed Serial Interface, Printer II, Printer IIA, Monitor II, Modem IIA.

1 Price subject to change without notice.

**Apple's smart peripherals make expansion easy.** Just plug 'em in and they're ready to run. I've already added two disks, a printer and the communications card.

---

**Programming is a snap!**

I'm halfway through Apple's BASIC manual and already I've programmed my own space wars game.

**Those math programs I wrote last week— I just rewrote them using Apple's mini-assembly and got them to run a hundred times faster.**
A Solid State Keyboard as Modern as Your Computer

Solid state electronics has moved the computer quickly from the business world into personal uses. Meanwhile, computer keyboards have hardly moved at all.

Now TASA introduces a keyboard as modern as your computer. Don't confuse it with ordinary flex switches. It is fully solid state and self-contained, ready to plug in and use. Since it has no mechanical moving parts, it responds quickly to your touch. And it provides full ASCII coding in TASA's exclusive color-keyed layout that makes it easier to say what you want to say to your computer.

This is the TASA Micro Proximity Keyboard, and it sells for only $49.95. Despite the price, CMOS/LSI integrated circuits make it totally reliable inside. With the sensors behind a shield of polycarbonate—the most rugged plastic ever developed—it is also durable and reliable outside.

The TASA Keyboard contains all the features you would expect in a professional keyboard—shift, shift lock, control functions, and a normal typewriter format.

If you're tired of costly mechanical keyboards and kits you have to assemble, bring your computer up to date the easy way. Plug in a TASA Keyboard. It will never come between you and your computer.
The TASA Keyboard

Features:
- 51 Keys, with entire 128 position ASCII code output.
- All keys identified as to Unshift, Shift and Control outputs.
- Full 8-bit ASCII output with selectable positive or negative parity.
- Single power supply, 12.5 - 20V unregulated.
- Output TTL, DTL and CMOS-compatible.
- Full solid state design with no moving parts.
- Standard PC edge connector.
- Use on any flat surface, or with Optional plastic support stand (as shown)

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- 51 Keys, with entire 128 position ASCII code output.
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WANTED: A RANDOM NUMBER CIRCUIT

Writing a really good pseudorandom number generator is not an easy thing to do; Knuth devoted half a volume to the process. Also, if you base a computer game on a pseudorandom number generator, you have the awkward problem of supplying a seed for each game. For these reasons, I would like a way of getting truly random numbers into a microprocessor. One way to do this is to have the computer increment a counter while waiting for the user to enter something. If the computer is fast enough, the low order bits of the counter will be random. However, this method is not good for generating large numbers of random numbers, since the user must be consulted for each one. What I really want is a circuit which generates random bits. I've heard that such circuits exist, based on something called "noisy" diodes. Where can I get details?

Scott D Johnson
241 Linden Av
Ithaca NY 14850

Certain processors, like the Zilog Z-80, have methods of apparently forming a random seed number. Since the hidden refresh counter for dynamic memory is always in operation it can be paged whenever a seed for a pseudorandom number generator is required. Within certain constraints it may also be possible to use a series of these numbers as pseudorandom numbers.

WHAT A SMALL COMPUTER CAN DO FOR THE MULTIPLY HANDICAPPED

Being extremely green at this computer game and having no hardware experience (come to think of it no experience whatever) I have only had my Apple about three weeks, but I have a glimpse of the tremendous possibilities now open to me.

Since breaking my neck whilst on National Service in Germany, I've been able to move my head, left, right and slightly backwards and forwards and that's my lot. If anyone tries lying on the floor on his back, using the above movements and tries writing his name with a pen in his mouth (holding a pad above) they will quickly realise there's not a big variety of things someone in my position can do.

Now imagine the same person with the keyboard of a computer in front of him you find the limits go up tenfold.

I know there are machines like "Pussom" issued in certain cases by the UK government. It will connect the disabled to TV telephone, it will open doors and curtains, and work a typewriter, about a dozen functions and it costs between £1,400 and £1,600 depending on the number of functions.

The processor I have is an "Apple II" 16 K and because I have to work with a stick in my mouth, the shift and control keys have had to be modified so that they work like a typewriter and use two movements to lock and release.

The Apple has opened up a new world I didn't know existed. It now makes jobs possible, the design and colour graphics and all the games (and don't knock the games, remember your capabilities while lying on the floor) and all this at a touch with a stick, and at costs comparable with "Pussom."

All I have to do now is buckle down and do a lot of studying and practicing.

I hope this gives some of your readers a glimpse of what a computer could do for the disabled and severely disabled. Also wonder if they have the same problem I have of doing a bit more, and a bit more to find it's 3 AM, or later, and that you have to force yourself to turn that switch off.

Charles Smith
222 West Ct
The Thistle Foundation
Edinburgh EH16 4EB
SCOTLAND

SOME NOTES FROM JAPAN

You may be interested in details of two recent Tokyo shows. At the Business Machines Show Sharp featured a new programmable calculator, the PC1300. This features magnetic card program storage, alphanumeric printer and display. It has 26 memories (A thru Z), program size is up to "256 steps," two levels of subroutine nesting are allowed, size is 44 by 123 by 220.5 mm (1.7 by 4.8 by 8.7 inches), weight is 680 grams (8 ounces). Numeric format is 10 digit mantissa, 2 digit exponent. Display scrolling (programmed?) was demonstrated at the show. Display and printer are both 16 characters wide.

Continued on page 66
Considering a Microcomputer?

Be Sure to Check Out the Product Offerings of the World's Largest Full Line Microcomputer Company.

All Ohio Scientific machines come with microcomputing's fastest full feature BASIC-in-ROM or on-Disk for instant use.

### Challenger I Series

Economical computer systems that talk in BASIC. Ideal for hobbyists, students, education and the home.

- **Superboard II** — World's first complete system on a board including keyboard, video display, audio cassette, BASIC-in-ROM and up to 8K RAM
- **Challenger IP** — Fully packaged Superboard II with power supply
- **Challenger IP Disk** — Complete mini-floppy system expandable to 32K RAM

### Challenger IIIP Series

Ultra high performance BUS oriented microcomputers for personal, educational, research and small business use.

- **C2-4P** — The professional portable
- **C2-8P** — The world's most expandable personal machine for business or research applications
- **C2-4P Disk** — The ultimate portable
- **C2-8P Single Disk** — Ideal for education, advanced personal users, etc.
- **C2-8P Dual Disk** — Most cost effective small business system

### Challenger II Series Interface System

Same great features as Challenger IIIP Series for those who have serial terminals: small business, education, industry.

- **C2-0** — Great starter for users with a terminal
- **C2-1** — Great timeshare user accessory; cuts costs by running simple BASIC programs locally
- **C2-8S** — Highly expandable serial machine, can add disks, etc.

### Challenger III The Ultimate in Small Computers

The unique three processor system for demanding business, education, research and industrial development applications.

- **C3-S1** — World's most popular 8” floppy based microcomputer
- **C3-OEM** — Single package high volume user version of C3-S1
- **C3-A** — Rack mounted multi-user business system directly expandable to C3-B
- **C3-B** — 74 million byte Winchester disk based system. World's most powerful microcomputer

**OHIO SCIENTIFIC** also offers you the broadest line of expansion accessories and the largest selection of affordable software!

Compare the closest Ohio Scientific Model to any other unit you are considering. Compare the performance, real expansion ability, software and price, and you will see why we have become the world's largest full line microcomputer company.

---

I'm interested in OSI Computers. Send me information on:

- [ ] Personal Computers
- [ ] Small Business Computers
- [ ] Educational Systems
- [ ] Industrial Development Systems
- [ ] I'm enclosing $1.00 for your 64-page small computer buyer's guide.

Ohio residents add 4½% tax.

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**OHIO SCIENTIFIC**

1333 S. Chillicothe Road
Aurora, Ohio 44202
(216) 562-3101

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**Minimum Configuration**

**Base Price**

<table>
<thead>
<tr>
<th>Model</th>
<th>RAM</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Superboard II</td>
<td>4K</td>
<td>$279</td>
</tr>
<tr>
<td>Challenger IP</td>
<td>4K</td>
<td>$349</td>
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<tr>
<td>Challenger IP Disk</td>
<td>16K</td>
<td>$1190</td>
</tr>
<tr>
<td>C2-4P</td>
<td>4K</td>
<td>$598</td>
</tr>
<tr>
<td>C2-8P</td>
<td>4K</td>
<td>$799</td>
</tr>
<tr>
<td>C2-4P Disk</td>
<td>16K</td>
<td>$1464</td>
</tr>
<tr>
<td>C2-8P Single Disk</td>
<td>16K</td>
<td>$1738</td>
</tr>
<tr>
<td>C2-8P Dual Disk</td>
<td>32K</td>
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<tr>
<td>C2-0</td>
<td>4K</td>
<td>$298</td>
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<tr>
<td>C2-1</td>
<td>4K</td>
<td>$498</td>
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<tr>
<td>C2-8S</td>
<td>4K</td>
<td>$545</td>
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<tr>
<td>C3-S1</td>
<td>32K</td>
<td>$3590</td>
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<tr>
<td>C3-OEM</td>
<td>32K</td>
<td>$3590</td>
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<tr>
<td>C3-A</td>
<td>48K</td>
<td>$5090</td>
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<tr>
<td>C3-B</td>
<td>48K</td>
<td>$11,090</td>
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<tr>
<td>C2-4P Disk</td>
<td>16K</td>
<td>$1464</td>
</tr>
<tr>
<td>C2-8P Single Disk</td>
<td>16K</td>
<td>$1738</td>
</tr>
<tr>
<td>C2-8P Dual Disk</td>
<td>32K</td>
<td>$2597</td>
</tr>
</tbody>
</table>
If you are interested in an ultra high performance personal computer which can be fully expanded to a mainframe class microcomputer system, consider the C2-8P.

Features:
- Minimally equipped with 8K BASIC-in-ROM, 4K RAM, machine code monitor, video display interface, cassette interface and keyboard with upper and lower case characters. (Video monitor and cassette recorder optional extras.)
- The fastest full feature BASIC in the microcomputer industry.
- Boasts the most sophisticated video display in personal computing with 32 rows by 64 columns of upper case, lower case, graphics and gaming elements for an effective screen resolution of 256 by 512 elements.
- The CPU's direct screen access, coupled with its ultra fast BASIC and high resolution, makes the C2-8P capable of spectacular video animation directly in BASIC.
- Fully assembled and tested: 8 slot mainframe class microcomputer, six open slots for expansion. Supports Ohio Scientific's ultra low cost dynamic RAM boards or ultra high reliability static RAMs.
- The C2-8P can support more in-case expansion than its four nearest competitors combined.
- The C2-8P is the only BASIC-in-ROM computer that can be directly expanded today to a complete business system with line printer and 8" floppy disk drives.
- It is the only personal class computer that can be expanded to support a Hard Disk! (CD-74)

The C2-8P is the fastest in BASIC, has the most sophisticated video display and is the most internally expandable personal computer. Therefore, it should be the highest priced?

Wrong: The C2-8P is priced considerably below several models advertised in this magazine. The C2-8P is just one of several models of personal computers by Ohio Scientific, the company that first offered full feature BASIC-in-ROM personal computers.

For more information, contact your local Ohio Scientific dealer or the factory at (216) 562-3101.

OHIO SCIENTIFIC
1333 S. Chillicothe Road • Aurora, Ohio 44202
OHIO SCIENTIFIC offers the broadest line of BUS compatible microcomputer boards. This line includes several new and exciting products which are not available anywhere else, such as a three processor CPU board, dual port memories and a multi-processing CPU expander.

OHIO SCIENTIFIC has delivered approximately 100,000 boards based on our 48 line BUS and is now delivering thousands per week in 17 models of computers and dozens of accessories.

OHIO SCIENTIFIC'S BUS design incorporates high band width, high density and mass production technology to achieve a truly remarkable performance to cost ratio.

Here is just a sampling of the many OSI 48 BUS compatible boards available for the systems user, prototype, OEM user and experimenter.

<table>
<thead>
<tr>
<th>Product Identification</th>
<th>Special Features</th>
<th>Power Supply</th>
<th>Board &amp; Doc</th>
<th>Assembled Product</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Challenger II CPU</td>
<td>Can use four 2716 EPROMS instead of BASIC or can be configured for disk</td>
<td>+5/ - 9</td>
<td>500</td>
<td>C2-0</td>
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<tr>
<td>BASIC-in-ROM</td>
<td></td>
<td></td>
<td>39.00</td>
<td>298.00</td>
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<tr>
<td>6502 based CPU</td>
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<td></td>
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<tr>
<td>with serial I/O</td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>4K RAM, machine code</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>monitor</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Challenger III CPU</td>
<td>1 megabyte memory manager, software programmable vectors</td>
<td>+5/ - 9</td>
<td>510</td>
<td>C3-0</td>
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<tr>
<td>has 6502A, 6800 and</td>
<td></td>
<td></td>
<td>NA</td>
<td>490.00</td>
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<tr>
<td>280 micros, RS-232</td>
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<td></td>
<td></td>
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<tr>
<td>serial port, machine</td>
<td></td>
<td>+5/ - 9</td>
<td>5002</td>
<td>NA</td>
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<tr>
<td>code monitor</td>
<td></td>
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<td>125.00</td>
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<tr>
<td>5602 multi-processing</td>
<td>4K RAM, machine code monitor</td>
<td>+5/ - 9</td>
<td>5000</td>
<td>NA</td>
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<tr>
<td>CPU expander runs PDP-8, 280 and</td>
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<td>9800 code</td>
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<tr>
<td>RAM</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>16K static RAM</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>(Ultra low power)</td>
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<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<td>+5/ + 12/ - 9</td>
<td>520</td>
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<tr>
<td>(low cost)</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>(low cost)</td>
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<td>24K static RAM</td>
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<td>+5/ + 12/ - 9</td>
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<td>(high density)</td>
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<td>520</td>
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<td>4K static RAM</td>
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<td>520</td>
<td>CM-3</td>
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<td>(2102 based)</td>
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<td>CM-3</td>
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<td>16K dynamic</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>(Ultra low cost)</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<td>32K dynamic</td>
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<td>+5/ + 12/ - 9</td>
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<td>48K dynamic</td>
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<td>EPROM Boards</td>
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<td>6K 8834 EPROM board</td>
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<td>4K 1702A EPROM board</td>
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<td>CM-3</td>
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<td>I/O Boards</td>
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<td>CM-3</td>
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<tr>
<td>Audio Cassette interface Kansas City standard 300 baud</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
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<td>RS-232 port board</td>
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<td>CM-3</td>
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<td>Combination audio cassette two</td>
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<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>8 bit DACs, one fast A/D and 8</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>channel input mux</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>Combination RS-232 two 8 bit DACs,</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>one fast A/D and 8 channel input mux</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>32 by 32 character video display interface</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>32 by 64 character video display interface</td>
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<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>16 port serial board RS-232 and/or</td>
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<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>high speed synchronous</td>
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<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>Parallel (Centronics) Line Printer Interface</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>96 Line Remote Parallel Interface</td>
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<td>520</td>
<td>CM-3</td>
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<td>520</td>
<td>CM-3</td>
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<td>Single 8&quot; floppy disk 250</td>
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<td>CM-3</td>
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<td>Kbytes storage</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
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<tr>
<td>Dual 8&quot; floppy disk 500</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>Kbytes storage</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>74 Million byte Winchester disk and interface</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>OTHER</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>8 slot backplane board with connectors</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>Prototyping board</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>Card Extender</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>215NS access time automatic power down standby mode</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>Can be daisy-chained to n-slots</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>Handles over 40 16 pin IC's</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
<tr>
<td>With connectors</td>
<td>215NS access time automatic power down standby mode</td>
<td>+5/ + 12/ - 9</td>
<td>520</td>
<td>CM-3</td>
</tr>
</tbody>
</table>

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The Mathematics of Computer Graphics

The personal computing literature is filled with material describing the hardware of microprocessors using video graphics. A great deal has also been written about specific graphic applications including video games, computer art, etc. Computer graphics is, however, a powerful tool that requires for its use an understanding of a set of underlying computing and mathematical principles. The purpose of this article is to present some of these principles in the context of personal computing.

The screen of a video display is essentially a space with two dimensions. While a number of schemes exist for dealing with two-dimensional spaces, the most common is Cartesian coordinates. Each point in the space is represented by a pair of numbers corresponding to its distance from two axes at right angles to each other. On a video display this pair of numbers corresponds to the scan line number and picture element within the scan line. The notation \([x, y]\) will be used here to denote the element number and scan line number. Due to the nature of displays, the values for \(x\) and \(y\) are integers of limited range. Each pair of values corresponds to a unique point in the display space.

For many problems in which computer graphics is useful, a second space is used. This is the problem space (see figure 1). This corresponds to the description of the problem geometry as opposed to the screen. The representation \([u, v]\) will be used here for problem spaces. For Space War its dimensions may be measured in parsecs, for a tennis simulation it may be measured in inches, etc. Problem spaces may be integer or real.
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bounded or unbounded and are defined by the nature of the problem, not the use of computer graphics as a tool.

Naturally, there must be a way to convert from one space to the other when both are used. If

\[
\begin{align*}
xs_{\text{min}} &= \text{left screen value} \\
xs_{\text{max}} &= \text{right screen value} \\
ys_{\text{min}} &= \text{bottom screen value} \\
ys_{\text{max}} &= \text{top screen value}
\end{align*}
\]

and

\[
\begin{align*}
up_{\text{min}} &= \text{minimum problem space u coordinate value} \\
up_{\text{max}} &= \text{maximum problem space u coordinate value} \\
v_{\text{min}} &= \text{minimum problem space v coordinate value} \\
v_{\text{max}} &= \text{maximum problem space v coordinate value}
\end{align*}
\]

then the point \([u \ v]\) in problem space maps into a point \([x \ y]\) in screen space as follows:

\[
\begin{align*}
x &= \left(\frac{u - up_{\text{min}}}{up_{\text{max}} - up_{\text{min}}} \right) \times (xs_{\text{max}} - xs_{\text{min}}) + xs_{\text{min}} \\
y &= \left(\frac{v - vp_{\text{min}}}{vp_{\text{max}} - vp_{\text{min}}} \right) \times (ys_{\text{max}} - ys_{\text{min}}) + ys_{\text{min}}
\end{align*}
\]

In most cases, operating on individual points is only a beginning. Generally, techniques are needed to deal with line segments that connect points to define figures and regions.

If two points \(P_0 = [x_0 \ y_0]\) and \(P_1 = [x_1 \ y_1]\) are to be connected by a line segment, it is often necessary to compute every point on the connecting line (see figure 2). A traditional representation of the straight line is of the form:

\[
y = mx + b
\]

where

\[
m = \frac{y_1 - y_0}{x_1 - x_0} \quad \text{and} \quad b = y_0 - (x_0 \times m).
\]

To compute the series of points that would represent the line segment connecting \(P_0\) and \(P_1\), a program would start with the point at \((x_0, y_0)\) and \(x = 0\) and add \(m \times \Delta x\) and \(b\) to \((x, y)\) as \(x\) increases from \(0\) to \(x_1\) (\(\Delta x\) means a small increment of \(x\)). It is important to realize that \(m\), \(b\) and the intermediate values of \(x\) and \(y\) may take on non-integer values. For each intermediate point, the rounded values of \(x\) and \(y\) are used to designate a picture element to be displayed as part of the line's representation.

An alternative to this scheme is the "parametric" line representation. Here, the mathematical representation of the infinite line that passes through \(P_0\) and \(P_1\) is not used.

Instead, we represent only the points between \(P_0\) and \(P_1\):

\[
x = (1-t)x_0 + tx_1 = x_0 + t(x_1 - x_0) \\
y = (1-t)y_0 + ty_1 = y_0 + t(y_1 - y_0)
\]

where \(t\) varies from 0 to 1

\[
(x, y) = (x_0, y_0) \quad \text{at} \quad t = 0 \\
(x, y) = (x_1, y_1) \quad \text{at} \quad t = 1
\]

A line similar to the above line is generated, but with simpler, more direct computations.

For more advanced systems, a number of hardware schemes for line generation exist. Since hardware is not the topic of discussion in this article, refer to reference 1 for a discussion of binary rate multipliers, digital differential analyzers and multiplying digital to analog converters.

Another basic graphics element is the polygon. The polygon is a plane figure consisting of all points inside and on the boundary of a simply connected series of straight lines. For our purposes it is more convenient to represent a polygon by a list of its vertices than by a list of the entire set of displayed points. Polygons raise the issue of the differences between video or raster displays and line drawing vector or calligraphic displays.

The line drawing display has been a standard graphics device. It contains hardware to draw lines between points in the screen space. The image is drawn by tracing over each line in the image in the order the lines were specified. Thus, only points on displayed lines are scanned.

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screen positions which are parts of the displayed image, the scanning beam is intensified, causing images to appear on the screen. On a line drawing display, polygons can be represented by their boundaries; on a raster display they can be “colored in.”

Displaying Polygons

A polygon is represented by an ordered set of points: \((x_0, y_0), (x_1, y_1), \ldots, (x_n, y_n)\).

An alternative notation for this collection is a matrix:

\[
M = \begin{bmatrix}
    x_0 & y_0 \\
    x_1 & y_1 \\
    \vdots & \vdots \\
    x_n & y_n \\
\end{bmatrix} = \begin{bmatrix}
    m_{11} & m_{12} \\
    m_{21} & m_{22} \\
    \vdots & \vdots \\
    m_{n1} & m_{n2} \\
\end{bmatrix}
\]

Each element of the matrix is a number, specified by its row index and column index. In memory, arrays are typically stored in consecutive locations in either row or column order. It is necessary to calculate an element address from the row and column indices of a particular element in order to access it.

Given the vertices, how can the displayed interior points be calculated? Let us assume (as is usually the case) that the display scans from top to bottom and from left to right. For each line segment in the polygon, determine the vertex with the maximum y value and sort the edges in descending order by the maximum y value. Every vertex in the polygon is now represented in two places: as the beginning and end of two lines. Beginning with the topmost vertex, a line generation algorithm is used on any line that crosses the current y value. Because of the sort that was performed, line segments which begin lower on the screen may be ignored. Since both ends of the line segment are present, a line is dropped from the computation when its “lower” end is passed. For every line passing through the current y value, the x value has been calculated. The points generated are now sorted by x value.

Starting with the minimum x value, fill in picture elements on the scan line until the next value is encountered; leave empty picture elements until another picture element (if any) is encountered. As the program scans from left to right, the x values occupying odd numbered positions (1st, 3rd, …) in the x-sorted list cause picture element insertion to begin; the even position elements cause picture element insertion to be superseded. Figure 3 shows how this process can be generalized and applied to an arbitrary plane figure in outline form, i.e. a letter “P.” This procedure is repeated as the y value is stepped down the screen space for each scan line until the “lowest” vertex is encountered, ending the figure.

Transformations

Now that the basic graphic elements have been defined in terms of points and a set of algorithms which generate lines and arbitrary figures from the points, it is necessary to examine the operations needed to manipulate points to perform useful tasks. There are three basic transformations in two dimensions: translation, rotation, and scaling or magnification.

Translation is the movement of a point or points by an amount in x and an amount in y. The motion is such that neither the shape, size nor orientation is changed. It may be expressed as:

\[
x' = x + \text{change}x \\
y' = y + \text{change}y
\]

where the \text{change}x need not equal \text{change}y.

If all of the points associated with a line or figure are translated by an equal amount, the graphic element is translated without change in size, shape or orientation. Figure 4

![Figure 3: Creating a letter P with a raster scanning video display. During each scan line the program creates blanks until it comes to the first line. After this point it creates solid picture elements until it encounters the next line, whereupon it switches back to blanks. The algorithm states that solid picture elements should follow odd numbered line intersections and that blanks should follow even numbered line intersections.](image-url)
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Figure 4: Translation in the xy plane.

shows the effect of a translation applied to our arbitrary figure, the letter “P.” Rotation is a somewhat different problem. It involves a computation which maintains shape but changes orientation. A rotation will generally leave only one point in the two-dimensional space with its position unchanged: the center of rotation. For the sake of simplicity, the rotation computation is developed with the point (0,0) as the center of rotation. The polar coordinate representation is used (see figure 5). Later it will be shown how to rotate about any arbitrary point. The point to be rotated, P₀, is at position (x₀,y₀) (see figure 6). This is at a distance r from (0,0) and the line from the origin to P makes an angle of a with the x axis. From trigonometry we know that:

\[
\begin{align*}
x₀ &= r \cos(a) \\
y₀ &= r \sin(a)
\end{align*}
\]

If P₀ is rotated about (0,0) by an angle of b to become P₁ then

\[
\begin{align*}
x₁ &= r \cos(a+b) \\
y₁ &= r \sin(a+b)
\end{align*}
\]

but from trigonometry we may substitute for the sum-of-angles form:

\[
\begin{align*}
x₁ &= r \cos(a) \cos(b) - r \sin(a) \sin(b) \\
y₁ &= r \cos(a) \sin(b) + r \sin(a) \cos(b)
\end{align*}
\]

The last of the basic transformations is scaling or magnification. This involves a change in size without change in orientation. Depending on the definition of shape, it is either unchanged or changed “without distortion.” As in rotation, only a single point in the plane is unchanged by a particular scaling transformation and once again, for convenience, the origin [0 0] is left unchanged. The equations:

\[
\begin{align*}
x₁ &= sx₀ \\
y₁ &= sy₀
\end{align*}
\]

will scale x and y by a factor s. The factor may be greater than or less than 1. If a negative value is used for s, then reflection about the origin is performed. If the scale factors for x and y are different, then “stretching” is accomplished. Figure 7 illustrates several scaling transformations applied to the “P” figure seen in several earlier illustrations.

Vectors and Matrices

The use of matrix notation allows simplified extensions and combinations of the basic transformations. A matrix is a rectangular array of numbers identified by row and column numbers. Every row in a particular matrix has the same number of entries, as does every column. The notation A(i,j) refers to the element of matrix A in the i-th row and j-th column. A matrix has a size associated with it, [r c], which defines the
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number of rows and number of columns. For matrices A, B and C each having the same number of rows and columns, the following rules are true:

\[ A = B \text{ if } A(i,j) = B(i,j) \text{ for all elements} \]
\[ A = B + C \text{ when } A(i,j) = B(i,j) + C(i,j) \text{ for all elements} \]
\[ A = B - C \text{ when } A(i,j) = B(i,j) - C(i,j) \text{ for all elements} \]

While addition and subtraction of matrices follow in fairly simple fashion from scalar (nonmatrix) arithmetic rules, multiplication and operations similar to division are not at all similar. (A scalar is a quantity that is completely specified by a single number, compared with multiple number data constructs, which are vectors and matrices.)

A matrix with only one row is called a row vector. Similarly, a matrix with only one column is called a column vector. The subject of matrix multiplication is first examined with these simplified forms. While there are two forms of vector multiplication, only the dot product (also called the vector-inner-product) is presented here. Again, using a matrix A (the row vector), B (the column vector) and C (their product) the vector product computation will be described. A vector product can exist only if the number of elements in A and the number of elements in B are equal. If each of these has N elements then

\[ C = A(1,1) \times B(1,1) + A(2,1) \times B(1,2) + \ldots + A(N,1) \times B(N,1). \]

This is called the dot product of the two vectors. It is the sum of the pairwise products of their elements. C, the dot product of the two vectors, is a single number (a scalar) not a vector or matrix. For example:

\[
\begin{align*}
A &= \begin{bmatrix} 1 & 2 & 3 & 4 \end{bmatrix} \quad \text{row vector} \\
B &= \begin{bmatrix} 3 \\
5 \\
7 \\
11 \end{bmatrix} \quad \text{column vector}
\end{align*}
\]

then
\[ A \cdot B = C = 1 \times 3 + 2 \times 5 + 3 \times 7 + 4 \times 11 = 78 \]

Now suppose that A and B are not restricted to one column and one row, respectively. Instead, we let A have size \([r \times c_A]\) and B have size \([r \times c_B]\). The matrix product can only be computed if \(c_A = c_B\): that is, the number of columns in A is equal to the number of rows of B. Two matrices for which this is true are called conformable. C will now have size \([r \times c_B]\), inheriting its size from both A and B. Each element in C (which is no longer a scalar) results from the dot product of a row in A with a column in B:

\[
C(i,j) = A(i,1) \times B(1,j) + A(i,2) \times B(2,j) + \ldots + A(i,N) \times B(N,j)
\]

where
\[ N = c_A = r_B \]
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matrix, with zeros everywhere but on the diagonal, where the value 1 is placed. The diagonal is the set of elements where the row index equals the column index. For example, if I and M are both 3 by 3 matrices, then IM = M:

\[
\begin{bmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1
\end{bmatrix} =
\begin{bmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1
\end{bmatrix}
\]

Now let's turn back to rotations, and see how these may be applied to a collection of points describing a figure on the display screen.

Two comments are worth noting at this stage. It is often useful and necessary to apply the same transformation to several points. This occurs when applying a transformation to items such as polygons or more complex collections of points. Additionally, it is useful to combine basic transformations to create more complex transformations.

A collection of points may be represented as a matrix:

\[
\begin{bmatrix}
x_0 & y_0 \\
x_1 & y_1 \\
\vdots \\
x_n & y_n
\end{bmatrix}
\]

Recall the basic operations of scaling, rotation and translation:

Scaling (about the origin)
\[
x_1 = sx \cdot x_0 \\
y_1 = sy \cdot y_0
\]

Rotation (about the origin)
\[
x_1 = x_0 \cos(b) - y_0 \sin(b) \\
y_1 = x_0 \sin(b) + y_0 \cos(b)
\]

Translation
\[
x_1 = x_0 + \text{changelog} \\
y_1 = y_0 + \text{changelog}
\]

If these transformations could be represented as appropriate matrices, they could be applied simultaneously to all points in the collection. Scaling may be represented in matrix form as:

\[
\begin{bmatrix}
x' \\
y'
\end{bmatrix} = \begin{bmatrix}
s_x & 0 \\
0 & s_y
\end{bmatrix}
\begin{bmatrix}
x \\
y
\end{bmatrix}
\]

or, for a collection of points:

\[
\begin{bmatrix}
x'_0 & y'_0 \\
x'_1 & y'_1 \\
\vdots \\
x'_n & y'_n
\end{bmatrix} = \begin{bmatrix}
x_0 & y_0 \\
x_1 & y_1 \\
\vdots \\
x_n & y_n
\end{bmatrix} \begin{bmatrix}
s_x & 0 \\
0 & s_y
\end{bmatrix}
\]

Rotation through angle \(b\) about the origin may be represented as:

\[
\begin{bmatrix}
x'_0 & y'_0 \\
\vdots \\
x'_n & y'_n
\end{bmatrix} = \begin{bmatrix}
x_0 & y_0 \\
\vdots \\
x_n & y_n
\end{bmatrix} \begin{bmatrix}
\cos(b) & \sin(b) \\
-\sin(b) & \cos(b)
\end{bmatrix}
\]

Translation presents a somewhat more difficult problem. No 2 by 2 transformation matrix can be devised that will transform a group of points by a uniform displacement. An alternative representation of the translation is:

\[
x' = (x\cdot 1 + \text{changelog})
\]

\[
y' = (y\cdot 1 + \text{changelog})
\]

If we now represent all points in two-dimensional space with a 3 element vector of the form \([x\ y\ 1]\) for the point at \([x\ y]\), then the translation operation may be represented in matrix form as:

\[
\begin{bmatrix}
x'_0 & y'_0 & 1 \\
\vdots \\
x'_n & y'_n & 1
\end{bmatrix} = \begin{bmatrix}
x_0 & y_0 & 1 \\
\vdots \\
x_n & y_n & 1
\end{bmatrix} \begin{bmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
\text{changelog} & \text{changelog} & 1
\end{bmatrix}
\]

Note that a third (unnecessary) column is added to the translation matrix to make the results have the same dimensions as the input points.

The scaling matrix is now rewritten as:

\[
\begin{bmatrix}
s_x & 0 & 0 \\
0 & s_y & 0 \\
0 & 0 & 1
\end{bmatrix}
\]

The rotation matrix is now:

\[
\begin{bmatrix}
\cos(b) & \sin(b) & 0 \\
-\sin(b) & \cos(b) & 0 \\
0 & 0 & 1
\end{bmatrix}
\]

The use of an \(n+1\) element vector to represent a point in \(n\)-dimensional space is known as the use of homogeneous coordinates.

Now that a uniform representation, the 3 by 3 matrix, is available for transformations, two questions arise: (1) How can more complex transformations be implemented? (2) What effects are obtained from matrices which do not fit into the special structures generated for the basic transformations?

Most complex geometric operations may
be implemented as a sequence of basic operations. A few examples are examined next.

Rotation About an Arbitrary Point \([x_r, y_r, 1]\)

Since we know how to rotate about the origin, the point \(R\) and the object are first moved to the origin. The object is then rotated and the system moved back so that \(R\) is at its original location. A matrix representation of this procedure is shown in example 1. The point \(R\) will be unchanged by this sequence of transformations. Transformations are not generally commutative; i.e., the order of application of the transformations is fixed to achieve a particular combined result.

A similar statement is true for matrix multiplication:

\[
AB \neq BA \quad \text{in general.}
\]

But, matrix multiplication is associative. That is, if the order of the matrices is fixed, the order in which the individual multiplications is performed does not matter as far as the value of the result is concerned. Thus, in the example shown, we could combine the last three (transformation) matrices by multiplication to yield a single 3 by 3 matrix which represents the combined transformation. If more than three points are represented in the coordinate matrix, this technique will reduce the amount of computation necessary to calculate the result.

As a general comment, it is useful to decompose complex transformations into a series of basic transformations. Any transformation which preserves shape in the sense discussed above can be decomposed into a series of basic transformations represented as matrices. The product of these matrices will be the matrix representation of the complex transformation.

A general 3 by 3 matrix might be represented by:

\[
T_3 = \begin{bmatrix}
a & b & c \\
d & e & f \\
g & i & j
\end{bmatrix}
\]

Three special cases of this matrix have been presented that represent the basic transformations. While the products of such basic transformations can yield many of the cases of the general \(T_3\) matrix, it is useful to examine some other simple cases. The 3 by 3 identity matrix:

\[
I_3 = \begin{bmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1
\end{bmatrix}
\]

yields a result identical to the original set of points. This is a null transformation. The effect of setting elements \(a\) and \(e\) (referring to the general \(T_3\) matrix elements) equal to other values results in scaling. Setting elements \(g\) and \(i\) to nonzero values creates a translation. The process of setting element \(h\) to a nonzero value is shown in the following equations:

\[
x' = x \\
y' = bx + y
\]

The effect of this change on our figure "P" test pattern is shown in figure 9. This type of transformation is known as a \(y\) shear. Note how the "P" has been distorted in the \(y\) direction only by this operation.

![Figure 9: An example of \(y\) shear.](image-url)
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1. Introduction
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3. Which category do you fit into
4. Now - About the Hardware
5. Peripherals that plug in?
7. Helpful Suggestions before spending money
8. Addresses

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Similarly, setting element $d$ equal to a nonzero value causes an $x$ shear as shown in figure 10:

$$
x' = x + dy
$$
$$
y' = y
$$

If element $c$ or element $f$ is nonzero, or if element $i$ is not one, the result of the transformation is of the form:

$$
h = \begin{bmatrix} h_x & h_y & h \end{bmatrix}
$$

Here, $h_x$ and $h_y$ are considered to be bilateral (2 letter) symbols or variable names, not products of $h$ and $x$ or $y$. In this case, we divide each element of the vector by the last (or homogeneous) element. Thus, the coordinates of the point $(x,y)$ in two-space may be represented by an infinite number of homogeneous representations $[h_x \, h_y \, h]$. The process of dividing through by the homogeneous coordinate is known as homogeneous normalization (see table 1).

A particular problem arises when $h = 0$. In this case, division is undefined. An understanding of this situation is attained by letting $h$ go to zero.

The value of the normalized point in table 1 goes out along a line from the origin through the point $[a \, b]$; as $h$ approaches zero, the point goes to infinity. Thus the representation $[a \, b \, 0]$ defines a point at infinity along the line from the origin through $[a \, b]$. This representation of points at infinity is completely consistent with all previous discussion and definitions of transformations. The only truly undefined homogeneous value in two-dimensional space is $[0 \, 0 \, 0]$.

In transforming graphic elements, a problem may arise regarding the screen space boundaries. Portions of objects may fall outside the screen space after transformation. A similar situation may arise when objects are converted from problem space to screen space. It is therefore necessary to have a procedure for “clipping” the portions of objects outside the screen space so that the on-screen portion is accurately portrayed. The procedure described operates on the typical 4 sided rectangular screen.

The procedure operates on each line segment in the image and determines what portion, if any, lies in the screen space. The two endpoints of each line segment are classified as satisfying or not satisfying each of the four inequalities. Three specific

$$
x \geq x_g \quad x_e = \text{leftmost } x \text{ value}
$$
$$
x \leq x_r \quad x_r = \text{rightmost } x \text{ value}
$$
$$
y \geq y_b \quad y_b = \text{bottom } y \text{ value}
$$
$$
y \leq y_t \quad y_t = \text{top } y \text{ value}
$$

The procedure operates on each line segment in the image and determines what portion, if any, lies in the screen space. The two endpoints of each line segment are classified as satisfying or not satisfying each of the four inequalities. Three specific

```
Table 1: Homogeneous versus normalized representation of coordinates in two-dimensional space. The homogeneous representation of the coordinate pairs is a way of encoding the numbers in a general manner using the extra element $h$ in the matrix row.
The values of the coordinates are found by dividing $h$ into each coordinate (expressed here as variable names, i.e: "$hx$"; this does not mean "$h$ times $x$."). The results are shown in the right side of the table. The extra column in the homogeneous form of the matrix is needed to make the matrix conformable with other matrices used for translation operations.

<table>
<thead>
<tr>
<th>Homogeneous Representation</th>
<th>Normalized Representation</th>
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<tbody>
<tr>
<td>$hx$</td>
<td>$hy$</td>
</tr>
<tr>
<td>$a$</td>
<td>$b$</td>
</tr>
<tr>
<td>$a$</td>
<td>$b$</td>
</tr>
<tr>
<td>$a$</td>
<td>$b$</td>
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<tr>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>$a$</td>
<td>$b$</td>
</tr>
</tbody>
</table>
```

Editor's Note: Analogies Between Hardware and Software

Readers with a hardware background are no doubt familiar with the concept of limiting the range of a signal, or "clipping" it. This is often accomplished using a nonlinear device such as a diode. In this article, we find the same concept used in the software which transforms a list of points making up an image so that it will fit on a display screen. Here, instead of an analog signal, the "signal" being limited is the numerical range of the coordinates being computed. The implementation is different, but the concept is identical...CH
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Figure 11: Three different ways a line can appear. Line (a) is completely within the borders of the video screen. The lines labeled (b) are completely outside of the screen area, and the lines labeled (c) are partially within the screen area.

Figure 12a: Clipping. One way of calculating the cutoff point for a line is to use the traditional method of similar triangles. A disadvantage of this method is that it requires multiplication, a relatively time consuming operation on a computer.

cases may result from this endpoint coding:

(a) Both endpoints satisfy all inequalities.
(b) Both endpoints do not satisfy the same inequality.
(c) Neither of the above.

In case (a) the entire line lies within the screen space and is therefore displayed. In case (b) the entire line lies outside the screen space and is therefore not displayed. Case (c) requires further treatment.

The visible portion (if any) of each case (c) line is determined by cutting it with every inequality line (screen boundary) which is violated by either endpoint. Each inequality or clipping boundary not satisfied will cut the line into two portions, visible and invisible. The portion remaining, if any, will be the line segment visible in the screen space.

One approach to determining the point at which a line is cut by a boundary is derived from geometry (see figure 12a). The formulas for the left x boundary can be derived and the x_m, y_b and y_t results follow in similar fashion. By similar triangles:

\[
\frac{y_b - y_t}{x_c - x_0} = \frac{y_t - y_0}{x_1 - x_0}
\]

but

x_c = x_0

so

\[
y_c = y_0 + \frac{y_t - y_0}{x_1 - x_0} (x_c - x_0)
\]

The visible portion of the line is from \((x_0, y_0)\) to \((x_1, y_1)\).

An alternative approach, the clipping divider, is more suitable for microprocessor implementation since it uses neither multiplication nor division. It is actually a type of binary search. Using the example in figure 12b, we define \((x_m, y_m)\) as the midpoint of the line to be clipped. \((x_m, y_m)\) is calculated as follows:

\[
x_m = \frac{(x_0 + x_1)}{2} \text{ (add and 1 bit shift)}
\]
\[
y_m = \frac{(y_0 + y_1)}{2} \text{ (add and 1 bit shift)}
\]

If \(x_m = x_0\), then \(y_m\) is the y coordinate of the clipped endpoint and the process is completed. If \(x_m\) violates the inequality, then replace \((x_0, y_0)\) with \((x_m, y_m)\). Recalculate \((x_m, y_m)\). If the new \(x_m\) satisfies the inequality, then replace \((x_1, y_1)\) with \((x_m, y_m)\). In either of the last two cases, repeat the procedure with the new line, either \((x_m, y_m)\) to \((x_1, y_1)\) or \((x_0, y_0)\) to \((x_m, y_m)\). Because of the shifting used to calculate \((x_m, y_m)\), the process continues no
Figure 12b: Clipping. Another method of calculating the cutoff point of a line on the screen is to use a form of binary search. The method involves halving the line segment successively until the y value converges to the correct answer. This method only requires adding and shifting and is thus quicker to compute than the method of similar triangles.

more times than the number of bits in a word and the y coordinate will converge to the correct value.

This clipping process completes the set of basic operations necessary to operate on two-dimensional information to produce graphic output.

I hope readers will be encouraged to use these practical techniques in their experiments with computer graphics.

BIBLIOGRAPHY


This article presents an introduction to the use of APL for creating and manipulating graphic images. The paper carries the reader through the steps of interactive graphic design using APL and IBM 5100 APL Graphpak. The last section of this article, giving background information about APL and Graphpak, should be reviewed by the reader not familiar with either of these two topics. August 1977 BYTE is a useful source of APL information. For more detailed information about APL see the references listed at the end of this article.

The initial checkout of the examples was done using an IBM 5100 in stand-alone mode. The results were drawn on an IBM 5103 printer by modifying Graphpak to use output functions from the IBM 5100 Print Plot/APL Problem Solver Library. When the designs grew more complex, the IBM 5100 was connected to an IBM System 370/Model 168 and the code was executed there. The IBM System 370/Model 168 produced its output on a storage scope equipped with a hard copy unit.

Developing Repetitive Patterns

The first example follows a graphic designer through the development of a pleasing design for wrapping paper. Using a triangle as the basis for experimentation, the coordinates for a triangle centered at the origin are derived as shown in figure 1. A matrix, TRI, is then created to describe the triangle to the DRAW function:

```
TRI+4 30 0 0.1 0 (COS 30), (-SIN 30), 0, 0, 1
```

For this example, TRI looks like:

```
TRI
1 0 1
0 0.87 -0.5
0 -0.87 -0.5
0 0 1
```

To create patterns, translate the TRI matrix into the display window and draw it with the following APL function:

```
V DESIGN1
[1] TR+(COS 30),SIN 30
[2] DRAW TR TRANSLATE TRI
```

When executed on the IBM 5100, DESIGN1 gives a very small triangle of the defined dimensions. It will be necessary to increase the size of the triangle since it is presently too small to be used in a design. The function DESIGN2, shown in listing 1, is written to rotate the triangle 15 times and then translate the magnified pattern into the viewing area before drawing it.

Note in line 4 of listing 1 that the initialization of variable OUT is to be a matrix with no rows and three columns. This is done so that OUT has the proper shape when in line 6 it is concatenated with TR12 (which has three columns). When DESIGN2 is executed on the IBM 5100 the result is:

```
Figure 1: Equilateral triangle centered at the origin, the basic drawing block of our design.
```

```
Even though the original (magnified) triangle is within the viewing window, the complete pattern is not. Instead of moving the whole pattern into the display window, the rotating triangles can be shrunk so they stay within each other. The result of experimenting with different shrinking factors (actually magnifications of less than 1.0) is the APL.
```
function in listing 2. Execution of DESIGN3 results in:

To extend the design over a larger area of the plane, an upside-down version of the nested triangles is used. This upside-down design is obtained by rotating the original design 180° (π radians). The original and new patterns are then drawn side by side. This is accomplished by adding the following two lines at the end of program DESIGN3:

```plaintext
[13] OUT2+180 ROTATE OUT
[14] DRAW 15 MAGNIFY (2×TR) TRANSLATE OUT2
```

Execution of this program gives:

This pattern is used to cover the plane. To do so, variable OUT is made into a matrix containing the description of both the original set of nested triangles and the upside-down nested triangles by replacing lines 12 thru 14 with:

```plaintext
[12] OUT2+TR TRANSLATE 180 ROTATE OUT
[13] OUT-OUT,(1) OUT2
```

Then, to draw the N by M tilings, two nested loops are added at the end of the APL function. These loops are incorporated in lines 14 thru 19 of the function DESIGN7, which is shown in its entirety in listing 3.

Note that, in line 16 of listing 3, unnecessary parentheses were used to make the meaning clearer. However, not enough parentheses were added to make the meaning completely unambiguous to readers not familiar with APL. For example, the expression

```plaintext
TRX×(1+2×J)
```
could be written

```plaintext
TRX×(1+(2×J))
```

Listing 1: DESIGN2, an APL routine used to rotate the basic triangle and translate it into the viewing window. This operation is repeated 15 times. Note the use of variables in the header line of the function. This assures only local use of those variables.

```plaintext
9 DESIGN2:TR:ROT.REP;OUT;TRI2
[1] TR-1×COS 30),SIM 30
[2] ROT-0
[3] REP-15
[4] OUT-0 3 00
[6] OUT-OUT,(11 TRI2
[7] ROT-ROT+5
[8] MAG-MAG-0.87
[9] -LOOP IF O<REP-REP-1
[10] DRAW 15 MAGNIFY TR TRANSLATE OUT
```

Listing 2: DESIGN3, an APL routine which rotates and shrinks the basic triangle shape to keep the rotated triangles inside of the previously drawn triangle. This also keeps the rotated triangles within the viewing window.

```plaintext
9 DESIGN3:TR:MAG;ROT;REP;OUT;TRI2
[1] TR-1×COS 30),SIM 30
[2] MAG-1
[3] ROT-0
[5] OUT-0 3 00
[7] TRI2-2×MAG MAGNIFY TRI2
[8] OUT-OUT,(1) TRI2
[9] ROT-ROT+5
[10] MAG-MAG-0.87
[12] DRAW 15 MAGNIFY TR TRANSLATE OUT
```

Listing 3: APL program for drawing an N by M tiling of a surface. Each of the tiles consists of a right side up, rotated, magnified triangle series and an upside down, rotated, magnified triangle series.
Figure 2: Repetitive pattern resulting from the execution of DESIGN1. The prerequisite for accepting this design is aesthetic. The author felt that this was a pleasing arrangement of triangles.

Listing 4: A modification to listing 3, incorporated in line 16, shifts every other row of the pattern half a triangle to produce a more pleasing effect.

V N DESIGN8 M;TR;TRX;TRY;MAG;ROT;REP;OUT;TRI2;OUT2
[1]  TR=(TRX*COS 30),TRY=SIN 30
[2]  MAG=1
[3]  ROT=0
[4]  REP=15
[5]  OUT= 0 3 0
[7]  TRI2=MAG MAGNIFY TRI2
[8]  OUT=OUT,[1] TRI2
[9]  ROT=ROT+5
[10]  MAG=MAG*0.87
[12]  OUT2=TR TRANSLATE 180 ROTATE OUT
[14]  I=0
[15]  LPJ:J=0
[16]  LPJ:TR=(TRX=-1*(2*J+2)*J),I+TRY=(I+1)
[17]  DRAW 15 MAGNIFY TR TRANSLATE OUT
[18]  -LPJ IF N=J+1
[19]  -LPJ IF N=I+1

Listing 5: DESIGN9, an APL program that produces pictures such as the one shown in figure 4. The basic pattern has been shifted from row to row to produce a more pleasing design.

V N DESIGN9 M;TR;TRX;TRY;MAG;ROT;REP;OUT;TRI2;OUT2
[1]  TR=(TRX*COS 30),TRY=SIN 30
[2]  MAG=1
[3]  ROT=0
[4]  REP=15
[5]  OUT= 0 3 0
[7]  TRI2=MAG MAGNIFY TRI2
[8]  OUT=OUT,[1] TRI2
[9]  ROT=ROT+5
[10]  MAG=MAG*0.87
[11]  -LOOP IF 0<REP=REP
[12]  OUT2=OUT
[13]  OUT=OUT,[1] TR TRANSLATE OUT
[14]  I=0
[15]  LPJ:J=0
[16]  LPJ:TR=(TRX=-1*(2*J+2)*J),I+TRY=(I+1)
[17]  DRAW 15 MAGNIFY TR TRANSLATE OUT
[18]  -LPJ IF N=J+1
[19]  -LPJ IF N=I+1

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Circl e 306 on inquiry card.
Figure 3: Full size design created by shifting the pattern of figure 2. The rows have been shifted in relation to each other for appearance.
COSMAC VIP, the completely assembled, ready-to-operate RCA Video Interface Processor, opens up a whole new world of computer excitement. New challenges in graphics, games and control functions. Yet it's just $249.00.

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Figure 4: Pattern produced by flipping the triangles over, an example of how easy it is to produce a wide variety of patterns with only small modifications to a basic design program.
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Most features of ALTAIR* Extended BASIC are included PLUS these added features:
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Tarbell BASIC occupies 18K of RAM. Source is available on cassette, CP/M** Disk, and printout—all at reasonable prices. Price for TARBELL CASSETTE BASIC and complete documentation: $36.00.

CP/M Disk Operating System

The I/O section of this software has been modified to operate with the TARBELL Floppy Disk Interface in 24K bytes of memory. Five commands permit listing of directory, typing contents of an ASCII file, renaming a file, erasing a file from disk, and saving memory on disk. Fourteen programs are included which are invoked like commands. Six source files are included for transferring between TARBELL Cassette and disk, cold-start loading, Basic I/O system with drivers, and reformating crashed diskettes. Documentation includes a listing of BIOS and instructions to patch CBIOS for your system. Price is $100 on CP/M diskette with documentation. (CP/M is a product of Digital Research).

CP/M 1.4 Update Package

A TARBELL Update Package for those now using CP/M 1.3 is now available on diskette. The Update Package adds new commands and the ability to access four disk drives, as well as 2 new CP/M manuals, TARBELL CP/M User’s Guide and a new BIOS listing. Price: $50.00.

SPOOLER

This 8080 program will save many hours of computing time. It intercepts all output to the list device, spools the output to a high-speed disk file, and directs the spooled data to a low-speed printer during unused cycle time while the CPU waits for transfer of data to and from the console. System throughput is greatly increased with the aid of SPOOLER. Output is never lost due to insufficient memory allocation. Fully compatible with the CP/M file system, SPOOLER permits parallel processing without hardware interrupt, and with minimal impact on other processes. Price: $50.00. (Copyright KLH Systems.)

BASIC-E Compiler

Designed to work with CP/M Disk Operating System this software requires a total of 20K bytes of memory. Included are 26 compiler error messages and 23 run-time error messages. Disk files may be read, written or updated by using both sequential and random access. Included are blocked and unblocked files. Price for compiler and run-time monitor on diskette is $10.00. Manual is available separately for $5.00. (Public domain software by Gordon E. Eubanks, Jr.).

CBASIC Programming System

Upward compatible from BASIC-E, CBASIC is similar but expanded to include several business oriented facilities, allowing decimal computations to 14 digits of precision, data formatting and PRINT USING statements. Statements allow access to disk files and disk file maintenance. Strings of characters may be read from the console to permit correct input line format to be checked before reading data. General programming features include variable names up to 31 characters, optional line numbers, dynamic debugging tracers, and optional data output to printer. CBASIC on diskette and manual priced at $100. (Copyright Software Systems).

EMPL-an 8080 APL

Especially suited to educational applications, EMPL is an adaptation of APL, using the ASCII character set. This 8K version occupies the first 5376 bytes of memory and operates in two modes. The Execution Mode permits all instructions to be executed immediately. The Definition Mode permits the user to enter functions. EMPL on Tarbell Cassette with manual is $15.00. (Copyright 1977 Erik Mueller).

*ALTAIR is a trademark/tradename of MITS, Inc.
**CP/M is a trademark/tradename of Digital Research.

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Circle 360 on inquiry card.

BYTN September 1978 47
but in reality it needs no parentheses at all. Similarly, all the parentheses in

\[(J \cdot TRY + (J+1))\]

are unnecessary. The values for TRX and TRY are computed in line 1 of listing 3. Variables N and M have been placed in the header line of the new APL function, and now become part of the calling syntax for it. Trying out the new function by entering:

2 DESIGN 2

results in figure 2.

It appears that a better design can be obtained by shifting every other row by half a triangle. This is accomplished by making use of the residue primitive function,

1

where

\[211\]

results in 1 if I is odd, and 0 if I is even. This change is incorporated in line 16 of DESIGN8:

\[16\] LPJ:TRX=(TRX-\{(2+1)+(2+1)\},J+TRY+(J+1))

Also incorporated in line 16 is a shift of TRX units to the left for the entire drawing. The purpose of this shift is to avoid uncovered areas in the display window.

When DESIGN8 was tested, it was clear that an appropriate selection of colors would add significantly to the design. Without going into details, DESIGN8 was modified so that it would create three different, overlapped pictures. Each could then be printed in a different color. The resulting design is shown in figure 3.

Several other interesting designs can be obtained by slight modification of program DESIGN8. For example, instead of rotating the nested triangles to obtain an upside-down pattern, the sign of the values for the Y axis of the original set of embedded triangles can be reversed. This is equivalent to flipping the pattern over. The result is shown in figure 4. The APL function used to produce the design for figure 4 is shown in listing 5. Additional designs can be created by overlapping patterns.

Designing the Cover

The areas involving graphics in which APL and Graphpak can be used are virtually unlimited. This second example follows a graphic designer who would like to create a design using a customer's trademark. He is told that the design should portray the virtues of the product. For the example consider the logo which appears on the cover of BYTE magazine.
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"Natural Sounding Speech"

ANYTHING YOU WANT TO SAY"

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PARAMETER EDITOR
SOFTWARE
(STD. WITH CT-1)

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Circle 46 on inquiry card.
The designer first creates a matrix called BYTE which contains the data required to draw the basic logo. This matrix was created by manually digitizing the logo. The logo can then be drawn, as in figure 5, by entering the command:

```
DRAW BYTE
```

The intention is to create the design at a 90° angle. This way the logo can be moved along the X side of the display window (which is longer than the Y side). By reducing the size of the logo as it is moved, the customer’s request for creating a feeling of “never-endingness” can be met. (Note: in figure 5, and in some of the figures that follow, the outline of the display window has been added to aid in understanding the discussion.)

One way to move an object while simultaneously shrinking it is to displace it from the origin while using the MAGNIFY function to reduce the values for the X and Y axes. To move the logo diagonally across

```
[1] LOGO=180 ROTATE BYTE
[2] LOGO= 100 76 TRANSLATE LOGO
[3] I=0
[4] MAG=1
[5] TR= 13 0
[6] MAGSIN= 4.2 10
[7] LOOP:FIG+MAG MAGNIFY LOGO
[8] DRAW TR TRANSLATE FIG
[9] MAG=MAGX0.74
[10] MAGSIN=0.95*MAGSIN
[12] MODULATE+MODULATE=MAGSIN
[13] TR=TR+MODULATE
[14] LOOP IF 50>I+1
```

Listing 7: Modification to the program. The addition of a sine function to the program changes the shrinking line of logos into a shrinking spiral.

```
V PICTURE1:J:M;LINE:MAG;ROT:M2:TR
[1] I=0
[2] N+ 0 3 p0
[3] LINE+ 2 3 p 1 0 24 0 21 ~12
[4] MAG=1
[5] ROT=0
[7] MAG=MAGX0.98
[8] ROT=ROT+3
[9] +LP IF 200x2=I+1
[10] Z=N
[12] Z=Z,[1] N
[13] TR= -(-1/z[2]),(-1/z[3])
[14] DRAW TR TRANSLATE Z
```

Listing 8: PICTURE1, an APL routine for producing a design using a series of shrinking and rotating straight lines. This design, when added to the pattern already created, results in the front cover of this month’s BYTE.
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- Cycle Time: 480ns
- Wait States Generated: None
- Maximum DMA Rate: 1 Mhz

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Description of Graphpak

This section covers common APL terminology, some Graphpak conventions, and a description of APL functions which are used in the paper. The discussion is, by necessity, oversimplified. It provides only enough information to understand the paper. For more complete information on APL and Graphpak, consult the references.

In APL, programs are called functions. Primitive functions are those which are part of the APL system, and are generally written as just one symbol or two overstruck symbols. One of the exceptions is the sine function which is written:

\[ \sin \]

For example:

\[ \sin \]

A scalar is a single number, for example: 3.1415. In general, a vector consists of several numbers, for example: 3 5 2.54. This definition of scalar and vector suffices as far as this paper is concerned. However, the exact definition of a scalar is "an object with 0 dimensions," and for a vector, "an object of 1 dimension." In fact, a vector can contain one or more elements or be empty.

This paper is limited to the "Drawing Component" and parts of the "Descriptive Geometry Component" of Graphpak. For a description of the other components of Graphpak refer to the *IBM 5100 APL Graphpak, Program Description/Operations Manual*.

The descriptive geometry functions of Graphpak are designed to perform geometric transformations on descriptions of three-dimensional objects, and to display projections of the transformed objects on the display window. The Graphpak display window is normally a rectangle in the XY plane with the coordinate origin at the left bottom corner. In this paper the width (X direction) of the window is 100 units and the height (Y direction) is 76 units. Even though only two-dimensional objects are used here, the transformations take place in three-dimensional space. The Z dimension is assumed to come perpendicularly out of the page.

To describe a series of lines to be drawn by Graphpak, a matrix with three columns is used. The first column is a binary vector. A 1 tells the program to go to the (X,Y) position indicated by columns 2 and 3 without drawing a line. A 0 means go to the indicated (X,Y) position while drawing a straight line. The function DRAW takes as its argument a matrix that describes a series of lines and draws them. For example, if the variable BOX contains:

\[
\begin{bmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1 \\
0 & 0 & 0
\end{bmatrix}
\]

then DRAW BOX gives:

![Drawing output]

The desired values can be placed in BOX by entering

\[
BOX+5 3p1 0 0 0 10 0 10 0 0 10 0 0 0
\]

where

\[
p
\]

(rho) is the reshape (primitive) function. The

<table>
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<tr>
<th>Table 1: Geometric transformation functions used in this article.</th>
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<tr>
<td><strong>2-D TRANSLATE X</strong></td>
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<td><strong>Z</strong></td>
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<tr>
<td><strong>2-A ROTATE X</strong></td>
</tr>
<tr>
<td><strong>Z</strong></td>
</tr>
<tr>
<td><strong>2-P MAGNIFY X</strong></td>
</tr>
</tbody>
</table>
left argument of rho specifies the shape to be given to the right argument. If two matrices describing two objects are to be put together, they can be *concatenated* in the first dimension using

\[ \text{cat} \]

For example, using the *TRANSLATE* function (whose description follows):

```
BOX2-10 10 TRANSLATE BOX
DRAW BOX.11 BOX2
```
gives:

![Diagram of Box]

The geometric transformation functions used in this article are summarized in table 1. In the descriptions given in table 1, *TRANSLATE* and *MAGNIFY* are described as operating only in the X and Y directions. This is a simplification for the purpose of the paper. They are capable of performing three-dimensional manipulations.

In addition to the Graphpak functions, the following APL functions are used here:

```
V Z+A IF E
[1] Z+B/A
V
V Z+/-X
[1] Z+10X+O+1+3+6
V
V Z+C/.X
[1] Z+20X+O+7+13+6
V
```

The *IF* function is used to make the APL code used in the paper clearer to readers not familiar with APL. The *SIN* and *COS* functions are also used to make the code clearer to readers not familiar with APL; but in addition, they take an argument expressed in degrees (the APL primitive trigonometric functions assume their arguments to be expressed in radians).

The display window after rotating it 180° requires:

```
DRAW 100 76 TRANSLATE 180 ROTATE BYTE
```

Incorporating the above into the APL function LOGOS1 (listing 6) to test the hypothesis produces figure 6.

Next the designer tries to make a spiral by adding an X and Y translation to the shrinking logo using a sine function (in APL, sine is designated by:

```
10 followed by an argument in radians) which decreases in magnitude. After some experimentation the function in listing 7 was found.

Note the shift by 13 units in statement 5 of listing 6. This was necessary because the translation using sines (statements 10 thru 15) carried the design into negative X values. Execution of LOGOS2 results in the pattern of figure 7.

There is still some empty space which could be filled with some type of interesting design. After experimenting with rotating a shrinking line, the function in listing 7 was developed.

Lines 10, 11, and 12 of PICTURE1 create a symmetrical picture by reflecting the figure generated about the Y axis. Line 13 determines the minimum translation required to get the figure within the display window. Execution of PICTURE1 results in figure 8. After rotating and making smaller drawings of the design created by PICTURE2, they are placed in the design created with logos. The finished product can be seen on the cover of this issue of BYTE.

In summary, we have followed a graphic designer using APL and Graphpak through two problems and have seen the ease with which these software tools can be used for creating and manipulating graphic images.

### REFERENCES

1. APL Language, IBM form GC26-3847.

2. IBM 5100 APL Graphpak, Program Description/Operations Manual, IBM form SB30-0850.

3. IBM 5100 APL Graphpak Application Brochure, IBM form GB30-0850.


A good practice in APL is to localize variables needed only within a function by placing them in the header line of the function. In this way all the local variables will disappear from the workspace when the function completes execution...RGAC.
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UCLA Computer Club 20th Anniversary Party

The UCLA Computer Club will be holding a 20th anniversary party and reunion in October 1978. The tentative date is October 14. The intent is to have club members from every era (WDPAC, Computing Facility, ARPA, CCN) present so that everybody has old friends to talk to. “Resisters” are also welcome.

If you are a former UCLA Computer Club member, or you knew members who would like to see them again, please send your name, address, and phone number to Joe Katz, Computer Club, 3514 Boelter Hall, UCLA, Los Angeles CA 90024. A complete list will be sent to everyone who responds whether they decide to attend or not.

A Worm Invades an Apple . . . (or, Computer versus Computer)

Rumor has it that the underground technology of defrauding the telephone monopoly took a dubious step forward with the notorious “Capt Crunch’s” latest escapade. Word is that the Federal prosecutors in the trial will introduce an Apple II computer in evidence as the instrument of the crime.

More Notes from the Rumor Mill: Heath Software

According to highly reliable sources, Heath is offering a slightly scaled down version of the DEC RT11 operating system (version 2C) as part of their H27 dual full-size floppy disk kit. The software package, called the HT11, is being bundled with the floppy kit for a total price of approximately $1700, and will be available in October 1978. The RT11 operating system (well-known in minicomputer circles) plus the RX01 dual floppy disk system will cost about $7000 if purchased from Digital Equipment Corporation (DEC).

The only difference between the RT11 and HT11 packages is that the latter does not have the super macro-assembler or the foreground-background monitor (plus some additional utilities). It does have DEC's standard BASIC, however. Heath will also be offering DEC's standard FORTRAN package for $100.

Finally, there is a possibility that Heath will be offering a UCSD Pascal package for $200 in the near future.

Computerland's Second Birthday

Computerland, currently the largest computer store chain, reports to us that they will be celebrating their second birthday on Saturday, September 23. Customers and friends are invited to local outlets of the chain. In our opinion, as patrons of the Nashua NH store, Computerland has to be one of the best planned and managed retail operations in this business. We trust that the Nashua store is typical of the other stores in this chain, which number over 40. . . .

Capacitor Value

In Robin Mosley's article “A Low Cost Light Wand Amplifier” (May 1978 BYTE, page 92), the value of capacitor C1 should be approximately 47 mF. Anyone using the optional peak detector to measure the amplifier output should allow for the forward drop of the two detector diodes and adjust the circuit for a DC output voltage from the detector of approximately 0.5 V.

Meetings in Bedford MA

In July 1978 BYTE, we mentioned in the Clubs and Newsletters section that the New England Computer Society meets monthly at the Mitre Corp Cafe­teria, Bedford MA. However, we neglected to mention that they meet the first Wednesday of each month at 7 PM. (Members of the BYTE editorial staff are usually in attendance at these meetings.)
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<td>of 80 characters per line</td>
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<tr>
<td>110 or 300 Baud switch selectable</td>
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<tr>
<td>Full keyboard</td>
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<td>RS 232C Serial Interface standard</td>
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| RS 232C Serial Interface       | 260.00  |

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| 12 IPS paper slew           |  |
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A “Tiny” Pascal Compiler

Part 1: The P-Code Interpreter

Roughly speaking, a compiler is a program that translates the statements of a high level language (such as Pascal or FORTRAN) into a semantically equivalent program in some machine recognizable form (such as machine or assembly code). The former is usually referred to as the source program while the latter is called the object program. An interpreter, on the other hand, reads in the source program and starts execution directly, without producing an object program.

There is little doubt that compilers and interpreters are a necessary part of any computer system. The reason most personal computer systems do not have high level language compilers is not that there is no need for them. Compilers, being inherently more complex than interpreters, require more effort to write and more computer memory to run. The main advantage of a compiler over an interpreter is the relative speed. A compiled program typically runs an order of magnitude faster than an equivalent program executed interpretively. In fairness, it must be also pointed out that interpreters are usually easier to use, and more suitable for an interactive environment.

This series of articles is an attempt to describe how a compiler for a subset of Pascal was implemented on an 8080 computer system. It is not our intention to go into details for the reasons for the choice of the language. Pascal is widely recognized as superior to many other languages. For an overview of the language, readers are referred to August 1978 BYTE. The publication, Pascal: User Manual and Report, by Kathleen Jensen and Niklaus Wirth (Springer-Verlag, 1974) should also be consulted as the authoritative source book on the language in its original form.

This is not, of course, the first Pascal compiler ever written for microcomputers. However, instead of waiting for a Pascal compiler to be written for our particular processor, we decided to undertake the project ourselves. In this way, we can add or subtract features from the original Pascal to suit our needs and system capabilities, so that it can be easily integrated with other system software developed so far.

2 Stage Compiler

The compiler is divided into two stages: a p-compiler and a translator. Instead of having the compiler generate machine code directly, it generates code for a hypothetical machine, called the p-machine. These codes, called p-codes, are then converted into the target machine codes by the translator. Dividing the task of a compiler into two stages offers several advantages. The compiler can be written abstractly, without committing oneself to a particular machine and worrying about details of code generation and optimization. Such a compiler is said to be portable, meaning that it can be used on other computer systems with minimal start up effort. It is only at the last stage of code translation from the p-codes to actual machine codes that we have to commit ourselves to a particular machine.

Another advantage this method offers is greater flexibility when writing the compiler. The compiler and the translator can be coded and debugged separately. The flexibility of such a compiler was apparent to us as we started to introduce more and more Pascal features into our original minimal subset. Seldom was it necessary for us to introduce new p-codes other than those originally specified.

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Figure 1: Memory overlay structure of the modules of the compiler. The North Star DOS and BASIC start at hexadecimal 2000 and take up approximately 14 K bytes of memory. The p-compiler is the largest BASIC program of the system; in its compressed form (void of all comments and blanks) it occupies 14 K bytes. It reads Pascal source programs created by the editor from disk files, and generates relocatable p-codes directly in memory. We use hexadecimal 0000 to 19FF for p-codes and find it adequate for Pascal source programs under about 300 lines in length. The smaller translator (9 K bytes) produces 8080 codes directly filled into memory. The origin of the codes can be specified. The run-time routines (which total 1 K bytes of memory) are needed only when the translated 8080 codes are being executed. The interpreter is written in Pascal, compiled and translated. The BASIC interpreter is no longer needed when it or any other Pascal program is being run.

the compiler into two stages: most small computers do not have enough memory space to store the complete compiler. After the p-codes are generated, the p-compiler is no longer needed, and can be overlaid with the translator. Therefore the compiler and the translator can share the same memory locations.

Actually we also use two other utility programs: a text editor and a p-code interpreter. The editor is used to prepare the Pascal source programs. The interpreter is used to interpret the p-codes produced by the p-compiler. This provides another alternative for running the Pascal programs. Because it is equipped with various debugging aids, such as setting up breakpoints in p-codes and outputting values for variables, debugging can be easily done. Only after a program is verified to be correct is the translator loaded, and 8080 code produced. This allows easy development of the Pascal programs without sacrificing efficiency at run time. Figure 1 shows the overlay structure for the various modules of the compiler. Figure 2 shows the logical flow during a program development.

In this part of the series on our project, we will describe the general plan. The Pascal subset is defined using syntax diagrams. A description of the p-machine and its codes are also given. We will discuss the p-compiler, translator and runtime routines in the following parts.

Bootstrap Compiler

How does one introduce a new language into a computer system with limited computer resources? By computer resources we mean not only the computer hardware like memory and peripherals, but also software tools. We have learned from experience not to attempt programs with the complexity of a compiler in machine or assembly language. This left us with BASIC. Although it is not the most desirable language to write a compiler with, it turned out to be adequate. Some careful thought is needed, of course, to handle recursive subroutine calls from BASIC, a feature central to our compiler writing.

The alternative to BASIC is to go to a commercial computer and write the whole or part of the compiler in an appropriate
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Language. The finished product (or part of it) can then be transferred to the smaller computer. This is, however, a luxury most of us cannot afford.

Of course, the compiler written in BASIC.
would be very inefficient and slow. But this actually would not matter, since it would only be used as a bootstrap compiler. The concept of bootstrapping should be familiar to most personal computer owners. We usually use it when initially starting up our computers. After turning on the power, a bootstrap loader is first loaded into the computer (either manually or through the use of read-only memory). This bootstrap loader is then used to load the loader, which in turn loads the monitor into memory. The bootstrap loader is a smaller version of the loader; it is just big enough to load the main loader and not adequate to be a general purpose loader.

The same idea can be applied to compiler writing. A compiler for a small subset of a language is first written. This subset should be big enough so that a compiler for a bigger subset of the same language can be written in it. The larger compiler is then written and compiled, using the first compiler. Next, a compiler for a still bigger subset of the same language can then be written and compiled, using the second compiler, and so on until a compiler for the complete language is produced. In actual practice, no more than three stages are used. It does not matter if the first compiler is very inefficient. The idea is to get a working, albeit primitive and inefficient, compiler with minimum starting effort.

Pascal Subset Syntax

The syntax of Pascal can be described precisely by using a notation usually called Backus-Naur form (BNF). This is a collection of rules for the grammar of the language. Instead of dealing with Backus-Naur form directly, we use an equivalent but more understandable notation: the syntax diagrams. Figure 3 describes the syntax of the Pascal subset we are interested in.

In the syntax diagram, the square boxes are called nonterminal symbols, while the ovals are called terminal symbols. Terminal symbols are the basic building units of the language and require no further expansion. In our case, the names that represent the terminals are also their textual representations in the language. The nonterminal symbols in the syntax diagrams can be expanded using rules specified in another syntax diagram, and there is a syntax diagram for each nonterminal symbol in the syntax diagram. A branch in the diagram represents options allowable by the grammar. When all nonterminal symbols are eliminated by expansion in this fashion, we would have a valid program. We start off a compilation with the nonterminal program. Looking at

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There are two mountain peaks of evolution on planet earth: on the land, homo sapiens—human beings; in the sea, cetaceans—whales, dolphins, and porpoises.
the syntax diagram we see that a program is a block followed by a period (.) . Looking at the syntax diagram for block, we notice that it can have an optional declaration part followed by the main body which begins with the string begin, followed by any number of the nonterminal symbols, statement, separated by semicolons (;), and then the string end. The statement block can be further expanded by the syntax diagram for statement, and so on.

The reason we go through the details here is because it is important to precisely describe the features we want to include in our language before starting to write the compiler. It is the first step towards writing the compiler. These syntax diagrams will later become flowcharts for the syntax analyzer of the compiler.

Readers familiar with Pascal will no doubt notice several important features missing from our subset. There is no GOTO statement. The only data type we have is integer and integer array of one dimension. Also missing from the subset is the structured data type, pointer type, user defined type, and file type. A less obvious omission is passing the parameter of a procedure by address; the parameters are passed by value only. Aside from the fact that these features are difficult to implement, they are not indispensable in our bootstrap process. Of course, features like user defined type and structured type are some of the unique features of Pascal, and should not be omitted in the long run. But we feel that they can be added later.

We have also included some trivial but nevertheless useful enhancements to the language, which we hope do not deviate from the standard too much. One is the addition of the optional clause else to the case statement which provides an exit path if the value of the variable does not fall into any of the case labels. Another is the inclusion of format controls in the read and write statements. Following an expression in a write statement, a pound sign, #, indicates numeric form and a percent sign, %, indicates hexadecimal format. If there is no
format control, a character whose ASCII code equals the expression is output. Also a hexadecimal constant is prefixed by %. This allows processing of hexadecimal numbers without conversion by the user.

To allow interfacing Pascal programs with assembly programs, a facility is provided to read or write a byte from or to absolute memory locations. The array `mem` is a reserved array name that is used to do this.

**Figure 3, continued: Elementary constructs for Pascal subset. Hexinteger is usually not defined in Pascal but is used here so that actual memory locations can be easily manipulated.**
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Continued from page 17

List price was about 100,000 Yen, which means it will sell discount for about 80,000+ Yen. Like the PC1200 (already on sale in the US) the PC1300 seems to use Sharp's own 4 bit 1 chip 64 pin flatpack microprocessor, with 2 K bytes of read only memory on chip. Sharp earlier released the EL-6000, a child's arithmetic practice calculator.

Mitsubishi had a 4 bit microprocessor (MS6840) with on-chip 8 bit analog to digital converter (5% accuracy claimed). Panafacom had the C15, a BASIC language 16 bit machine with touch keyboard, video display, 15 ips Philips cassette, but no printer (it will be an option). Its BASIC includes graphics, matrices (option) and strings, cassette tape utilities and commands for its IEC bus option. (The 16 bit chip is not new.) 700,000 Yen with 16 K memory, 16 K expansion will be option. They also have a do it yourself kit, the "L-kit," with color graphics.

NEC's BASIC station, a do it yourself 8080 board with hexadecimal keyboard, plus separate alphanumeric keyboard, video (TV) and cassette interfaces, runs a 4 K Tiny BASIC with peek, poke and graphic commands. It costs about 200,000 Yen. Their Level 2 BASIC, with strings, subscripts and arrays, and standard (sin, log, etc) math routines plus up to 18 character alphanumeric names, is due in July. (Level 1 and Level 2 are not compatible, maybe they plan to use their new 16 bit chip µPD768B).

A small company, INPEX, has an 8085 kit with large keyboard for machine language programming; the keys correspond to opcodes Cost is about 80,000 Yen.

RARE CHASSIS?

I want to thank Dan Fylstra for his article in the May 1978 BYTE, page 22, "Convert Your TV Set to a Video Monitor." It was clearly written and well illustrated. I was about to purchase a TRS-80 from Radio Shack and his article convinced me that I should buy a Hitachi TV and a Pickles and Trout converter. Thus I would have both a computer display and a portable TV.

But alas! I live in Dallas TX. And in Dallas TX not one store that I called that handles Hitachi TVs has the models with the SX chassis! What's more, the Hitachi district offices listed in the yellow pages have closed and I was given a phone number in Atlanta GA! Now I could have called long distance to Atlanta, but I wasn't interested in ordering a TV from Atlanta or Tokyo. Changes are the model has been discontinued anyway.

Pickles and Trout had a good idea, but does a 12 inch TV exist that is not AC/DC? A TV chassis with a transformer type power supply does allow an easier hookup than does a "hot" chassis. But if one is not generally available, there is a market for an AC/DC converter that is as specific as the Pickles and Trout unit.

As for me, I ordered the TRS-80 complete with display cathode ray tube (CRT). After all, they toss in the cassette recorder if you buy the whole thing! But I do hope the SX chassis does exist elsewhere so others can use Mr Fylstra's article.

Clarence J Stinson
9138 Chimney Corner
Dallas TX 75243

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I would be so grateful for some information concerning satellite receiving stations using computers for data storage and video display. (I am interested in observing cloud cover.)

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Thank you for any help you can provide.

Brad Sloicum
236-D E Red Oak Dr
Sunnyvale CA 94086

We've not published such an article to date, but it would make an excellent topic for the homebrewer. For output one could use one of the new electrostatic printers with graphic capability which retail for about $800 -- or simply display the images on your video outputs with bit map graphics, possibly using colors where available. . . .CH

DREAMING . . .

I am 12½ years old, and plan to get a computer system up and running in the near future. The mainframe I have selected is the Heathkit H11, incorporating the DEC LS1-11 processor. I chose this mainframe because of the processor employed and the low price, only $1295. This price is offset by a few disadvantages, such as its bus, with only six slots, and the fact that its price is only relatively low (at this time I have only $724.08). But, like any other problems in this world, these can be solved. I can fix the bus problem by simply buying an expansion interface from DEC, but this makes the second problem worse yet. And, unlike other problems, buying more of what you need (money) simply defeats itself in its purpose. So I just have to save. (And save, and save. . . .)

However, by the time I finally do
have the money for it, something bigger and better (and slightly more expensive) will have appeared on the horizon. I will probably continue at this pace until I am a millionaire at 21. At this point, of course, I will buy a large computer from DEC or some other company and charge people to timeshare on it. Only problem is, I don't know where I am going to get the million dollars in the first place. It's nice dreaming, though, and my dreaming is going to get me somewhere in this world. (I hope so, anyway!)

Norman Aleks
659 Driftwood Ln
San Dimas CA 91773

A sound philosophy... . .

GOTCHA!

On page 154 of the May 1978 BYTE you described the new products by Lucas-Adams Labs Unltd. The address of this manufacturer was not printed. Could you please let me know the address so that I can enquire about the products?

K L Yap
2217 7th Av NW
Calgary, Alberta
CANADA T2N 0Z9

Unfortunately, Lucas-Adams Labs Unltd did not supply us with their address. However, we thought that our readers would be interested in their (totally fictional) product line so we published the press release. I am sure that with perseverance, their address may be found in the combined annals of April fools jokes for this year...RGAC

KUDOS FOR KENT

It seems E W Kent ("The Brains of Men and Machines," January through April 1978 BYTE) has violated Higher Education Law #1: Never explain complex issues in understandable terms. Kent must be aware of the ramifications of violating this most basic principle of higher education, the most significant being the release of usable information to lay people who might understand it and use it.

Kent has produced a classic, and has given the computer scientist a game plan for the creation of the first real cybernetic system. He has also given the electrical engineering community a new direction: If you are an engineer, think neuron and cortex instead of bus and processor. While you are doing this (in conjunction with people like E W Kent), the computer scientist will be developing algorithms and operating systems to support your hardware. We have a long road ahead, but thanks to Kent we're on our way.

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Some Words About Program Structure

Microprocessor programming, at this point in time, is a black art. Once you have learned the basic instruction set, you’re on your own. Some people get the knack of this mysterious task fairly quickly, and some do not. Those who do well seem to have developed some sort of system for going about it. The point is that an organized, systematic approach is required if there is any hope for continued programming success. The purpose of this article is to describe to you one such method which has become very popular with programmers of all types, using all kinds of computers from micros to the giants.

Concept

What we’re looking for is simplicity in the writing of programs. This is usually achieved if the program can be reduced to a collection of basic components which fit together in very well-defined ways. This is the concept behind structured programming.

Any program can be considered to have only two basic building blocks. One is the process block shown in figure 1. It simply performs some defined function, or process. It might represent a simple function requiring only a few, maybe only one, instructions in the program, or a much larger function requiring many instructions. Whatever it does, it has one input and one output.

The second basic block is the decision block shown in figure 2. This elementary capability of any computer is that which gives it all its power and flexibility. It is the ability to alter the path taken by the program based upon the value of some parameter or condition which can be tested by certain instruction types. For example, two numbers can be compared and a test for equality used to decide which of two program paths will be taken as a result.

These two fundamental building blocks will now be used in the construction of a set of basic program structures with which any other program can be built. The three general structures are called sequence, if-then-else and loop. Variations of these will be examined, as well as combinations which can be used to build more complex functions.

Figure 1: The process block is the “black box” of programming: it is entered by a single input path, does some arbitrary operations upon data, and is exited by a single output path. The “arbitrary operations” can be as simple as one step in an arithmetic calculation, or as complex as a compilation of a program – it all depends on the point of view taken.

Figure 2: The decision block is a simpler concept than the process block, in the sense that the amount of computation required rarely approaches the generality of an “arbitrary process.” A decision block has one input and, depending upon a binary condition, takes one of two output paths. In this figure, the names “true,” “then” and “yes” denote one possible path; the names “false,” “else” and “no” describe the other possible path. In programming languages, the “then” or “else” terminology for the two paths is frequently built into the language design; the other terms are frequently seen in flowchart representations of programs.
Remember: In structured programming, everything is a process block, with one input path and one output path.

Editor's Note:
BYTE Flowchart Flow Conventions

As an "ideal" standard, flowcharts in BYTE use a direction of flow convention as follows:

Default flow: Vertical flow is from the top of a diagram toward the bottom, and horizontal flow is from the left of a diagram towards the right, unless explicit flow is used. Thus:

Explicit flow: Vertical flow upward or horizontal flow leftward in a drawing is shown with an explicit arrow at the end of the flow path, thus:

Merged flow: When two or three paths of flow merge, the two or three inputs to the joint path have arrows noted:

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Basic Structures

The simplest of the program structures, shown in figure 3, is the sequence structure, which is composed of one or more process blocks strung together serially. Like the process block from which it is built, the sequence structure has only one input path and one output path. In fact, you will soon see that one of the rules that we want all structures to conform to is that they have a single input path and output path. Furthermore, an entire program, which can be represented by one large process block, should also conform to this rule.

The next structure is the if-then-else structure, shown in figure 4. It consists of a decision block and two process blocks. Only one of the process blocks is executed for any single pass through the structure. The result of the test or comparison represented by the decision block determines which process block is chosen. Notice that regardless of which path is taken there is one common exit path from the if-then-else structure. This is required to maintain our single exit philosophy.

An if-then-else structure does exactly what it says: if a condition is true, then take a specified action, else take a specified alternate action. However, there are times when only one action is required in only one of the paths. No action is necessary in the other path. In an actual flow diagram, this is of course shown by drawing a flow line in place of one or the other process block of the if-then-else structure since the most trivial process is simply going to the next process without doing anything. Note however that only one of the process blocks can be made up of this simplest case of "do nothing" since if both process blocks were eliminated from the if-then-else structure, the net effect would be to "do nothing" all the time whether or not the condition was true or false.

The if part of an if-then-else structure is simply any program instruction which can perform a test and take one of two paths depending upon the outcome. In an assembly language, this is usually a conditional jump or a branch instruction based upon the outcome of some comparison, arithmetic operation or other operation which affects processor status flags used in such branches and jumps. The branching instruction specifies the destination address of the beginning of one path. Whether it is the then or the else leg is arbitrarily defined, and the next sequential instruction is assumed to begin the opposite path.

Some higher level languages like BASIC have ready-made if-then-else instructions. BASIC has IF and THEN; ELSE is implied. The following shows how an if-then-else would look in BASIC:

```
1 IF X=Y THEN 10
   11 . . . . . .
   12 . . . . . . } FALSE PART
   13 . . . . . .
10  GOTO 15
   15 . . . . . . } TRUE PART
15 END
```

In this example, the else code immediately follows the IF instruction. The GOTO 15 ends the else path and causes the program to branch to the common exit point at line 15. The then path starts at line 10 and ends at line 15. BASIC is considered to be an "unstructured" language because of the need for an explicit GOTO following
Blaise Pascal

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The "false part" of an IF-THEN-ELSE construction.

If you use assembly language in your programming, and your assembler has a macroinstruction capability, then you can write your own if-then-else macros. It is beyond the scope of this article to describe how this is done, but it isn't very difficult.

If you use assembly language and don't have facilities for writing macros, then you can simulate the function of the macroassembler in order to gain the advantages of structured programming. Simply sit down and write yourself a set of standard if-then-else structures. Take the five or six most common decision types (equal, not equal, zero, greater than, etc) and write skeleton programs for each. Leave blanks for the actual condition to be tested, and leave space for the actual code which will perform the then and else functions. Later, when you need an if-then-else while writing a program, you can draw upon your set of prewritten structures. Not only does this eliminate your having to invent similar program sequences over and over again, but it also prevents many bugs and greatly eases the effort you have to put into program writing.

The last basic structure is the loop, which provides a means of repeating a sequence of instructions until some stop condition is found to exist. There are two kinds of loop structures: do-until and do-while.

A do-until structure, shown in figure 5, performs the function in the process block at least once. After that, a test is done to determine if the condition for stopping the process looping has been found true. As long as the condition is not true, the looping continues. When it becomes true the looping ends and the exit path is taken. This type of structure can be used, for example, when you need to search a table of values, looking for a particular value. If you know that the table will always contain a matching entry, the program routine need not be more complicated by logic to detect end-of-table before a matching value is found. Notice that the first table entry is always examined before the decision is made to continue (this is because the ending condition decision is based upon the value of that entry).

The second type of loop is the do-while, shown in figure 6. The difference between this and the do-until structure is that the test is done before the process block is executed. In many cases there is not a lot of significance to this difference because both types of structures can do the same jobs.

In specific situations you will find that one form will usually be better suited or more convenient than the other. The primary difference to remember is that the do-until form always executes the process block at least once whether or not the until condition is true, and that the do-while may not execute the process at all if the while condition is false at the time of the first test. Experience will best teach you which to use in the various situations.

A variation of the loop structures of either form might be considered, the endless loop or do-forever. This form of loop occurs when the while or until condition is never changed to allow execution of the output...
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path of the structure. Intentional endless loops are occasionally used, as in the low level programming trick of hanging up execution in a tight loop to flag errors, or the quite legitimate endless loops which form the outer level of control of a typical executive or monitor program. But for most programming purposes, an endless loop is a bug or error in the program.

An Example

Now using the basic structures, we can construct a program of any size and complexity by combining and nesting in any manner as long as some fundamental rules are adhered to:

- The program as a process should have only one input path and one output path.
- Structures within the program can be nested but each structure must be totally contained within the structure in which it is being nested (this will be illustrated later).
- There should be no branching unless it is part of a structure (for example, the GOTOs required in languages like BASIC).
- Refrain from attempting to optimize the program by violating the above rules. There is a right time for this later.

Before we look at an example of structuring a program, let’s first look at how nesting of basic structures works. Figure 7 shows a flowchart of a program which,
overall, could be represented by a single
if-then-else. But when it is looked at in more
detail, the else leg contains another if-then-
else as part of the instruction sequence
there; the else leg of that structure con-
tains yet another if-then-else. The heavy
outlines show that each of the nested struc-
tures are totally enclosed by their parent
structures; there is no overlap. A BASIC-
like program to perform the function shown
in figure 9 appears as listing 1. Again, I
use outlines to illustrate that each structure
is embedded in its entirety within another
higher level structure. Notice that I have
used indentation of lines to increase the
readability of the program. Each separate
structure should be at a different level of
indentation than its parent.

```
00 FOREVER
ENDLESS LOOP

THIS ACTS LIKE THE PROCESS BLOCK IN DO-FOREVER

KEY ON
YES (THEN)

NO (ELSE)

THIS ACTS LIKE FALSE
PROCESS BLOCK OF IF-THEN-ELSE

KEY IN LOCK
NO (ELSE)

YES [THEN]
TRUE PROCESS

NO (ELSE)
FALSE PROCESS

DOOR OPEN
YES (THEN)
TRUE PROCESS

SUBROUTINE
SOUND THE BUZZER

NO (ELSE)
NON-NULL PROCESS

LIGHTS ON
YES (THEN)
TRUE PROCESS

SUBROUTINE
SOUND THE BUZZER

NO (ELSE)

TIME DELAY

CONTINUE

32 END
```

Listeing 1: A BASIC-like program equivalent for the
flowchart of figure 7. The
lines in the picture em-
phasize the structured pro-
gramming formalism.

Figure 9: Taking the algorithm of figure 8 and casting it into a standardized, structured pro-
gramming form eliminates all GOTO operations in languages with a complete if-then-else
structure, and in languages like BASIC, reduces use of GOTO operations to standardized struc-
tures. In this flowchart, we've positioned all the blocks to emphasize the nesting of structure.
One of the primary reasons for the emphasis on structured programming is one of communica-
tions of ideas to other programmers (or the originating programmer at a later date). The claim
is made that a flowchart like this one, and its equivalent representation in listing 2, provide a
standardized way of communicating algorithms which makes the listing or chart easier to under-
stand and read.
Let’s look now at an example of a simple program and show how a structured version might differ from an unstructured version.

The program is one which might be part of a future automobile computer control system using a microprocessor. Its purpose is to trigger a buzzer if the ignition key is left in the lock when the left front door is opened, or if the headlights are left on when the key is not in the lock. A delay is performed before conditions are checked again.

The flowchart in figure 8 shows how we might have drawn it without attempting to apply any of the principles of structured programming. Now, look at figure 9 which shows the structured version. Both forms of the program do the same function, but the structured form is clearly more straightforward and easier to write code from.

Basically, a number of things happened to the flowchart when it was structured. First, all the branches (or GOTOs) became forward branches except those in loop structures. This allows for reading the chart from top to bottom in an orderly way. Secondly, each decision block and process block has been put into a proper structure and nested totally within its parent structure. Thirdly, every structure regardless of its place in the overall program has only one input and one output.

One thing has happened that might appear to be a little strange to you. The sequence structure which performs the buzzer function appears twice now, where it only appeared once before. This is necessary in order to keep the structure clean. Remember, you cannot simply branch into the other buzzer block because those two structures would then overlap. The inefficiency implied by the double appearance of that block might bother you, but it will probably turn out that the block will be written as a subroutine and the only inefficiency will be an extra call instruction.

Listing 2 is a BASIC-like program for the structured flowchart. (Here “BASIC-like” means using the syntax of BASIC but allowing variable names to be many characters in length for purposes of illustrating their meaning.) I have not attempted to make the program complete and have taken some liberties in order to illustrate my points.

A few words of explanation are in order. First, the instructions at lines 3, 4 and 5 represent a do-until structure which is used to implement a delay by simply incrementing a counter (X) until it reaches a large value. The name BUZZ represents the line number of a subroutine (not shown) which activates an electronic buzzer in the car’s dash.

Now is the time to go back and look at the program to make it more efficient in its operation or in the amount of memory required. This should be done only if it is absolutely necessary. If it is necessary, try to maintain the structuring to the extent that it doesn’t destroy the clarity of the program or increase its complexity. In our example program, notice that there are three CONTINUE instructions at lines 13, 14 and 15 leading to a GOTO at line 16. The speed of the routine can be improved and the memory requirements can be reduced by eliminating the CONTINUEs and changing any instruction which references any of them to go to line 16. Alternatively, you could change each of those references to go directly to line 1 although you would be seriously interfering with the intent of structuring.

In conclusion, I invite you to try the techniques described in this article when you write your next program. If you have done it any other way before, it takes a little getting used to, but I think you will ultimately agree that it has a lot to offer. Hopefully, you will see the benefits in the form of less time spent getting your program designed, written and debugged. In short, I believe that it can help make programming even more enjoyable.

---

**Listing 2: A BASIC-like application program for activating a buzzer of an automobile given several conditions. A subroutine BUZZ is indicated (by a call with the keyword GOSUB) to actually sound a noise during the loop. In this BASIC-like representation, several liberties with syntax have been taken.**

```
1 LET X = 0
2 IF KEY = ON THEN 7
3 LET X = X + 1
4 IF X > 5000 THEN 5
5 GOTO 3
6 GOTO 13
7 IF KEY = INLOCK THEN 11
8 IF LIGHT = ON THEN 10
9 GOSUB BUZZ
10 GOTO 13
11 IF DOOR = OPEN THEN 13
12 GOSUB BUZZ
13 CONTINUE
14 GOTO 1
```
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**SIMULATION**, the second book of the series, are articles dealing with various aspects of specific types of simulation. Both theoretical and practical applications are included. Particularly stressed is simulation of motion, including wave motion and flying objects. The realm of artificial intelligence is explored, along with simulating robot motion with the microcomputer. Finally, tips on how to simulate electronic circuits on the computer are detailed.

**NUMBERS IN THEORY AND PRACTICE**. This book includes information of immense value to both the novice and the experienced personal computerist. The mechanics of the binary system are discussed, including division and multiplication, as well as the places to look for numerical error in programs. Floating point numbers, what they are and how to use them, are covered. There are also sections on numerical methods (functions, approximations, statistics), Boolean math, and several different approaches on how to obtain random numbers.

**BITS AND PIECES**. The articles collected for this book are mostly unrelated and do not neatly fit into the topics of the previous three books, but still have a lot to do with programming techniques. Areas such as multiprogramming and interactive computing with the personal computer are discussed, as well as stacks, sorting, Polish notation, and program optimization. This is by far the most general book of the series.
RA6800ML: AN M6800 RELOCATABLE MACRO ASSEMBLER is a two-pass assembler for the Motorola 6800 microprocessor. It is designed to run on a minimum system of 16 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (such as Motorola MIKBUG read-only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

The Assembler can produce a program listing, a sorted Symbol Table listing and relocatable object code. The object code is loaded and linked with other assembled modules using the Linking Loader LINK68. (Refer to PAPERBYTE™ publication LINK68: AN M6800 LINKING LOADER for details.)

There is a complete description of the 6800 Assembly language and its components, including outlines of the instruction and address formats, pseudo instructions and macro facilities. Each major routine of the Assembler is described in detail, complete with flow charts and a cross reference showing all calling and called-by routines, pointers, flags, and temporary variables.

In addition, details on interfacing and using the Assembler, error messages generated by the Assembler, the Assembler and sample IO driver source code listings, and PAPERBYTE™ bar code representation of the Assembler’s relocatable object file are all included.

This book provides the necessary background for coding programs in the 6800 assembly language, and for understanding the innermost operations of the Assembler.

ISBN 0-931718-10-4
Author: Jack E. Hemenway
Pages: approx. 120
Price: $25.00
Publication: Fall 1978

LINK68: AN M6800 LINKING LOADER is a one-pass linking loader which allows separately translated relocatable object modules to be loaded and linked together to form a single executable load module, and to relocate modules in memory. It produces a load map and a load module in Motorola MIKBUG loader format. The linking Loader requires 2 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (for instance, Motorola MIKBUG read-only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

It was the express purpose of the authors of this book to provide everything necessary for the user to easily learn about the system. In addition to the source code and PAPERBYTE™ bar code listings, there is a detailed description of the major routines of the Linking Loader, including flow charts. While implementing the system, the user has an opportunity to learn about the nature of linking loader design as well as simply acquiring a useful software tool.

ISBN 0-931718-09-0
Authors: Robert D. Grappel & Jack E. Hemenway
Pages: 48
Price: $8.00
Publication: Summer 1978

TRACER: A 6800 DEBUGGING PROGRAM is for the programmer looking for good debugging software. TRACER features single step execution using dynamic breakpoints, register examination and modification, and memory examination and modification. This book includes a reprint of "Jack and the Machine Debug" (from the December 1977 issue of BYTE magazine), Tracer program notes, complete assembly and source program listing in 6800 assembly language, object program listing, and machine readable PAPERBYTE™ bar codes for the object code.

ISBN 0-931718-02-3
Authors: Robert D. Grappel & Jack E. Hemenway
Pages: 24
Price: $6.00
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TINY ASSEMBLER 6800, Version 3.1 is an enhancement of Jack Emmerichs' successful Tiny Assembler. The original version (3.0) was described first in the April and May 1977 issues of BYTE magazine, and later in the PAPERBYTE™ book TINY ASSEMBLER 6800 Version 3.0.

In September 1977, BYTE magazine published an article entitled, "Expanding The Tiny Assembler". This provided a detailed description of the enhancements incorporated into Version 3.1, such as the addition of a "begin" statement, a "virtual symbol table", and a larger subset of the Motorola 6800 assembly language.

All the above articles, plus an updated version of the user's guide, the source, object and PAPERBYTE™ bar code formats of both Version 3.0 and 3.1 make this book the most complete documentation possible for Jack Emmerichs' Tiny Assembler.

SUPERWUMPUS is an exciting computer game incorporating the original structure of the WUMPUS game along with added features to make it even more fascinating. The original game was described in the book What To Do After You Hit Return, published by the People's Computer Company. Programmed in both 6800 assembly language and BASIC, SUPERWUMPUS is not only addictively fun, but also provides a splendid tutorial on setting up unusual data structures (the tunnel and cave system of SUPERWUMPUS forms a dodecahedron). This is a PAPERBYTE™ book.

MONDEB: AN ADVANCED M6800 MONITOR-DEBBUGGER has all the general features of Motorola’s MIKBUG monitor as well as numerous other capabilities. Ease of use was a prime design consideration. The other goal was to achieve minimum memory requirements while retaining maximum versatility. The result is an extremely versatile program. The size of the entire MONDEB is less than 3 K.

Some of the command capabilities of MONDEB include displaying and setting the contents of registers, setting interrupts for debugging, testing a programmable memory range for bad memory locations, changing the display and input base of numbers, displaying the contents of memory, searching for a specified string, copying a range of bytes from one location in memory to another, and defining the location to which control will transfer upon receipt of an interrupt. This is a PAPERBYTE™ book.

BAR CODE LOADER. The purpose of this pamphlet is to present the decoding algorithm which was designed by Ken Budnick of Micro-Scan Associates at the request of BYTE Publications, Inc., for the PAPERBYTE™ bar code representation of executable code. The text of this pamphlet was written by Ken, and contains the general algorithm description in flow chart form plus detailed assemblies of program code for 6800, 6502 and 8080 processors. Individuals with computers based on these processors can use the software directly. Individuals with other processors can use the provided functional specifications and detail examples to create equivalent programs.
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Part 3: The Torres Chess Automaton

19th Century Developments

The automata of the 18th century were in fact sequence controllers possessing both digital and analog stored programs whose readouts were mechanisms that imitated human and animal actions (computers of a sort). During the next century they inspired a flood of automata, the best of which von Helmholtz described in his 1847 book, *Über die Erhaltung der Kraft*, as being equal in achievement to the best in any other branch of science. Derek Price's book, *Automata in History*, includes material from von Helmholtz (see bibliographical notes).

In the 19th century men were starting to contemplate how mechanisms might be able to improve the human state. Charles Babbage had this notion in mind when in December 1837, precisely 99 years after Vaucanson's marvelous demonstration (see July 1978 BYTE "Antique Mechanical Computers, Part 1") he wrote the first sentence of *On the Mathematical Powers of the Calculating Engine*: "The object of the present volume is to show the degree of assistance which mathematical science is capable of receiving from mechanism." An obscure accountant of Manchester, Percy Ludgate, working without knowledge of Babbage, expressed the same thought when he wrote in 1909 the first sentence of *On a Proposed Analytical Engine*: "I propose to give in this paper a short account of the result of about six years work, undertaken by me with the object of designing machinery capable of performing calculations, however intricate or laborious, without the immediate guidance of the human intellect."

I think we may be too near to our machines to see the revolution residing in what these men said. Before Babbage and Ludgate, machines amplified or assisted or enabled the physical actions of humans. But now these men were suggesting that a machine could assist in or substitute for a mental activity of a human. Machines would enter into the realm of the human brain. It was a breathtaking idea, but not an easy one to put into effect. Babbage's two machines were never fairly begun, nor was Ludgate's. (In Babbage's case the reason was not that nineteenth century machine technology was unequal to the task, but rather because he kept changing his concepts and never produced any completed working drawings as he continuously visualized bigger and bigger machines. For him, the end was never in sight, and he left off working at a point where the machine would have been the size of a basketball court and some yards high. His son completed the "Mill" (ALU) with its printhead long after Babbage's death, in 1906. See Randell in the bibliographical notes for a photo of the Mill and a reproduction of the printout of multiples from 1 to 23 of \( \pi \) in 28 significant figures.)

Torrés and the Incredible Chess Playing Automaton

Gifted chess players have been known to play several concurrent games, making moves without hesitation from board 1 to board \( n \), then back to board 1. The best chess playing programs of today can't do that with any degree of success against most skilled players. But the remarkable fact is that in 1911 a machine was invented that automatically played a particular endgame of chess (King and Rook versus King) against a human opponent, and detected any false moves!

Leonardo Torrés was the inventor, and his machine was displayed in the Mechanical Laboratory at the Sorbonne early in 1914. Photo 1, taken from a 1915 issue of the *Scientific American Supplement*, shows the
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Photo 1: Front (a) and back (b) views of the 1911 chess playing automaton invented by Leonardo Torres. The unit played a particular chess endgame (King and Rook versus King) only and could force a win. The chessboard is shown in the lower right of center in photo 1a. Horizontal and vertical arms moved the pieces (which were actually electrical jacks) from square to square, and the logic circuitry consisted of battery driven relays arranged in a logical tree structure (see figure 3). Photos courtesy of Scientific American (Supplement 80, Number 2079, November 1915).

Torres was a true amateur who did his work because he loved it.

machine. It seems to have been powered by the array of weights atop the console, but it used electricity (almost surely from a battery) in its logic system, which consisted of commutators and intricate switchgear. Indeed, most of the face of the console is covered with relays and switches with their linkages and wiring, but one can make out the vertical chessboard, sans chess pieces, in the lower right quadrant of the face. It is about 8 to 10 inches (20 to 25 cm) wide and has holes in the center of each of the 64 squares that are really plug holes into which fitted the carved chess pieces (actually jacks on their lower ends used to make electrical contact). Sequential switches of two sorts are visible on the apron in the foreground, and the signalling lamps consist of a 3 lamp cluster in the middle with another single lamp on the right.

The machine in operation must have been an amazing sight, for its visible action was automatic. The sliding arms (poorly shown in the photo; located both above and to the left of the board) would grasp the chosen White piece, unplug it, transfer it to a new computed location, and reinsert the piece into the board. Then it waited for Black's next move. This is a degree of automation I don't recall seeing since I last gazed at a Linotype, and in 1914 it must have been an awesome spectacle. To be sure, Black always was checkmated, even with the first move, since White (the machine) had too much strength. If Black made a false move, the machine would sense it and light a signal lamp, then wait until the piece was moved to a legitimate square. Three false moves in the course of a game would "jam" the machine, which would not continue play until a reset switch was closed and pieces were properly placed. Possibly the pieces could be placed anywhere on the chessboard upon initiating a game; accounts do not make this clear. At any rate, the algorithm is quite general and directs the White King a square at a time, and the White Rook a row or column at a time inexorably toward the Black King until he is hemmed in.

In 1922 an improved version was displayed. Photographs and a description may be found in Chapuis (see bibliographical notes). This more modern machine had a horizontal chessboard grooved to accom-
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modate wires that sensed the location of a piece, and a complex clutch and gear system within the tabletop accomplished White's moves, via magnets. It was all powered by a few small electric motors, and a phonograph record pronounced the words "échec et mat" when Black was checkmated. Figure 1 shows a chart of the action, drawn from the Scientific American article. [According to David Levy in Chess and Computers, the Torres machine is still in good working order and can be seen in the museum at the Polytechnic Institute in Madrid, SPAIN. . . . CM]

"It is necessary that the automata imitate living actions according to their inputs, and adapt their conduct to changing circumstances."

One of his first interests was mechanical analog computing devices, perhaps before 1900. He was familiar with Babbage's publications. In a paper dated 1920 he outlined an electromechanical calculating machine he exhibited in France. The machine consisted of a modified typewriter and several boxes of apparatus, connected only by a bundle of wires, all mounted on a table for display. (A picture of the machine is in Randell’s book; see the bibliography.) The operator types in the numbers desired to be manipulated together with the sign of the operation to be performed, and after a few moments an answer is followed by the result is typed out. This is a 4 function machine that can deal with perhaps six or seven digits. This was in 1920, mind you! He revealed the
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"Construction of mechanisms which play the role of sense organs is not difficult in theory."

Theoretical underpinning for his calculating apparatus in general terms in 1914, in the *Essais sur l'automatique*. (In 1914, *automatique* was a new word, translatable as automation or as automatics.)

Torres' essay is so lucid and fresh that today, 64 years after publication, it still casts much illumination on the human and machine interface. After describing a first type of automaton, a machine designed to mimic the movements of a living creature, he describes a second type of automaton (Torres' own italics), "...those that imitate, not the simple gestures, but the thoughtful actions of a man, and which can sometimes replace him." He gives examples: "...the self-propelled torpedo, which knows how to maneuver in order to arrive at its target, the balance which weighs coins so as to choose the ones which are of legal weight." He speaks of the need for a "...special chapter of the theory of machines which would be called *Automatics*" and of the need to investigate "means for constructing automata endowed with a pattern of behavior of greater or lesser complexity." "These automata will have sense organs, i.e. thermometers, magnetic compass, manometers, etc." together with "limbs, i.e. machines or mechanisms capable of executing the operations which they are instructed to do." And they will need power sources. "Moreover, it is essential, being the chief objective of *Automatics*, that the automata be capable of *discernment*; that they can at each moment take account of the information they receive, or even information they have received beforehand, in controlling the required operation." "It is necessary that the automata imitate living beings in regulating their actions according to their inputs, and adapt their conduct to changing circumstances."

After noting that construction of mechanisms which play the role of sense organs is not difficult in theory, and that new apparatus to achieve this measuring (sensing) function is invented every day (what cannot be measured today will be measured tomorrow or shortly), he adds that the same may be said of devices to effect the automaton's work. No one can point to a limit in the inventing of machines to perform functions. But, "It is not the same when one asks whether it is possible to construct an automaton which, in order to decide on its manner of working, *ponders* on the circumstances which surround it. The estimate is, I believe, that this may be done only in some very simple cases... it is thought possible to automate the mechanical operations performed without thinking by a workman, but that those requiring the exercise of mental faculties will never be executed mechanically." "I shall try to show in this article, from a purely theoretical point of view, that it is always possible to build an automaton whose actions depend on a greater or lesser number of circumstances, according to rules which one can impose arbitrarily during its construction."

In reference to this quote, Torres described a simple digital device, but with the novelty that it displays a worked out form of conditional branching: ahead of its time, like so much of Torres' writings and work.

In his writings, Torres selected his words so carefully that it is possible to argue his distinction between "to discern," a process of input which he welcomes and illustrates as measurements; and "to ponder," a verb he seems to reserve for human thought, where more has to be taken into account than just the information of the moment or information previously received. And what is that "more"? I suggest that only people who know mechanics very well can appreciate fully the chasm between their creations and those of life (i.e. between organic information and mechanical information). Randell observes, and I heartily agree, that "In all this work [Torres] was deliberately exploi-
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BIBLIOGRAPHICAL NOTES

1. The information in these articles has been synthesized from various sources I have encountered in reading about the history of computers, several histories of which make mention of Vaucanson in the sentence that directly precedes the one about Babbage. I found no literature explaining Vaucanson's creations until I came across:


Here an astonishing and catholic variety of automated devices are described and illustrated, most of them trivial, such as pictures with clockwork-driven, moving figures. It is maddening that Chapuis' *Automata* treats the great mechanical computers of the past with little care. Chapuis and Droz were in a unique position because they read French, the language of most of the original docu-
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ments. They had pursued the field of automata so long (Chapuis & Edouard Gelis published *Le Monde des Automates* in 1928, as well as making a film about automata in 1945) that their fame on the continent would have enabled them to study the machines minutely. They meticulously reconstructed the dates of inception, untangled the inventors of automata, and deduced the fate of the machines. Their myriad illustrations are unsurpassable.

2. You can read a translation of Vaucanson’s own description of his automata in:


which is currently in print. This book mentions and illustrates the Eureka poetry composing machine, a violin playing device, and quotes a newspaper account of one or two astonishing automats (unless they are fabricated) such as a life-size mannequin that plays violin sonatas under keyboard control. There is little else of interest regarding stored programs. Lots of fun, though.

3. A most valuable survey which speaks of a great many mechanisms and machines from the historical viewpoint, but describes them hardly at all is:


which is worthwhile for the long perspective it offers on mechanics, and for the sense of continuity it conveys regarding human endeavor. You begin to learn that the world has always been filled with restless, thoughtful, imaginative and inventive people.

4. It is fun to read a splendidly researched volume like:


which is still in print and describes a nearly century long hoax (for which Vaucanson had unwittingly cleared the path), as well as Maelzel’s actual mechanical achievements that blossomed into an industry by 1900.

5. For me the doyen of computer historians is:


where the developments that preceded and led up to the digital computer are spelled out event by event. As if Randell’s crystalline commentary were not enough, he includes original papers (some in lucid translation) by Babbage, an incredibly clever man, and just about everybody who did anything useful in the development of computers, such as Aiken, Hopper (the only woman in the book), Eckert, Von Neumann, Goldstine, and Mauchly. They are included here, along with Leonardo Torres. Many machines are also included, such as the Zuse relay computer of wartime Germany, the Bell Labs relay computer, Altanasoff’s Iowa State computer with its novel capacitor storage system, and of course, ENIAC and EDSAC, those feeble giants.

6. The following article makes fascinating reading:

Anonymous, “Torres and His RemarkableAutomatic Devices (He Would Substitute Machinery for the Human Mind.),” *Scientific American Supplement 80*, number 2079, 6 November 1915.

7. Torres’ machine is also described in:

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Let Your Fingers Do the Talking

Scanner Applications

In "Let Your Fingers Do the Talking — Add a Noncontact Touch Scanner to Your Video Display" (August 1978 BYTE, page 156), I detailed the hardware design of a noncontact touch scanner which sits over a conventional video screen. This system, though lower in resolution, allows a fingertip to simulate the function of a light pen and with proper programming can become as important a peripheral as the common ASCII keyboard.

Quick Hardware Review

The scanner consists of 32 pairs of infrared light emitting diode transmitters and photo transistor receivers arranged around the perimeter of a picture frame. There are 16 pairs on the X axis and 16 pairs on the Y axis. The hardware logic sequentially activates the 32 pairs, first in the X direction (horizontal) then in the Y direction (vertical). If a physical obstruction is placed in the plane of the scan, one X and one Y beam are interrupted. The corresponding X and Y beam addresses are stored when this happens. Since there are 16 pairs per axis, each coordinate can be represented by a 4 bit code and both the X and Y addresses can be packed into one data byte.

The end result of the hardware logic is a very simple scanner to computer interface. The scanner output is one 8 bit byte containing the 4 bit X and 4 bit Y addresses. The only other signals are a little something often referred to as hand shaking. A data ready line is set to a high level output when the scanner has sensed an obstruction.

This data ready signal can be tied to a parallel input port and scanned as I have done, used as a control line on a peripheral interface circuit, or used directly to generate a processor interrupt. If the touch panel is to be exercised in BASIC, the first method will prove to be easiest. The latter method, normally used with a machine language program rather than BASIC, will be the most efficient from a memory utilization standpoint.

I continue to use BASIC wherever the interface data processing speed allows it. In this way I can write illustrative program examples which are not tied to a particular processor. Of course, the speed advantages of machine language may be useful if your programs using the touch panel have a lot to do; so feel free to strike out on your own using these BASIC programs as a model.

Whatever the software method utilized to recognize the data ready bit, the program action must be the same. After the data ready bit goes high, the data byte is stored and the data ready is reset by momentarily pulsing the ready reset line low. In BASIC, the easiest way to do this is to tie the ready reset line to one bit on a parallel output port (it need only be a strobe rather than a latched output) and then sequentially execute two OUT instructions. The 10 ms pulsewidth I get on my machine is the result of the time it takes for BASIC to respond. The program examples presented in the listings use the following port allocations (in decimal):

Photo 1: The basic information returned from the touch panel is a coordinate pair for one of 256 possible finger sized locations on the video display's face. Here, using the program in listing 3, the displayed coordinates 10 and 9 correspond to the point just touched on the screen.
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ARTIST AND COMPUTER edited by Ruth Leavitt
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PROJECTS IN SIGHT, SOUND, & SENSATION by Mitchell Waite
- Dedicated “to all space cowboys.” Detailed theory and practice of seven fascinating amateur electronics projects, along with a complete and detailed appendix on how to make PC boards. The projects included in this book are: The Syntheshape, an art generator that can be used to generate innumerable complex and beautiful patterns on the screen of an oscilloscope. An electronic music box that will play over 3000 possible melodies when the lid is lifted. A way to control muscle tension explained in chapter 4. A muscle wave bio-feedback monitor can be used to achieve deep relaxation. The laser-light show transfers light into fascinating patterns in a darkened room. Other projects include a Kirlian camera, a digital ESF machine, and neon-light randomizer. $5.25.

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200 \( D_2 = D \) AND 15

195 REM \( D_1 \) IS THE X COORDINATE

180 \( O = \text{INP}(16) : \text{REM \( \text{SCANNER IS ATTACHED TO PORT} \ 16 \) }

170 \text{REM' .. READDATA ..}'

160 IF \( T \neq 1 \) THEN GOTO 140 : \text{REM TEST TO SEE IF DATA READY IS SET}

140 \( T = \text{INP}(2) \) : \text{REM THE DATA READY SIGNAL IS BIT 0 OF PORT 2}

130 \text{REM ** TESTDATAREADY • • •}

150 \( T = T \) AND 1 : \text{REM MASK ALL BUT BIT 0}

120 \text{OUT} 16,0 : \text{OUT} 16,255 : \text{REM THIS WILL GIVE A SHORT RESET PULSE TO}

210 RETURN : \text{REM RETURN IS ONLY NECESSARY IF CALLED AS A}

205 REM \( D_2 \) IS THEY COORDINATE

190 \( \text{D}_1 = (\text{DAN D} 240)/16 : \text{REM MASK AND SHIFT RIGHT 4 BITS} \)

180 \text{REM THIS IS THE ONLY SOFTWARE NECESSARY TO EXERCISE THE}

140 \text{SCANNER}

130 \text{PORT 16}

120 \text{X, Y Coordinate}

110 \text{Input Port 16}

100 \text{Variable \( D_1 \) would contain the X coordinate and \( D_2 \) would contain the Y value. Each call}

97 to this subroutine results in return ing to

88 the main program with the X, Y address of

80 a single touched point. To obtain ten touch

76 inputs would require calling this routine ten

70 times.

66 The simplest program utilizing the scanner

62 would be one which sensitizes the entire

57 screen to act as one giant push button. Such

54 a program is similar to a press any key op­

51 eration on a keyboard.

51 The program in listing 2 prints “MY

48 SCREEN ITCHES!! PLEASE SCRATCH

46 IT!” on the video screen, waits for some­

40 one to touch any place on the screen and

38 then responds with the message in line 30.

36 Notice that we did not use the coordinate

33 information from the scanner because we

29 only needed to take advantage of the fact

25 that the subroutine returns only if data is

21 ready.

17 Test the Coordinate System

13 If one builds the touch panel, the first

13 program written should be one that illus­

11 trates the coordinate system dynamically,

11 such as the program in listing 3. (All

10 BASIC programs in this article are written

10 in Micro Com 8 K Zapple BASIC.)

9 After printing an opening comment on

8 the video screen, the program calls the

7 scanner subroutine as before. This time

6 when it returns, it prints out the X and Y

5 coordinate which was touched as shown in

4 photo 1. The rest of the program is a repeat

2 of this basic cycle with one exception. The

2 values of \( D_1 \) and \( D_2 \) are both compared to

1 15 after each scan. Should you point at

1 coordinate position (15,15) the program

0 ends.

Converting Position to Function

So far we have displayed only the raw

output of the scanner and have not used it in its true application. Telling you that you

are pointing to location (4,2) illustrates that

the touch panel functions, but does no use-
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Photo 2: Here is a picture of an experiment which was backed up by a fairly long BASIC program: using the screen as the input device for a simulation of an ordinary 4 function calculator. The imagination of the user, to use a well-worn cliche, is the only limitation upon trying experiments with special purpose keyboards and interactive sequences on the screen. Use of the video display behind the touch panel area makes easily altered software the determining factor—rather than physical tools in the workshop.

Listing 4: Illustration of a BASIC program which divides the screen into four sectors and performs a function dependent on which sector is touched by the user.

```
100 S=USR("CG")
110 PRINT"NAME" ADDRESS'
120 FOR L=1 TO 12
130 PRINT
140 NEXT L
150 PRINT"PHONE VITAL CHARACTERISTIC '
160 GOSUB 1000
170 IF D1<7 THEN GOTO 300 ELSE GOTO 200
200 REM THIS ROUTINE DECIDES IF YOU ARE PRINTING TO
202 REM SECTOR 1 OR 2
210 IF D2<7 THEN PRINT"UNLISTED NUMBER" I GOTO 2000
220 PRINT"BRENDA (THE LITTLE WOMAN) CIACCIA"
230 GOTO 2000
250 REM MAIN ROUTINE DECIDES IF YOU ARE PRINTING TO
252 REM SECTOR 3 OR 4
254 IF D2>7 THEN PRINT"SCOTTISH TERRIER --14 LEGGED AURAL ALARM" I GOTO 2000
256 PRINT"MK 562 VALENTINBURG+CHR. 06819"
260 GOTO 2000
290 REM
300 REM SCANNER SUBROUTINE
300 OUT 16,0 OUT 16,255
310 T=INP(23)
320 D=0 AND 1
330 IF T=0 THEN GOTO 1010
340 D=0 AND 15
350 D=0 AND 15
360 D=0 AND 15
370 RETURN
390 FOR W=1 TO 2000
400 NEXT W
```

Figure 1: Physical arrangement of sectors on the screen as used by program in listing 4.
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Specify Verbatim
Listing 5: Keyboard simulation program.

```
100 REM THIS PROGRAM DISPLAYS A KEYBOARD ON THE CRT SCREEN
110 REM IT ILLUSTRATES DATA ENTRY WITHOUT A PHYSICAL KEYBOARD
120 REM JUST POINT AT THE LETTERS AND IT WILL "TYPE" YOUR MESSAGE
120 PRINT A, B, C, D, E, F, G, H
130 PRINT
140 PRINT
150 PRINT A, J, K, L, M, N, O, P
160 PRINT
180 PRINT
190 PRINT A, SPACE*
200 GOSUB 3000
210 GOSUB 1000
220 IF D2=12 THEN PRINT CHR$(13)+CHR$(10)+GOTO 245
230 IF D2=10 THEN PRINT CHR$(13)+CHR$(10)+GOTO 246
240 IF D2=8 THEN PRINT CHR$(13)+CHR$(10)+GOTO 248
250 IF D2=6 THEN PRINT CHR$(13)+CHR$(10)+GOTO 246
260 IF D0=0 THEN PRINT CHR$(13)+CHR$(10)+GOTO 245
270 IF D1=15 THEN PRINT CHR$(13)+CHR$(10)+GOTO 245
280 IF D0=15 THEN PRINT CHR$(13)+CHR$(10)+GOTO 245
290 PRINT CLEAR SCREEN
300 PRINT "TRY A RETRY EXERCISE----TOUCH SCREEN"
310 GOSUB 1000
320 GOTO 200
330 OUT 16,0: OUT 16,255: REM LINES 1000-1070 READ THE SCANNER DATA
340 IF T=INF(2) THEN RETURN
350 T=T+1
360 IF T>3 THEN GOTO 1010
370 OUT-INF(16)
380 D1+D AND 24016
390 D2=INF(15)
400 RETURN
410 FOR A=0 TO 500: REM THIS IS A SHORT DELAY
420 NEXT A
430 RETURN
```

Listing 6: Method for scanning two input devices simultaneously on a Digital Group 2-80 system.

```
100 REM THIS PROGRAM DISPLAYS A KEYBOARD ON THE CRT SCREEN
110 REM IT ILLUSTRATES DATA ENTRY WITHOUT A PHYSICAL KEYBOARD
120 REM JUST POINT AT THE LETTERS AND IT WILL "TYPE" YOUR MESSAGE
120 PRINT A, B, C, D, E, F, G, H
130 PRINT
140 PRINT
150 PRINT A, J, K, L, M, N, O, P
160 PRINT
180 PRINT
190 PRINT A, SPACE*
200 GOSUB 3000
210 GOSUB 1000
220 IF D2=12 THEN PRINT CHR$(13)+CHR$(10)+GOTO 245
230 IF D2=10 THEN PRINT CHR$(13)+CHR$(10)+GOTO 246
240 IF D2=8 THEN PRINT CHR$(13)+CHR$(10)+GOTO 248
250 IF D2=6 THEN PRINT CHR$(13)+CHR$(10)+GOTO 246
260 IF D0=0 THEN PRINTCHR$(13)+CHR$(10)+GOTO 245
270 IF D1=15 THEN PRINTCHR$(13)+CHR$(10)+GOTO 245
280 IF D0=15 THEN PRINTCHR$(13)+CHR$(10)+GOTO 245
290 PRINT CLEAR SCREEN
300 PRINT "TRY A RETRY EXERCISE----TOUCH SCREEN"
310 GOSUB 1000
320 GOTO 200
330 OUT 16,0: OUT 16,255: REM LINES 1000-1070 READ THE SCANNER DATA
340 IF T=INF(2) THEN RETURN
350 T=T+1
360 IF T>3 THEN GOTO 1010
370 OUT-INF(16)
380 D1+D AND 24016
390 D2=INF(15)
400 RETURN
410 FOR A=0 TO 500: REM THIS IS A SHORT DELAY
420 NEXT A
430 RETURN
```

Photo 3: Touch panel input using the program of listing 5. The line of text at the bottom of the display was entered by touching the index finger to each letter in turn. The photo is shown with the letter P about to be pressed.

concept is used in the calculator of photo 2. While never meant to replace the hand held calculator it uses a routine similar to the previous example to determine the action of each of the 16 possible entries. The picture is included to present the reader with one of the many possible applications of the scanner. The program, however, is quite long and difficult to explain in an introductory article such as this.

Simulated Keyboard

One use of the touch panel would be the simulation of direct keyboard entry. Obviously this technique is valuable only where limited data entry is required. Large menu selection programs with numerous choices displayed may not always have the particular item of interest. By having one of the available selections be a keyboard display and entry routine such as photo 3 and listing 5, the miscellaneous entry could be accommodated. The program of listing 5 displays a keyboard on the video screen and allows one to type by pointing to the individual characters. The example does not include punctuation and a carriage return, but they could be easily accommodated.

One final note. Using the touch panel need not eliminate the standard ASCII keyboard as an input device. By using the BASIC INPUT command, keyboard entry is still available to the user as is the scanner through a callable subroutine. A program could be written where some entries come from the touch panel and others from the keyboard. A more versatile program would allow input from either device at any time.

Listing 6 is a simple program which demonstrates how BASIC can scan two input devices simultaneously and provide appropriate response.

I hope that this touch panel design will spark the creative interests of other computer enthusiasts. In a field where technology advances by leaps and bounds and product obsolescence can be described in months, innovative ideas are necessary to extend the concept of creative home computing. By adding advanced peripherals and high level languages, system obsolescence is delayed considerably.

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S2L: An Altair (S-100) to LSI-11 Bus Adaptor

For many months, those of us who admire the architecture of the PDP-11 computers have been looking for a way to adapt the wealth of Altair (S-100) bus products to this processor. The introduction of the Heath H11 (LSI-11 based) processor has further emphasized the need to solve the problems which have thus far made the LSI-11 incompatible with the Altair (S-100) bus peripherals. This article describes the problems which exist, and one solution which I see for them. It has been written in advance of actually implementing the solution, but it should prove valuable to all those experimenters who wish to take up the challenge of an LSI-11 to Altair bus adapter.

For years, the only problem with the LSI-11 as a personal computer has been price. The processor board (KD11-F) itself is a rather good deal at a discount level of 20 to 30 percent, but the accessories are somewhat expensive compared with typical personal computing products as seen in table 1.

Most of the extra expense of the LSI-11 systems can be attributed to three factors:

1. The DEC prices are generally higher. The memory prices demonstrate this.
2. The use of highly regulated power supplies with the DEC products results in a more costly power supply. In addition, few experimenters are likely to homebrew such a power supply due to its complexity and its being the single element which could cause major destruction should it fail.
3. The LSI-11 has no front panel switches, and instead requires the user to examine and modify the state of the machine via a serial console device. While most industrial customers of DEC are able to afford the high cost of a serial terminal, many

Table 1: Price comparisons of Industrial quality Digital Equipment Corporation LSI-11 modules and systems with functionally similar modules for the Altair (S-100) bus.

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<th>Component</th>
<th>Typical Hobby Price (S-100 Products)</th>
<th>Typical DEC/MOB/ RDA Price Comments</th>
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<td>$500 for 16 K bytes</td>
<td>$900 for 16 K bytes Required</td>
</tr>
<tr>
<td>Serial IO</td>
<td>$100</td>
<td>$230</td>
</tr>
<tr>
<td>Parallel</td>
<td>$100</td>
<td>$200</td>
</tr>
<tr>
<td>Video display memory</td>
<td>$200</td>
<td>$600</td>
</tr>
<tr>
<td>Power supply</td>
<td>$100</td>
<td>$400 to $1000</td>
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<tr>
<td>Backplane</td>
<td>$150</td>
<td>$350</td>
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<tr>
<td>Chassis</td>
<td>$200</td>
<td>$350</td>
</tr>
<tr>
<td>Prototyping card</td>
<td>$25</td>
<td>$75 to $150</td>
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</tbody>
</table>

These prices were effective at the time of the article's writing. Current prices differ markedly. . .CH
hobbyists have discovered that memory mapped video is both cheaper and faster than a serial device. Because of this, DEC's decision to use the serial interface in this fashion forces a user to either support two terminals (one serial and one memory mapped) or make do with the serial device. It is unfortunate that a serial device, at any reasonable data rate, is simply unacceptable for some of the applications which an experimenter might wish to pursue, one example of which is state of the art word processing applications.

The three conflicting forces of the high prices of the LSI-11 systems, the desire for that processor's architecture, and the problems with the serial terminal requirement have kept me from going ahead with an LSI-11 system for well over a year. I have finally started on a project of my own which is to adapt an LSI-11 to Altair (S-100) bus peripherals and memory.

My idea was that, since the widest variety of reasonably priced peripherals are available on the Altair (S-100) bus, I should build an Altair (S-100) to LSI-11 bus adaptor (S2L). In order to start the design of an Altair bus adaptor, a number of decisions had to be made. Initially, I decided that splitting the 16 bit LSI-11 bus (also known as the "Q" bus) into two 8 bit Altair (S-100) buses, one for the even bytes and one for the odd bytes, would create too much havoc. Certainly one could purchase pairs of memory boards and allocate them in the memory address space appropriately, but when dealing with devices such as memory mapped video displays, adjacent bytes on the screen would be every other byte in the address space of the LSI-11. Additionally, two of every card would be needed in most cases, and adjacent memory mapped IO ports (the only type being considered in the case of the PDP-11 architecture) would be on alternate cards. For this reason, I felt that only one Altair (S-100) bus should be connected to the bus adaptor. This implied that multiple byte reads and writes would have to be performed by the bus adaptor and some sort of state machine would have to be built to do this.

The project was made more difficult by the fact that the LSI-11 allows both 16 bit word width reads and writes, as well as single byte writes. (Single byte reads are not required, since the processor can ignore whatever data it wishes.) Additionally, a read modify write cycle is provided, and that had to be supported by the bus adaptor.
Finally, both direct memory access and vectored interrupts had to be supported if there was to be any hope of running LSI-11 software on the beast which would result. It should be noted that just because a memory address responds from the Altair (S-100) bus, that doesn't mean that it couldn't be built to look to the LSI-11 as if it were a "normal" LSI-11 device interface. I wouldn't be giving up the facility to use standard PDP-11 software by building this bus adapter, but merely making it a bit more difficult.

I should note here that what follows is an untested design based on the references given at the end of the article and some conversations with friends who have Altair (S-100) systems. A variety of Altair (S-100) schematics from Processor Technology, IMSAI, Technical Design Labs and Cromemco, to name a few, were scanned to try to insure some approximation of compatibility, but the design is neither built nor tested. I welcome any comments from readers who are interested in this project.

The block diagram of the S2L bus interface box is shown in figure 1. It consists of three main sections devoted to memory signals, direct memory access signals and interrupt signals. The schematics for the control logic blocks may be found in figures 7 thru 9, but for the time being, I will discuss their function rather than their detailed implementation in order to simplify the discussion.

Let us first consider a memory read operation as diagrammed in figure 2. Note that all times in the timing diagrams are sequenced correctly, but, many times they are not to scale. Also, note that the clock (F2) may be shown as being synchronous with some signals, but this is not necessarily so since the LSI-11 bus is an asynchronous bus. The LSI-11 indicates the start of a bus cycle by asserting the BSYNC L signal. ("Asserted" means going into a logical 1 state, not becoming +4.5 V;
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I am using the trailing "L" to denote negative logic, so in this case assertion means going to 0.4 V.) The negative logic used by all LSI-11 bus signals is due to the bus being implemented with open collector logic, rather than the three state logic which is common in most hobby computers. The rising edge of BSYNC should be used to latch the data and address bus lines (BDAL0 L to BDAL15 L), since at this time they contain the address for the bus cycle. When BDIN L is asserted, the first of the two Altair (S-100) bus cycles occurs. This cycle occurs during the first complete cycle of the S2L clock that occurs after BDIN L is asserted. The first byte read is the most significant byte of the word (ie: the byte with the odd address), and the LSCMP signal is asserted during this time in order to provide the correct address on the Altair (S-100) bus. I am assuming that since only 16 bit word reads may be made, all addresses on the bus during read cycles will be even addresses.

The falling edge of the S2L clock (\( \Phi_2 \)) latches the most significant byte of data enabled by the low state of the MSBCLK signal (\( D \) in figure 2). Then the second read cycle is initiated, this time for the least significant byte (even address). When the cycle completes, the least significant byte is latched with the next S2L clock enabled by a low state on the LSBCLK signal (\( B \) in figure 2). After this, LDEN is asserted to drive the latched data onto the LSI-11's "Q" bus, and BRPLY L is sent back to the LSI-11 to tell it that the data on the bus is valid. The termination of the BDIN signal indicates to the S2L that the data has been accepted by the LSI-11, and the S2L then terminates BRPLY L.

For this interface to work with a reasonable variety of Altair (S-100) bus memory boards, phase 2 clock, RDY1, RDY2 and WAIT signals are provided. Any S2L clock pulse may be inhibited by one or both of the ROY lines until a slow peripheral has data ready, or has accepted data, in a manner similar to that of the 8080 and 6502 processors.

The write cycle, diagramed in figure 3, is almost identical to the read cycle. The differentiation between read and write is made by the LSI-11 by asserting the BDOUT L signal rather than BDIN L. During a write, rather than having to provide two clocks to latch the bytes read, the S2L must provide
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a byte selection signal (DOUTSEL) to a multiplexer which will determine which half of the word will be written at any time. The timing is as in the figure. As in the case of the read, I assume that only word width writes will occur with a word (even) address.

In order to perform a single byte write cycle, the S2L performs a normal write cycle, except that it skips the first of the two Altair (S-100) bus writes. Since it is the write to the address with the inverted lowest bit which is skipped, the correct byte is written in half of the time, and the cycle terminates normally. The diagram for this is shown in figure 4.

The LSI-11 bus supplies signals with which the memory and device interfaces reply to the LSI-11 when IO transactions take place (BRPLY L). The S2L adaptor will respond with a BRPLY L signal whether the address requested is implemented or not. This will cause problems with some LSI-11 software and firmware, especially the firmware ODT LOAD command which sizes memory automatically by sensing when memory addresses fail to set a BRPLY L response. Also, the system of reply signals has another advantage which will be lost when using the S2L adaptor: when attempting to write to ROMs on the LSI-11 system, no BRPLY L is generated and a bus time-out error occurs, which is a good error detection system. The S2L will effectively eliminate this facility.

The procedure for dealing with direct memory access (DMA) is much easier on the Altair (S-100) bus than on the LSI-11 bus, and the S2L interface enables the Altair (S-100) devices to take advantage of the simpler protocol. Looking at figure 5, the device starts the DMA cycle by asserting the HALT L signal to request use of the bus. The assertion of BDMR L by the S2L requests the use of the bus by a peripheral of the LSI-11. The simultaneous assertion of BDMGI L and the termination of BSYNC L and BRPLY L indicates that the DMA privilege has been granted by the LSI-11. The S2L then responds by terminating the BDMR signal, and by asserting both the BSACK L signal to tell the LSI-11 that the bus is in use, and the HLDA L signal to tell the Altair bus peripheral that it may now use the bus. Note that if more than one peripheral wishes to perform direct memory

Figure 4: Timing diagram of an LSI-11 memory write (8 bit byte) cycle as it is interpreted by the S2L and passed on to the Altair (S-100) bus.

Figure 5: Timing diagram for the initiation of DMA activity on the Altair (S-100) bus between memory segments on that bus and peripherals on that bus. (DMA from an Altair (S-100) bus peripheral to peripherals or memory on the LSI-11 "Q" bus is not supported in this design.)
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Figure 6: Timing diagram of the S2L interface's response to an Altair (S-100) bus vectored interrupt signal. When one of the eight possible vectored interrupt signals is asserted (low), the S2L interface responds by creating a vectored interrupt sequence for the LSI-11 "Q" bus.

access, neither will be able to determine easily which device is being selected. Whenever the Altair (S-100) bus peripheral is finished with the bus, it terminates the HALT L signal, causing the S2L to terminate the BSACK L signal, releasing the bus for the LSI-11 to use.

Note that this interface will not allow Altair (S-100) bus devices to perform DMA to any memory which is on the LSI-11 side of the S2L; I felt that the simplicity of the interface as shown, combined with the complexity of the extended function interface, was justification for leaving things as shown. In any event, one justification for the development of this adaptor was that Altair bus memory was cheaper than DEC memory, so one can expect most of the system memory to be Altair (S-100) bus memory.

One other point to make is that the LSI-11 on board memory is dynamic and requires refreshing, which the LSI-11 does by microcoded routines. This microcoded refresh creates bursts of bus activity every 2 ms, lasting about 130 µs. These bus activations can cause problems in a real time environment, and can cause data overruns in DMA devices if these devices do not allow enough internal buffering to last the 130 µs. Although nonburst-mode refresh is possible, the prices which DEC asks for the module are pretty high for the facility. For this reason, use of Altair (S-100) bus static memory and disabling of the KD11-F's dynamic memory and refresh microcode might be useful to some people.

The eight vectored interrupt lines on the Altair (S-100) bus lend themselves directly to interfacing with DEC's vectored interrupt scheme. Looking at figure 6, the timing for the S2L's interrupt sequence is given. Whenever one of the vectored interrupt inputs from the Altair (S-100) bus (VI0 thru VI17) is asserted, BIRO L is sent back to the LSI-11 to request interrupt service. The

Figure 7: Memory Control Logic.
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LSI-11 will respond by asserting BIAKI L and BDIN L, the former to request that an interrupt vector be placed on the bus, and the latter to indicate that data is coming in on the bus. The S2L responds to this by placing the vector on the bus, and by asserting BRPLY L, to inform the LSI-11 that the bus value is now valid data. The termination of BDIN L and BIAKI L by the LSI-11 results in the S2L's termination of BRPLY L and the release of the bus for other uses. At this point, an interrupt should occur. Each of the eight interrupt lines is prioritized and will cause an LSI-11 interrupt when asserted. The LSI-11 vector address for each Altair (S-100) bus vectored interrupt line will be the value programmed in the read only memory.

I am not going to go through the schematics in figures 7 thru 9 in detail, since their function is fairly well-defined by the timing diagrams and the above discussions. However, a few notes are in order. The use of the 7495 is a bit subtle since the load, which occurs via CLK2 whenever a BDIN or BDOOUT signal is asserted, changes the mode of the shift register from LOAD to SHIFT. This allows the first write to be skipped conditionally upon the state of the BWTBT L signal at the start of the write cycle, and allows the shifting to stop when the one bits coming in from the serial input reach the third flip flop. The latches used for most significant byte and least significant byte storage are 8551s since they have three state buffers, which allow their output to be placed on the LSI-11 bus conditionally.

REFERENCES


Also: numerous Altair (S-100) bus peripherals schematics borrowed from friends served as background information for this discussion.

Figure 8: Direct memory access control logic.

Figure 9: Interrupt control logic.
The Electric Pencil II is a Character Oriented Word Processing System. This means that text is entered as a string of continuous characters and is manipulated as such. This allows the user enormous freedom and ease in the movement and handling of text. Since line endings are never delineated, any number of characters, words, lines or paragraphs may be inserted or deleted anywhere in the text. The entirety of the text shifts and opens up or closes in full view of the user. The typing of carriage returns as well as word hyphenation is not required since lines of text are formatted automatically.

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SVN | VDM | TTY or similar | Tarbell | North Star | $125.
DS | SOL | Diablo 1610/20 | Cuts | --- | $150.
DP | VFI | Diablo 1610/20 | Tarbell | --- | $150.
DV | VDM | Diablo 1610/20 | Tarbell | --- | $150.
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The decimal point merely tells where the boundary exists between the positive powers of ten and the negative powers of ten. Numbers to the left of the decimal point are positive powers of ten and those to the right are negative powers of ten. In binary (base 2) numbers the same rule applies. The base 10 equivalent of the binary number 101.11 is:

\[
\begin{align*}
1 \times 2^2 &= 1 \times 4 = 4.00 \\
0 \times 2^1 &= 0 \times 2 = 0.00 \\
1 \times 2^0 &= 1 \times 1 = 1.00 \\
1 \times 2^{-1} &= 1 \times .5 = 0.50 \\
1 \times 2^{-2} &= 1 \times .25 = 0.25 \\
\end{align*}
\]

\[
\frac{5.75}{5.75}
\]

The `.` , which is now called a binary point, denotes the division between positive and negative powers of two. This concept can be expanded to any base, but here we will only consider base 10 and base 2. In general the `.` might be called the “base point.”

Quite often it is more convenient to represent real decimal numbers in scientific notation. This allows both very small and very large numbers to be written with the fewest number of digits (e.g., \(3.75 \times 10^4\), rather than \(0.000000000375\)). Numbers in scientific notation are represented by three parts: integer portion, fractional portion and exponent. In order to conserve memory within the computer and to make calculations have fewer steps, it is more convenient to represent all real numbers with only a fraction and an exponent. This is accomplished by moving all digits to the right of the base point and adjusting the exponent appropriately. Thus all numbers are of the form: \(\text{FFF} \times 10^{EE}\) in base 10 (where “FFF” are the fractional digits and “EE” is an expression for the power of ten exponent). This change of form does not in any way alter the value of the number or change the accuracy of the subsequent calculations. For example: \(3.75 \times 10^2\)
becomes $0.375 \times 10^3$ thus eliminating the integer portion of the number.

If the fractional portion of a number has a fixed number of digits as is the case within a computer, then the greatest accuracy is achieved if the digit following the base point is nonzero. Using a 5 digit fraction, the number $0.37868 \times 10^5$ is more accurate than $0.03787 \times 10^6$. We now have formulated two rules that will make calculations easier and maintain maximum accuracy:

- Floating point numbers will consist of only a fraction and an exponent.
- Floating point numbers will be adjusted so that no zeros immediately follow the base point.

The only exception to these rules is the number zero which is allowed to violate rule two. Manipulating numbers so that they conform with the above rules is called normalization.

All of the above examples were in base ten, but as might be expected the concepts are just as valid in base two except the exponent is now a power of two instead of ten. Therefore, numbers are of the form: $FFF \times 2^{EE}$ (where $FFF$ and $EE$ are now hexadecimal representations of binary numbers). At this point we must decide upon a specific format to use within the computer that will give sufficient accuracy without wasting memory. A fraction containing 24 bits gives an accuracy of $1/2^{24}$ or about seven decimal places. A two's complement exponent of base 2 containing seven bits gives an exponent range of approximately $\pm 10^{\pm 19}$. This format has sufficient magnitude range for many applications and can represent numbers over 38 decimal orders of magnitude.

There are several common formats for floating point numbers. In some, the exponent is a power of 16 and a fraction is considered normalized if any of the four most significant bits are set. Exponents are often represented in "excess" form instead of two's complement form. In this form some appropriate number is added to all exponents so they are all positive. The specific format I chose consists of four 8 bit bytes for each number and is shown in figure 1. The high order bit (bit 7 typically) of byte one is the algebraic sign of the number ($1 = -$). The low order seven bits of the first byte (bit 6 to bit 0) are the signed two's complement value of the exponent. Bytes two, three and four contain the normalized unsigned fraction with the understood binary point preceding byte two. Note that bit seven of byte two is 1 for all normalized numbers except zero because of normalizing rule two.

Some sample numbers and their decimal equivalents are given in table 1.

### Table 1: An example of binary floating point numbers and their decimal equivalents.

<table>
<thead>
<tr>
<th>Binary</th>
<th>Decimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000000</td>
<td>.10000000 00000000 00000000</td>
</tr>
<tr>
<td>00000001</td>
<td>.10000000 00000000 00000000</td>
</tr>
<tr>
<td>00000001</td>
<td>.11000000 00000000 00000000</td>
</tr>
<tr>
<td>10000001</td>
<td>.1 1000000 00000000 00000000</td>
</tr>
<tr>
<td>01111111</td>
<td>.10000000 00000000 00000000</td>
</tr>
<tr>
<td>11111111</td>
<td>.10000000 00000000 00000000</td>
</tr>
<tr>
<td>00000000</td>
<td>.10000000 00000000 00000001</td>
</tr>
</tbody>
</table>

### Listing 1: Algorithm for inputting real numbers. This algorithm will result in a floating point number in the four byte form described in this article.

```
Begin
  Clear exponent and integer of answer
  Clear fraction of answer (4 bytes)
  Do while input character * '.'
    If input character = ' ' then set fraction sign = 1
    If input character is a number then
      Convert input character from ASCII to binary
      Integer: = integer * 10 + input number
    End if
  End do
  N: = 1
  Do while input character = number and N < 8
    Convert input character from ASCII to binary
    Fraction: = fraction + (Table(N) * input number)
    N: = N + 1
  End do
  Do while integer > 0
    Shift integer and fraction one bit right
    Increment exponent
  End do
  Normalize answer
  Roundup answer
  Delete integer portion and fraction byte 4
End
```

### Ins and Outs

Now that we’ve defined a format for real numbers, how can we put it to use? Several subroutines will be required. We need to be able to read real numbers from a terminal.
and convert them to our defined format and vice versa. Also, we need to outline how we can operate on real numbers once they are converted. First, the ins and outs.

The conversion to and from the terminal

Table 2: Decimal fraction to binary equivalent conversions. The table covers only the first seven digits since the accuracy of the routines we are considering is only seven places. This conversion assumes that the exponent is set to zero.

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>00011001 10011001 10011001 10011001 = 10^-1</td>
</tr>
<tr>
<td>0.01</td>
<td>00000010 10001111 01011100 00101000 = 10^-2</td>
</tr>
<tr>
<td>0.001</td>
<td>00000000 01000001 10001001 00110111 = 10^-3</td>
</tr>
<tr>
<td>0.0001</td>
<td>00000000 00000110 10001101 10111000 = 10^-4</td>
</tr>
<tr>
<td>0.00001</td>
<td>00000000 00000000 10100111 11000101 = 10^-5</td>
</tr>
<tr>
<td>0.000001</td>
<td>00000000 00000000 00010000 11001101 = 10^-6</td>
</tr>
<tr>
<td>0.0000001</td>
<td>00000000 00000000 00000000 10101101 = 10^-7</td>
</tr>
</tbody>
</table>

Example 1.

1 x 0.10 = 1 x 00011001 10011001 10011001 10011001
+ 5 x 0.01 = 5 x 00000010 10001111 01011100 00101000 00100110 01100110 01100110 0110001

Example 2.

Integer Fraction Exponent
00001101 00100110 01100110 01100110 01100110 01100110 01100110 01100110 00000000

Example 3.

Integer Fraction Exponent
00000000 11010010 01100110 01100110 01100110 01100110 01100110 01100110 00000000

Example 4.

Exponent Fraction
00000100 11010010 01100110 01100110

Table 3: Portion of table used to convert the exponent of 2^e into decimal notation of the form F x 10^{Exp}.

<table>
<thead>
<tr>
<th>e (index)</th>
<th>Exp (1 byte)</th>
<th>F (3 bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>00000010 (2)</td>
<td>00101000 11101010 11000001 (0.16)</td>
</tr>
<tr>
<td>3</td>
<td>00000001 (1)</td>
<td>11000100 11000110 11001110 (0.60)</td>
</tr>
<tr>
<td>2</td>
<td>00000001 (1)</td>
<td>01100110 01100110 01100110 (0.4)</td>
</tr>
<tr>
<td>1</td>
<td>00000001 (1)</td>
<td>00100110 00100110 00100110 (0.2)</td>
</tr>
<tr>
<td>0</td>
<td>00000000 (0)</td>
<td>00000000 00000000 00000000 (0)</td>
</tr>
<tr>
<td>1</td>
<td>00000000 (0)</td>
<td>10000000 00000000 00000000 (0.5)</td>
</tr>
<tr>
<td>2</td>
<td>00000000 (0)</td>
<td>01000000 00000000 00000000 (0.25)</td>
</tr>
<tr>
<td>3</td>
<td>00000000 (0)</td>
<td>00100000 00000000 00000000 (0.125)</td>
</tr>
</tbody>
</table>

is the most difficult part of handling floating point numbers. An attempt is made here to outline a procedure that is well adapted to microprocessors. Several other algorithms are outlined in *The Art of Computer Programming*, volume 2 by Donald Knuth (see references following this article) including information on converting to and from scientific notation.

Suppose the input string 13.05 is typed at a terminal. Since the computer will see the characters as they are typed left to right, the program in listing 1 can easily convert any number preceding the decimal point into a binary integer. In this example the 13 becomes 00001101, assuming an 8 bit integer. Once the decimal point is read the fraction can be calculated if a table of unnormalized fractions corresponding to the binary equivalent of 10^-n is stored in memory. Since there is no need for n to be larger than the accuracy of the final format, table 2 was calculated with n equal to seven. Table 2 was calculated using a BASIC program to determine which bits in the fraction should be set. Note that the fractions in this table are 32 bits wide instead of the 24 bits required in the final answer. This is done to insure the accuracy of the conversion. Using this table and starting with a zero exponent byte and zero in a 4 byte fractional portion in the answer, when the first number following the decimal point is typed on the terminal it is multiplied by the table value of the fraction for 0.1 and added to the fraction of the answer. Subsequent inputs are multiplied by 0.01, 0.001, etc, and added to the answer until the bottom of the table is reached after seven inputs or the input string is exhausted. Since the input numbers are 0 thru 9, it is easier and takes less time in a microprocessor to do the multiplication by successive additions. For the example input, 13.15, the fraction is calculated by example 1. Including the integer portion and the exponent the input becomes the representation in example 2. Normalizing this by shifting the integer and fraction four bits to the right and adding 4 to the exponent it becomes example 3.

Now the integer portion and the low order byte of the fraction can be deleted after incrementing the next to low order byte by seven of the low order byte was set (rounding up). See example 4 for the final value in the correct 4 byte format. Had the input number been -13.05 instead of +13.05, the only difference in the number generated would be bit seven of the exponent (fraction sign bit) would be set. Note that if the input had been something like 0.005 the normalizing process described above would require left shifts of the frac...
tion while decremenenting thus creating a negative exponent.

Outputting real numbers is slightly more difficult. The fraction and exponent part must be dealt with simultaneously since conversion of the exponent from base 2 to 10 will affect the fraction. Due to this complexity, it is preferable to output real numbers in scientific notation. The output form that is used is \(1.305 \times 10^2\).

To accomplish the conversion we will need a rather large (4 by 128 byte) table to convert \(2^e\) (where \(e\) is the exponent of the real number to be output) to \(F \times 10^E\) (where \(F\) is an unnormalized fraction in our 3 byte notation and \(E\) is the power of 10 of the number we wish to print. A portion of the middle of the table is given in table 3.

The base 2 exponent \(e\) is not a member of the table, but is used as the index into the table to retrieve values of \(E\) and \(F\). Using \(e\) we access the table and multiply the fraction \(F\) times the fraction of the number we wish to output using a multiply fraction subroutine described later. The resultant fraction of this multiplication will be the fraction that must be converted and printed followed by the letter E and the decimal value of \(E\), including its sign, from the table to obtain the desired scientific notation.

Printing of the fraction uses the same table as used for converting to real format. In the first iteration the binary fraction for \(0.1\) is subtracted from the fraction until the fraction goes negative. For each subtraction except the last a counter is incremented and becomes the number to print. After the number is printed, the fractional value of \(0.1\) is added back into the fraction. This whole process is effectively a binary divide by \(0.1\). After \(0.1\) is added back, the procedure is repeated for \(0.01, 0.001, \ldots\), until all seven output digits are printed. This process is summarized in listing 2.

It should be noted that the above algorithms pose particular problems on various implementations and the programmer should be cautious of such things as overflow and carry flags as well as round off errors while doing the multiprecision operations.

The Arithmetic

Now we have a format for floating point or real numbers and we know how to input and output them. All that remains is the internal manipulation subroutines. All these subroutines require two normalized real arguments, which in the following text and listings will be referred to as argument 1 (ARG1) and argument 2 (ARG2). They all create a normalized real answer (ANS). We will use the predefined format except that during the internal manipulation some extra bits are occasionally needed at the right of the fraction to retain accuracy. Only a couple of bits are necessary, but since most microprocessors have 8 bit words, it is easier to add a whole byte to each fraction thus creating a 4 byte fraction instead of the prescribed three bytes. This fraction will be rounded to a 3 byte fraction in the defined format before returning to the caller of the manipulation subroutines.

Addition is defined as \(\text{ARG1} + \text{ARG2} = \text{ANS}\). Once again the base 10 analogy will be useful in understanding how to implement an algorithm. If we desire the sum of the two normalized real numbers \(0.375 \times 10^5\) and \(0.22 \times 10^4\), we must first make the exponents equal before we can add the fractions. Once the exponents are equal, the fractions can be added and the answer given the common exponent. Thus, the example becomes:

\[
0.375 \times 10^5 + 0.22 \times 10^5 = 0.397 \times 10^5
\]

To make the exponents equal in this example, the number with the smaller exponent was shifted right \(n\) decimal digits and its exponent incremented by \(n\). It is desirable to adjust the smaller number since shifting the larger number would require left shifts that might result in numbers being shifted into the integer portion which

---

**Listing 2: Algorithm for outputting real numbers.** This algorithm uses table 2 to convert the fraction. The output algorithm shifts the fraction and integer part left until the exponent equals zero or bit 7 of the integer word is set to 1. If bit 7 of the integer word is set, any further shifts will destroy the number.

```plaintext
Type entry = record of
  Exp: 8 bit binary
  F: 24 bit fraction
Var conv-table: array [−64..63] of entry
          table: array [1..7] of 24 bit fraction
          (* e is the base 2 exponent of the number to be output*)
Begin
  Fraction = conv-table[e].F * fraction of number to be output
  If Fraction sign = 1 then print '+';
  Print decimal point
  N: = 1;
  Do while N < 8
    CTR := -1
    Do while fraction is positive
      Fraction = fraction-table(N)
      CTR := CTR + 1
    Enddo
    Fraction = fraction-table(N) + table(N)
    Convert CTR to ASCII and print it
  Enddo
  Print 'E'
  If conv-table[e].Exp is negative then print '-';
  Endif
  Convert conv-table[e].Exp to decimal ASCII and print it
End
```

---

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would violate the defined format. Any shifting, however, can create accuracy problems in a fixed digit (or bit) computer, since if the magnitude of two numbers differs by a large amount, their sum will be equal to the larger number. For example, if we had a calculator with six digits for a fraction and we added $0.300 \times 10^8$ and $0.20 \times 10^9$, the answer would be $0.300000 \times 10^8$ since shifting 0.20 seven digits to the right would cause it to become zero.

Listing 3: Algorithm for real addition and subtraction. Before additions or subtractions can take place the numbers must be manipulated so that their exponents are equal.

Begin
  Do while exponent ARG1 ≠ exponent ARG2
    If exponent ARG1 > exponent ARG2 then
      Shift fraction ARG2 right one bit
      Increment exponent ARG2
    Else
      Shift fraction ARG1 right one bit
      Increment exponent ARG1
    Endif
  Enddo
  If fraction ARG1 is negative then 2's complement fraction ARG1; Endif
  If fraction ARG2 is negative then 2's complement fraction ARG2; Endif
  If operation is addition then
    Fraction ANS = fraction ARG1 + fraction ARG2
    Else
    Fraction ANS = fraction ARG1 - fraction ARG2
  Endif
  Exponent ANS = exponent ARG1 or ARG2
  Normalize ANS
  Roundup ANS
End

Listing 4: Real multiplication algorithm. When multiplying real numbers it is not necessary to worry about the exponents being equal. Multiplication can take place under any conditions.

Begin
  Fraction ANS = fraction ARG1 * fraction ARG2
  Exponent ANS = exponent ARG1 + exponent ARG2
  Set overflow flag if exponent overfloued or underflowed
  Normalize ANS
  Roundup ANS
End

Listing 5: The real division routine must check to see if the dividing number is zero. If it is, the overflow flag is set and the routine is ended. The fractional part of the number to be divided should always be smaller than the dividing number. This is assured by shifting the number to be divided one place left and incrementing the exponent.

Begin
  If fraction ARG2 = 0 then
    Set overflow flag
  Else
    Shift fraction ARG1 one bit right
    Increment exponent ARG1
    Fraction ANS = fraction ARG1/fraction ARG2
    Exponent ANS = exponent ARG1 - exponent ARG2
    Set overflow if exponent overfloued or underflowed
    Normalize ANS
    Roundup ANS
  Endif
End

Binary real addition is identical to the above decimal example except the shifts are by $n$ binary bits and the exponent is a power of 2. The algorithm in listing 3 first checks to see if the exponents are equal. If not equal, the fraction of the smaller argument is shifted one place right and its exponent incremented. This continues until the exponents are equal. Since our format stores the fractions as absolute unsigned values, all the fractional portions of negative fractions must be two's complemented before addition can proceed. Once the negation of any negative fractions is completed, the fractions can be added by a multiprecision addition. The fractional portion of the answer is then composed of the sum of the adjusted fractions and the exponent becomes the common exponent. This answer may need to be normalized. In fact, all the manipulation subroutines will require a check for normalization before exit, and therefore a subroutine to normalize arguments is desirable.

Subtraction is defined as $\text{ARG1 - ARG2 = ANS}$. The subtraction routine is identical to the addition routine except a multiple precision subtract is substituted for the addition. In most implementations the addition and subtraction routines are the same routine with a flag to indicate whether a subtraction or addition of the fraction should occur.

Multiplication of real numbers is easier than addition since the fractions can be multiplied regardless of the exponents. The multiplication algorithm in listing 4 is defined as: $\text{ARG1 \times ARG2 = ANS}$. The multiplication of the fractions involves a 32 bit by 32 bit multiplication, but only the most significant 32 bits of the result are necessary which reduces the complexity of the multiplication somewhat.

For details on writing a multiplication subroutine check the references, or better yet check the user group library for your microprocessor to see if one already exists. The biggest problem with real multiplication is that overflow or underflow of the exponent can occur during the addition of the exponents. Therefore, the subroutine must take precautions to check for overflow or underflow and flag the result as erroneous if either occurred. The answer obtained by the above algorithm may need to be normalized before returning it to the caller.

Division is similar to multiplication and is defined as $\text{ARG1/ARG2 = ANS}$. Since most division algorithms will not terminate if ARG2 is equal to zero, the division algorithm in listing 5 first checks the fraction of ARG2 to see if it is zero. If it is zero, the algorithm should return with an
overflow indication. Also, many division algorithms require that the fraction of ARG1 be smaller than the fraction for ARG2. The division routine could check to see if this condition exists, or better yet, since we know both numbers are normalized (ie: the most significant bit is set) and since we have added an extra byte for accuracy, we can always shift ARG1 one bit to the right and insure that it is less than ARG2. Of course, we must add one to ARG1’s exponent to compensate for the right shift. Now we can proceed with a normal 32 by 32 bit divide of the fractions. Once the fractional portion of the answer is complete, the exponent of the answer is equal to the exponent of ARG1 minus the exponent of ARG2. Again precautions must be taken to insure (or at least flag) that no underflow or overflow of exponents has occurred. The answer may need to be normalized.

Conclusion

This article has attempted to give an overview of what is necessary to create a package of floating point subroutines that can be used for many applications. Floating point manipulation is not trivial and some microprocessors will be better adapted to the task than others. Instructions that can handle multiple precision arguments such as “add with carry,” “subtract with carry” in conjunction with shifts and rotates on memory make the implementation simpler. Be cautioned that the procedures outlined are general and any particular microprocessor will require special procedures to adjust for processor peculiarities. In any case, it seems the majority of the code is dedicated to shifting fractions right or left to insure accuracy or in checking for various error conditions.

On the positive side, a good debugged binary floating point package takes less memory and runs faster than the decimal floating point implemented in many BASIC packages. The add, subtract, multiply and divide routines lay the framework for the programmer to create more exotic subroutines such as sine, cosine, etc. Best of all, when we ask our computer to divide 5 by 2, it responds with 2.5.

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I want to use the addresses hexadecimal 0000 to 0FFF to hold all the programs and simulated IO routines that will eventually go in the 6505, then use addresses hexadecimal 1000 to 13FF for the programs that test the 6505 programs. Readers with the same problem may care to use my solution which I have been using successfully for some months.

Use address switch setting 0001 for an address range of hexadecimal 1000 to 1FFF. Then modify the connections for address lines AB10, AB11 and AB12 as in figure 1. This modification will map the KIM-1 address range of 0400 to 13FF into a KIM-2 address range of 1000 to 1FFF.

Figure 1: Modification to allow the address of the KIM-1 from hexadecimal 0400 to 13FF to be mapped into a KIM-2 address range of 1000 to 1FFF.
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5. JWACs ($5 per year)
6. Bob Jones, editor
10. For more information, send a SASE to the above address.

1. Microcomputer Investors Association
   2. 2415 Ansdel Ct
   Reston VA 22091
3. As called
5. The Microcomputer Investor
6. Jack Williams
8. Nonprofit, professional association, $30/member
9. The functional purpose of the association is to facilitate the exchange of data and information relating to investments and microcomputers with the express purpose of such interchange being directed toward maximizing profits in stocks, bonds, warrants, stock options and commodities, including commodity options and futures strategies.

1. Chesapeake Microcomputer Club Inc
2. POB 87
3. White Oak Library
   11701 New Hampshire Av
   Silver Spring MD
4. Fourth Monday at 7:30 PM
   7:30 PM
5. The Analytical Engine
6. Rich Kazmack
7. (703) 821-2873 (home)
8. $12 per year
9. Processor-oriented special interest groups, investors group, store and forward system with Bell 103 access for message and software interchange, PC networking.

1. Amateur Radio Research and Development Corp (AMRAD)
2. 1524 Springvale Av
   McLean VA 22101
3. Patrick Henry Branch Library
   101 Maple St E, Vienna VA 22180
4. First Monday of each month at 8 PM
5. AMRAD Newsletter
6. Paul L Rinaldo
7. (703) 356-8918
8. Regular $10, second in household $5, student $2. Life: regular $100, second in household $50.

1. Crystal City Computer Club
2. 3008 Mosby St
   Alexandria VA 22305
3. Commissioner’s Conference Room,
   Bldg 3, 11th Floor, Crystal Plaza
   Arlington VA
4. First nonholiday Monday, 11:30 to 12:30
5. IO
6. Russell E Adams
7. (703) 548-8261
8. $4 per year and $5 with newsletter
9. Assist newcomers and interchange of programs and ideas
10. Have small library, occasional classes, 48 members; affiliated with Chesapeake Computer Club.

1. Charlottesville Computer Hobbyists Club
2. 1928 Arlington Blvd, #209
   Charlottesville VA 22903
3. Math-Astronomy Building
   University of Virginia
4. Second Monday of each month
5. No name, monthly if possible
6. Richard A Stanley
7. (804) 296-5583 or 293-7976
8. $2 per year (supports newsletter)
Stop reading about computers and get your hands on one! With ELF II or ELF II Plus, you can run your own programs. You can master computers in no time at all. ELF II demonstrates its capabilities. ELF II is a complete package to teach you how to use almost all of the RCA COSMACK II’s capabilities. ELF II is a complete learning aid for you. You won’t find another computer like it. No wonder ERM researchers, chapters of universities and major corporations have chosen the ELF II to introduce their students and personnel to computer programming.

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If you work with large computers, ELF II and our short course with it will help you learn and make use of computer systems.

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With ELF II, you learn to use machine language—the fundamental way all computers work. You’ll be using your own programs, which is what computers are really used for.

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- **Deluxe metal cabinet for ELF II.** $25.95 plus $3 to ship.
- **Deluxe floppy disc drive for ELF II.** $25.95 plus $3 to ship.
- **Deluxe metal cabinet with plastics and disc drive for ELF II.** $39.95 plus $3 to ship.
- **RCA COSMACK II Computer Board.** $149.95 plus $3 to ship.
- **RCA COSMACK II User’s Manual.** $10.50 plus $3 to ship.

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- **RCA COSMACK II User’s Manual.**
- **RCA COSMACK II User’s Manual.**
- **RCA COSMACK II User’s Manual.**

### Other Options:

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- **$39.95 plus $3 to ship.**
- **$25.95 plus $3 to ship.**
- **$25.95 plus $3 to ship.**

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3. **City:**
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5. **Zip:**
6. **Phone:**
7. **Fax:**
8. **Credit Card:**
9. **Payment Method:**
10. **Payment Total:**

**Thank you!**

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1. Triangle Amateur Computer Club
   POB 17523
   Raleigh NC 27609
2. Dreyfus Auditorium
   Research Triangle Park
   Last Sunday of each month at 2 PM
3. Okaloosa Computer Hobbyist Club
   32 Denton Blvd, NW #72
   Fort Walton Beach FL 32548
   Every second and fourth Tuesday
4. Central Florida Computer Club
   2821 Sunset Rd
   Apopka FL 32703
   Basement of Orlando Utilities Bldg, 300 S Orange Av, Orlando FL
   Third Sunday of each month, 2 PM
5. The Shift Register
   130 September 1978 © BYTE Publications Inc Circle 132 on inquiry card.

   1. Indian River Computer Society
   2. FIT Elect Eng Dept
   3. Florida Institute of Technology
   4. FIRSTS Florida Institute of Technology Room 112
   5. First and third Thursdays of each month at 7 PM
   6. THE MBUS (monthly)
   7. Frank Canova, president

   Zips 30000 - 40000
   1. Atlanta Area Microcomputer Hobbyist Club
      POB 7602
      Atlanta GA 30357
   2. Decatur Federal Savings
      Dunwoody Village
   3. First and third Thursdays of each month
   4. AAMHC Newsletter
   5. Jim Stratigos
   6. (404) 894-3505 (days), 457-8030 (nights)
   7. $10 per year
   8. Personal computing; 6800 and 8080 systems, although other systems are used by members as well.

   Zips 40000 - 50000
   1. Amateur Computer Society of Columbus OH (ACSCO)
   2. Computer Data Systems
   3. Center of Science and Industry
   4. First Wednesday every month, 7:30 PM
   5. I/O
   6. Fred Hatfield K8VDU, president
   7. $10 per year
   8. Personal computer networking, implementation of SAM 76 language versions and amateur radio applications.

   1. The Cleveland Digital Group
   2. 8650 Harvard Av
   Cleveland OH 44105
   3. Same
   4. Third Sunday of the month, 2 PM
   5. The Shift Register
   6. David A Rolnick, chairman; programs committee
   7. (216) 524-2434
   8. $10 per year
   9. Informal meetings held every Tuesday night 7:30 on. Speakers come on a regular monthly basis (Sunday meetings).

   1. Goodyear Computer Club
   2. c/o J F Derry, D-109E PIT 1
   Goodyear T&R Co
   Akron OH 44316
   3. Goodyear Hall, 8 PM fourth Tuesday each month
   4. IAG meets 7 PM before club meeting; club meets at 8 PM, business, speaker, demos; HG meets at 9 PM
   5. The Late Edition

   S-100 BUS COMPATIBLE. The EMM 1104 single card plug-in memory has been field tested and proven in a variety of systems including the Poly 88, IMSAI 8560, TRS-80, MITS, COMPAL-80, TLD and CREMEMCO. 16K BYTES ON A CARD. Convenient plug-in card, fully burned-in, tested and guaranteed by one of the industry's largest memory suppliers. NMOS STATIC RAM. The 4K static RAMs have been proven in applications ranging from single chip memories to IBM 370 add-on systems. They are fast, reliable, and no refresh cycle is required.

   COMMERCIAL MEMORY PRODUCTS, a Division of Electronic Memories & Magnetics Corp.
   12821 Chadron Avenue • Hawthorne, California 90250 • Telephone (213) 644-0881

   NMOS static RAM
6. R Messner, Goodyear Aerospace Corp., D-47063, Akron OH 44315
7. (216) 794-7265
8. $10 per year
9. Investment analysis group (IAG), hardware group (HG), software group – under discussion (SG), setting up club library reference service for magazine exchange.
10. Have club Xerox CF-16 (Goodyear surplus) and Burroughs accounting machine. Looking for space to set up. Goodyear employees can telephone into GAC Sigma 9, 5 PM to midnight seven days a week using HG modem or equivalent. Membership not limited to Goodyear employees.

The listings follow this form:
1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

CONTAINS:
Battery Tool BW-630
Hobby Wrap Tool WSU-30 M
PC Edge Connector CON-1
DIP/IC Extractor Tool EX-1
DIP/IC Insertion Tool INS-1416
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(504) 888-4884
TWX 810-991-5229

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**Clubs and Newsletters**

**DIRECTORY, continued**

1. Compute, Evaluate, Trade
2. POB 104
   Tip City OH 45371
3. IUPUI, Indianapolis IN
4. Last Wednesday in month
5. Byte Buck
6. Charles Tzyzter
7. None
8. Business systems.

1. Dayton Microcomputer Association
2. Dayton Museum of Natural History
   2629 Ridge Av
   Dayton OH 45414
3. Same as above
4. Last Tuesday of month, 7:30 PM
5. Dayton Microcomputer Association
   Data Bus
6. Dean Lampman, president
   Marilyn Mix, vice-president
   Jack Steele, secretary
7. (513) 984-2084, 253-9468,
   256-8005, respectively
8. $10 per year includes Data Bus
9. The 6800, 8080, 6502 special
   interest groups meet individually
   at least once a month
10. For the past two years we have held a
day show of computers for the
   public. This year we demonstrated
   at the Dayton Amateur Radio Con-
   vention and at the National Airborne
   Electronics Conference.

1. Apple I Library
2. 51625 Chestnut Rd
   Granger IN 46530
3. Mail
4. Joe Torzewski
7. (219) 272-4670
8. Stump appreciated for reply
9. Promote Apple I computer

1. Floyd County Computer Enthusiasts
2. RR #2, POB 466A
   New Albany IN 47150
3. Varies
4. Set meetings are uncommon
5. None
6. Nathan Engle
8. None
9. Software, robots, artificial
   intelligence
10. Most of our members are high school
    level and we are making an effort to
get a computer center in the local
    school system. Any help we can get
    would be much appreciated.

1. Purdue University Computer
   Hobbyist Club (PUNCH)
2. Room 67, Electrical Engineering Bldg
   Purdue University
   West Lafayette IN 47907
3. Matthews Hall, Purdue University
4. Monday nights, 7 PM
5. PUNCH newsletter, published
   irregularly
6. Don Gille, president
7. (317) 463-2340
8. $2 annual dues
9. General hardware and software

1. Southeastern Michigan Computer
   Organization (SEMCO)
2. POB 9578
   Detroit MI 48202
3. Ford Automotive Safety Center
   Auditorium, Dearborn MI
4. Second Sunday of every month at
   7 PM
5. Data Bus
6. Jim Rarus, president
7. (313) 775-3320 (24 hour club news
   line)
8. $10 per year or $6 per year 50 miles
   from Detroit
9. We have a number of special interest
groups (SIGs). The following are
some of our interests: Radio Shack,
S-100 bus, KIM, 6800, Digital Group,
RCA 1802, Heathkit, medical appli-
cations, SIG-BIG large machines and
microinterfaces. A number of our
members are also employed and
interested in automotive applications.
10. Charter member of the Midwest
    Affiliation of Computer Clubs
    (MACC); host 1978 Computerfest;
active in giving talks to educational
institutions; access to club computer
message service; free time to club
members on HP 2000 BASIC system.

1. Mid Michigan Computer Club
2. 15151 Ripple Dr
   Linden MI 48451
3. Various places (members' homes)
4. Irregular
5. None
6. Tony Preston
7. (313) 735-5279
8. None
9. Helping beginners select equip111cn11;
10. Most of our members are high schoo l
    level and we arc mak ing an effort to
    get a comp ute r cen ter in the local
    school system. Any help we can get
    would be much appreciated.

1. Eastern Iowa Computer Club
2. POB 164
   Hiawatha IA 52233
3. REC Bldg, basement
   999 35th St
   Marion IA
4. Last Sunday of month
5. Yes
6. Cecil Fretwell
7. (319) 386-3723
8. $6 per year
9. Softwa re, robots, art ifica l
   intelligen ce
10. Most of our members are high school
    level and we are making an effort to
get a computer center in the local
    school system. Any help we can get
    would be much appreciated.

1. Quad City Computer Club
2. 2155 W 30 St
   Davenport IA 52804
3. Rock Island Arsenal
   Rock Island IL 61201
4. Monthly newsletter
5. Cecil Fretwell
7. (319) 386-3723
8. $6 per year
9. Softwa re, robots, art ifica l
   intelligen ce
10. Most of our members are high school
    level and we are making an effort to
get a computer center in the local
    school system. Any help we can get
    would be much appreciated.
1. FPGA-Moorhead Computer Club (FMCC)
2. POB 2017
Fargo ND 58102
3. First Thursday: NDSD Fargo
Third Thursday: MSU Moorhead
4. First and third Thursdays at 7:30 PM
5. Dan Kary
(218) 233-6682
6. $5 per year
7. Circuit design, promoting small computer interest; general programming.

About 80 members on list.

1. Missoula Amateur Computer Club
2. 2203 E Crescent
Missoula MT 59801
3. First Monday of month
4. David Eggebraten
(406) 728-5657
5. No dues
6. All aspects of microcomputers for persons in western Montana.

Zips 60000 - 70000

1. CACHE (Chicago Area Computer Hobbyist's Exchange)
2. POB 52
South Holland IL 60473
3. Northern Illinois Gas Bldg, Golf and Shermer Roads, Glenview IL
4. 1 PM, third Sunday of month, July excluded.
5. MicroSCOPE and meeting announcements
6. Hotline (recorded announcement), (312) 849-1132
7. $10 per year
8. More general than special - CP/M local users group; SOL/Cuts and 8080 - Tarbell cassette software with libraries; computer aided instruction group getting started; North Star users; Digital Group Users, etc.
9. Regular presentations by manufacturers, stores and fellow hobbyists.

1. ICE 9ine Inc
2. POB 291
Western Springs IL 60558
3. Various dinner meeting locations
4. 9ine Journal
5. R A Hoekstra
(312) 530-0067
6. Newsletter subscription is $10 per year
7. Communication via newsletter information about RCA 301/UNIVAC Series 70 users, equipment, and software.

The listings follow this form:
1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Due or subscription fees
9. Special interests
10. Other comments

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You learn to solve complex problems by breaking them down into easily programmed modules. Prepared by professional design engineers, the Modu-Learn™ course presents systematic software design techniques, structured program design, and practical examples from real 8080A micro-computer applications. All in a modular sequence of 10 lessons, more than 500 pages, bound into one practical notebook for easy reference. You get diverse examples, problems, and solutions. With thorough background material on micro-computer architecture, hardware/software trade-offs, and useful reference tables. All for only $49.95.

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G/2 Extended Basic can read tapes written in PT's 5K and Extended Basic. This allows you to use all your previously developed programs.

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THE REASON YOU BOUGHT YOUR COMPUTER.
Introducing G/2 Standard Basic for the SWTPC computer series. It'll load faster and do more than you ever thought possible.

Developed by Microsoft™, the industry leader in microprocessor languages, and proved for more than 3 years in MITS applications, G/2 Standard Basic is now available for the first time for use with Southwest Technical Products Corporation's 6800 hardware.

Four to eight times faster than the basic you're now using, this interpreter offers string arrays, extensive string functions, Peek, Poke, Wait and Continue, direct execution of statements in the calculator mode, 10 nested machine language subroutines, multidimensional arrays and much more. And it uses only 7K of memory.

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1. Name of organization
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5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

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### Midland College

- **Odessa chapter:** Second Monday each month at 7:30 PM
- **Odessa chapter:** Second Saturday each month at 1 PM

### Permian Basin Computer Group

- **Data Processing Dept**
  - c/o Ector County Schools
  - POB 1912
  - Odessa TX 79760
- **Midland chapter:** Student Center,
Circle 142 on inquiry card.

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* ANSI Standard Fortran IV Compiler
  - Byte, Word, Real, Double, Complex, and String data types and operations.
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Clubs and Newsletters

Zips 90000 - 99999

1. Glendale College Computer Club
   2. 1500 N Verdugo Rd
      Glendale CA 91208
   3. Glendale College
   4. R Unterman
   5. (213) 240-1000 ext 200
   6. $2 per year

1. Compucolor-Intecolor Users Group
   2. 5250 Van Nuys Blvd
      Van Nuys CA 91401
   3. Same as above
   4. Bimonthly
   5. Stan Pro
   6. (213) 788-8850
   7. $15 first year
   8. Business programs; game programs; interfacing to other systems; special uses and interfaces to machines.

1. San Diego Computer Society
   2. POB 9988
      San Diego CA 92109
   3. Yes
   4. $4 membership donation; $6 newsletter subscription
   5. The San Diego Computer Society is a nonprofit, tax exempt corporation whose purpose is to provide its members and the general public with a useful source of computer related information.
   6. Write to above address for membership application.

1. Homebrew Computer Club
   2. POB 626
      Mountain View CA 94042
   3. Stanford Linear Accelerator Center and Sherman Fairchild Medical Center
   4. Printed in newsletter
   5. Homebrew Computer Club Newsletter
   6. Robert Reiling
   7. (415) 967-6754 after 7 PM
   8. Donation of $10 to $12 per year requested to pay meeting and newsletter costs.
   9. A sample Homebrew Computer Club Newsletter, listing meeting dates and location, may be obtained by sending an SASE to the Homebrew Computer Club Newsletter at the above address.

1. The Apple Core
   2. POB 4816
      Main Post Office
      San Francisco CA 94101
   3. Yes
   4. Scot Kamins
   5. To be determined
   6. To qualify as a member, you must own or regularly use an Apple in any memory configuration.


1. Bay Area Microprocessor Users Group (BAMUG)
2. 1211 Santa Clara Av
   Alameda CA 94501
3. 1450 53rd St, Emeryville CA
4. First Thursday of each month
5. Bay Area Microprocessor Users Group Newsletter
6. Timothy O'Hare
7. (415) 523-7396
8. Donations; no dues or fees required.
9. The club is open to all interested persons. It has an education forum every month with guest speakers to enlarge computer knowledge.
10. The club also has a software library, group buys on equipment and a swap meet at every meeting.

1. Diablo Professional Users Group
2. c/o R J Hendrickson
   321 Golf Club Rd
   Pleasant Hill CA 94523
3. Library conference room, Diablo Valley College
4. Fourth Wednesday of each month
5. Meeting minutes constitute the newsletter
6. R J Hendrickson
7. (415) 687-8373
8. None
9. Professional applications of personal computer systems. Meetings are comprised of speakers, demonstrations and random access sessions.

1. 6800 Computer Club
2. POB 18081
   San Jose CA 95158
3. University of Santa Clara
4. First Tuesday of each month
5. None
6. Ray Boz
7. (408) 269-9522
8. None
9. Everything on hardware and software for all 6800 systems.
10. For 6800 users we provide the place to exchange software, discuss problems, find solutions to problems, evaluate vendors, use limited

The listings follow this form:

1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

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<th>Directory, continued</th>
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<th>Disk wanted: Mini: 01 10 16 Maxi: Hard Soft System</th>
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</thead>
<tbody>
<tr>
<td>Please note name and address of store on separate sheet. MasterCharge and Visa OK. Give acct. # and exp. date.</td>
</tr>
</tbody>
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* We'll tip him to our Verbatim dealer program. Dealers: call 800·523·9350 for details.

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**HUNT NO MORE!**

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Program for disassembly of object code into source code for direct editing and re-assembly.

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- Reports number of bytes in source code file, number of external labels, number of local labels, and number of variables for computing memory space necessary to assembly source code generated.

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Circle 320 on inquiry card.
group buying power and exchange information on home computer news and events. We have a software library with programs on tape (KCS) at cost of reproduction and tape. All inquiries are answered when time permits.

**DIRECTORY, continued**

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Address</th>
<th>Type</th>
<th>Contact</th>
<th>Membership</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Sacramento Microcomputer Users Group (SMUG)</td>
<td>POB 161513 Sacramento CA 95816</td>
<td>Software Library</td>
<td>(916) 455-8071</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
<tr>
<td>2</td>
<td>SMUD Training Facilities, 59th St</td>
<td>Sacramento CA 95816</td>
<td>Workshops</td>
<td>(916) 455-8071</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
<tr>
<td>3</td>
<td>Push &amp; POP</td>
<td>Sacramento CA 95816</td>
<td>Workshops</td>
<td>(916) 455-8071</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
<tr>
<td>4</td>
<td>PET and SOL workshops</td>
<td>Sacramento CA 95816</td>
<td>Workshops</td>
<td>(916) 455-8071</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
</tbody>
</table>

**Please write SMUG at the address above with all meeting, membership and other questions.**

**1.** Sacramento Microcomputer Users Group (SMUG)
**2.** POB 161513
**3.** Sacramento CA 95816
**4.** Push & POP
**5.** POB 161513
**6.** Sacramento CA 95816

**Turn Your Computer Into a Teaching Machine**

The staff at Program Design did not learn about educational technology from a book—we wrote the book! We have been innovators in such teaching materials as programmed instruction and multimedia presentations. We also belong to that minority in education who actually test materials to see that people can learn from them.

Now Program Design brings this experience to the personal computer field. PDI is developing a line of educational and game programs for the whole family—from preschool child to adults.

Program Design educational software uses the computer’s full teaching potential in exciting and effective ways. Programs are simple to use and memory efficient, and most important...they teach!

**Tapes Now Available for the TRS-80, PET, Apple II**

**Sample our Software for $2.00.** Send us $2.00, your name, address, and type of computer, and we’ll send you a tape for your computer with actual samples of our programs.

Or circle our number on the reply card for a printed catalog.

**Directory continued**

<table>
<thead>
<tr>
<th>Name</th>
<th>Address</th>
<th>Type</th>
<th>Contact</th>
<th>Membership</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Portland Computer Society</td>
<td>4032 SE Grant C Portland OR 97214</td>
<td>Social: First Thursday of each month; Business: Third Wednesday and Saturday of each month.</td>
<td>(503) 227-0400</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
<tr>
<td>2. PCS7976</td>
<td>Percy G Wood</td>
<td>Social: First Thursday of each month; Business: Third Wednesday and Saturday of each month.</td>
<td>(503) 227-0400</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
<tr>
<td>3. Northwest Computer Society</td>
<td>POB 1943 Seattle WA 98104</td>
<td>Social: First Thursday of each month; Business: Third Wednesday and Saturday of each month.</td>
<td>(206) 224-9409</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
</tbody>
</table>

**Foreign and International Clubs and Newsletters**

<table>
<thead>
<tr>
<th>Name</th>
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<th>Type</th>
<th>Contact</th>
<th>Membership</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Anchorage Computer Group</td>
<td>364 H 6th St Ft Richardson AK 99505</td>
<td>Assistance to the novice home computerist.</td>
<td>(907) 453-7169</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
<tr>
<td>2. Apple Core Computer Club</td>
<td>220 N 2nd St #17 Yakima WA 98901</td>
<td>Assistance to the novice home computerist.</td>
<td>(509) 453-7169</td>
<td>Free</td>
<td>All inquiries answered when time permits.</td>
</tr>
</tbody>
</table>
1. KIM-1/6502 User Group
2. 109 Centre Av
   Norristown PA 19401
3. KIM-1/6502 User Notes
4. Eric C. Rehmke
7. (215) 631-9335
8. $5 for six issues
9. A communication medium for KIM users
10. Around 2000 members worldwide.

1. Buss
2. 325 Pennsylvania Av SE
   Washington DC 20003
3. none
6. Chazas Piotto, editor
8. $17 for 12 issues
9. Software and hardware compatible with H8, H11, or ET-3400.
10. Sample issue available upon request mentioning BYTE.

1. TRS-80 Users Group
2. 7554 Southgate Rd
   Fayetteville NC 28304
3. Our group is international so we do not have meetings.
5. TRS-80 Users Group Newsletter
6. R. Gordon Lloyd
7. (919) 867-5822
8. $10 per year (ten newsletters, 20 pages per issue)
9. Radio Shack TRS-80 computer, programs for the TRS-80, and interfacing the TRS-80 to the outside world.
10. SR-52 Users Club
2. 9459 Taylorsville Rd
   Dayton OH 45424
3. None
5. SR-52 Notes
6. Richard C. Vanderburgh
8. $1 per issue of SR-52 Notes; back issues start June 1976.
10. SR-52 Notes: style and technical level are aimed at individuals with above average intelligence and attention span, but whose formal education may have ended with high school. Scope is all of the Texas Instruments personal programmable calculators. Coverage of the TI-58/59 machines began June 1977. The SR-52 Users Club is a national/international group.

1. Personal Computing Society
2. c/o James White

The listings follow this form:
1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

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10. Other comments

---

1. **Boards DO Something**

If your system needs to know what time it is, our CL2400 is the board for you. The present time in hours, minutes, and seconds is always available for input, and is continuously updated by the highly accurate 60 Hz power line frequency. Need periodic interrupts? The CL2400 can do that, too, at any of 6 rates. Reference manual with BASIC and assembly language software examples included.

If your system needs on/off control of lights, motors, appliances, etc., our PC3200 System components are for you. Control boards allow one I/O port to control 32 (PC3232) or 16 (PC3216) external Power Control Units, such as the PC3202 which controls 120 VAC loads to 400 Watts. Optically isolated, low voltage, current-limited control lines are standard in this growing product line.

P.O. Box 516
La Canada, CA 91011
(213) 790-7957
---

1. **Having Reservations About Your Software?**

**HUNT NO MORE!**

Smoke Signal Broadcasting presents the

**SMART BUG**
A Cure For Mikbugitus

1024 byte monitor program for use with
MOTOROLA 6800 microprocessor

- The only monitor really MIKBUG compatible.
- Designed to replace the MIKBUG ROM used in many systems including the SWTPCo's 6800 microcomputer.
- TRACE feature allows user to single step through a program, examining the registers if desired.
- MIKBUG entry locations maintained, including most relatively obscure ones.
- Quick program debugging when the TRACE is used with BREAKPOINT.

Instruction Manual and Complete Source Listing...$19.50
SMARTBUG on 2708 including listing ...... $39.95
SMARTBUG on 2716 including listing ...... $49.95

---

1. **SMOKE SIGNAL BROADCASTING**

6304 Yucca/Hollywood, CA 90028/(213) 462-5652

---

**If your system needs to know what time it is, our CL2400 is the board for you. The present time in hours, minutes, and seconds is always available for input, and is continuously updated by the highly accurate 60 Hz power line frequency. Need periodic interrupts? The CL2400 can do that, too, at any of 6 rates. Reference manual with BASIC and assembly language software examples included.**

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Instruction Manual and Complete Source Listing...$19.50
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FULLY STATIC
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10 SLOT MAINFRAME
TT-10... KIT $325
10 SLOT TABLE TOP
MICROCOMPUTERS
TT-8080... KIT $440
SYSTEM WITH 16K & I/O
TT-8080-S. KIT $1050

CARD CAGE &
MOTHER BOARD
ECT-100.. KIT $100
CCMB-10.. KIT $75
WITH CONNECTORS
& GUIDES
ECT-100-F... KIT $200
CCMB-10-F... KIT $125

CPU, MEMORY
MOTHER BOARDS
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EXTENDER CARDS
POWER SUPPLIES

SHIPPING EXTRA
DEALER INQUIRIES INVITED

ELECTRONIC CONTROL TECHNOLOGY

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763 RAMSEY AVENUE
HILLSIDE, N. J. 07205

MAILING ADDRESS:
P. O. BOX 6
UNION, N. J. 07083

(201) 686-8080

1202 Riverview Ln
Watertown WI 53094
5. Soon to be announced
6. Richard A. Kuzmack
7. (703) 821-2873 (evenings)
9. The Society’s communications objectives will include publication of a newsletter for computer clubs and a club directory. Surveys will be conducted and published to share information on matters of interest to computer enthusiasts. PCS will foster the development of standards such as those necessary to the operation of a personal computer communications network.
10. This national organization was recently formed to facilitate non-commercial applications of computer technology. It will foster communication and coordination among the numerous computer clubs and individuals in the personal computing community. The board of directors of PCS are: Charles Floto, Washington DC; Richard Kuzmack, McLean VA; Sol Libes, Scotch Plains NJ; Larry Press, Santa Monica CA; Jim Rarus, Detroit MI; Robert Reiling, Mountain View CA; Gifford Toole, Mississauga, Ontario CANADA; M. D. Turner, Austin TX; and James White, Watertown WI.

the Mullen CB-1
Controller Board:
now only $88

People have used our original model CB-0 Controller Board for controlling audio systems, model railroads, time lapse photography, and dozens of other applications requiring intelligent, computer-controlled switching.

Our improved model CB-1 has all the features of its predecessor, 8 relays that respond to an 8 bit word for control purposes, 8 opto-isolators that accept input data for handshaking or further control purposes, full 5-100 buss compatibility, address selection switch, quality components and board, and so on.

But... the limited use (and expensive!) flat cable connector has been replaced with new connectors. These allow you to use pairs of wires of mixed gauges and lengths as needed. Also, a self-test feature is built on the board itself, and a new output design allows replacement of the relays with opto-isolators.

The best part is that you don’t pay a penny more for these new features. In fact, compared to the CB-0 price, you pay 2,900 pennies less. Available at computer stores nationwide, or by direct mail (mail orders shipped postpaid in USA; Californians and sales tax).

MULLEN COMPUTER BOARDS
BOX 6214, HAYWARD, CA 94545

1. Theater Computer Users Group
2. 104 N St Mary
Dallas TX 75214
3. Assorted conventions of other groups
(USITT, ATA)
4. Random
5. TCUG Newsletter
6. Mike Firth
7. (214) 827-7734
8. $4 per year
9. Uses of computers of any size, but particularly small ones, in any aspect of producing live drama, including lighting control, ticket management, bookkeeping, inventory, costing, research.
10. A national organization created to share data in a specific area.
change of information among small computer users.

1. Robot Builder
2. 208 Via Colorin
   Palos Verdes Estates CA 90274
3. none
5. Robot Builder
6. Michael Westvig
7. (213) 378-0580
8. $6 per year (bimonthly), $12 overseas, beginning with volume 2,
   number 1, January 1979.

1. Computer Information Organization Inc
2. POB 158
   San Luis Rey CA 92068
3. Publishing only
5. Radio Shack Computing, Low-Cost
   Word Processing and S-100 Bus
   Computer User Notes
6. Bill McLaughlin, editor
7. (714) 757-4849
8. Radio Shack $10 for 12 issues,
   S-100 $5 for six issues and Word
   Processing $12.95 for 12 issues
9. Real uses of computers: either
   business, home, education, small or
   large organization
10. Word Processing newsletter is
   developing interfaces to ordinary
   electric typewriters, to Selectric,
   Olivetti and other single element
   typewriters, to Friden and other
   special machines.

1. PPC
2. 2541 W Camden Pl
   Santa Ana CA 92704
5. PPC Journal
6. Richard J Nelson, publisher
8. $15 per year
9. To share programs, techniques,
   news, etc, for HP PPCs.
10. Six chapters at present: Cincinnati/
    Dayton, Chicago, Washington DC,
    Albuquerque, Orange County and
    NE Iowa Chapters. Nearly 2000
    members in 35 countries. Started
    June 1974. More information
    send 9 by 12 inch SASE (2 oz
    postage attached) to above
    address.

1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

Having Reservations About Your Software?
HUNT NO MORE!
Smoke Signal Broadcasting presents the
SA-1 SUPER ASSEMBLER

Uses Motorola Standard Mnemonics
for 6800 Microprocessor

• Input source code from file on Smoke Signal Broad-
  casting's BFD-68 disk system.
• Disk capability allows assembly of source code larger
  than available memory.
• Outputs object code to disk file.
• Assembly listings include alphabetized and tabulated
  symbol table.
• Complete source listing included.

Only $29.00 (on diskette)

We're the "CHIEF" in 6800 products software

SmoKE Signal BroadcASTING
6304 Yucca/Hollywood, CA 90028/(213) 462-5652

Circle 320 on inquiry card.
1. Calculator Lib: The Liberated Calculator Users Club
2. POB 2151
Oxnard CA 93034
3. Ventura County (we do not have a permanent meeting address yet)
4. Quarterly club activity report and the irregularly published newsletter
   Calculator Lib
5. Gene Hegedus
6. (805) 486-7191
7. Yearly membership dues of the non-profit club is $6 which includes the quarterly reports. The irregularly
   published newsletter Calculator Lib is $2.75 per issue postpaid.
8. This global club (with members on three continents) is the first to serve the interests of all calculator users,
   regardless of the make of their machines. It is dedicated to exploring the limits of the state of the art of
   calculator mathematical techniques.
9. The club presently is in a formative stage, having been organized on original 24 key keyboards of
   calculators mathematical techniques. It is dedicated to exploring the limits of the state of the art of
   calculator mathematical techniques.
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    calculators mathematical techniques. It is dedicated to exploring the limits of the state of the art of
    calculator mathematical techniques.

1. Computer Faire
2. POB 1579
Palo Alto CA 94302
3. Varies
4. Varies
5. Silicon Gulch Gazette (a randomly published 4 to 20 page newspaper)
6. Jim Warren
7. (415) 851-7075
8. None
9. Intelligent machines for home, business and industry
10. We maintain a cooperative but independent relationship with the manufacturer. Send $1 for sample
    issue of newsletter.

1. Ottawa Computer Group
2. POB 13218
Kanata Ontario
3. Microcomputers, peripherals and software among owners
4. First Monday of each month, 8 PM
5. OCG Newsletter
6. W Mitchell, secretary
7. (613) 596-2287
8. $5 per year and $5 initiation fee.
11. Association of Computer Experimenters (ACE)
12. c/o Ken Bevis, 220 Cherry Post Dr
Mississauga, Ontario
13. Hamilton, Ontario CANADA
14. Ipo Facto
15. Bernie Murphy, editor, 102 McCraney St, Oakville Ontario,
   CANADA L6H 1H6
16. Tentatively $10
17. Microcomputers, peripherals and software in general, with RCA-1802

P.E.T.™ PRODUCTS
SOFTWARE/ACCESSORIES/HARDWARE

Memory Expansion! 31.743 Bytes Free! NEECO now has internal memory
Expansion Boards Available for your PET! 16K, 24K and 32K Memory
Configurations. Call or write NEECO and ask for our "Free" Software and
Hardware Directory. Power up to 32K Bytes! Call NEECO for more info.

Software-NEECO has too many programs to list them all here! Call or
write and ask for our "Free" Directory! **Software Authors-NEECO offers
25% Royalties on PET programs with nationwide distribution! Call
NEECO for additional information on our 25% Royalty Program.

PET & Peripherals—NEECO offers last (off the shell?) delivery schedules
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excellent personal & Warranty service!!! Interested in a PET? Call and
request our P.E.T. Info Pak. Feel free to call and ask questions.

The Music Box: Music Composer and sound effects generator allows you
to compose and hear music on your PET! Program & Hardware allows
you to display notes, hear the notes, save pages of music on tape for later
playback or modification! The Music Box actually displays the notes as a
song or tune is played! Allows you to add sound effects to your own PET
Programs. Endless Possibilities! All Cassette Software, plug-in Hardware,
and Music Box instructions for only $49.95! Music Box Fits right inside
your PET! No assembly required! Music Box even plays random tunes!

NEECO Dust Cover: Protect your PET with our PET protective Dust Cover
& keyboard from dust that can, over time, cause intermittent chip failures!
Heavy, clear Plastic Dust Cover shows off your PET while protecting it from dust, spits, and those inevitable "Unwanted Sticky fingers!"
Manufactured to last as long as your PET—only $7.95

VISA OR MC Phone orders Accepted-4% Surcharge on Hardware

NEW ENGLAND ELECTRONICS CO.
248 Bridge Street
Springfield, Mass. 739-9626

142 September 1978 © BYTE Publications Inc.
Circle 281 on inquiry card.
microprocessor and software in particular.
9. The ACE club started in September 1977 and has about 450 members from across the US and Canada.

1. Toronto Region Association of Computer Enthusiasts (TRACE)
   POB 545, Streetsville, Ontario
   CANADA L5M 2C1
2. North Campus, Humber College,
   room J209 and Ontario Science Centre, lecture hall C
3. Fourth Friday of each month,
   8 PM and second Sunday of each month, 2 PM, respectively
4.  T RACE Newsletter
   Ross Cooling, president
   (416) 488-3314
5. $15 per year or $7 per year newsletter only.

1. Kitchener-Waterloo Microcomputer Club
   E2-3354 Electrical Engineering Dept, University of Waterloo
   Waterloo, Ontario
   CANADA N2L 3G1
2. Engineering 4, room 3388, University of Waterloo
3. First Wednesday of each month,
   7:30 PM
4. None
5. Roger K Sanderson
   (519) 579-6445 (home) or 885-1211 ext 3815 (work)
6. None
7. We hold very informal meetings for
   the purpose of getting people with similar interests together.
   We also have a small dedicated group of
   regulars who are doing interesting hardware and software development.

1. West Coast Computer Society
   POB 4476
   Vancouver BC
   CANADA
2. British Columbia Institute of Technology, room D412
3. First Wednesday of each month at
   8 PM (no meetings July and August)
4. Print Out
5. Peter Luckham
6. (604) 522-3484
7. $15 per year
8. None

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<tr>
<td>5. Newsletter or publication</td>
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<td>6. Contact person</td>
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<td>7. Contact phone number</td>
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<tr>
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</table>

LSI-11 TIME

It's TIME you brought your LSI-11 up to DATE, TIME and DATE, two important parameters in the computer world, are available to your LSI-11 on one DUAL SIZE BOARD. When requested, the TCU-50D will present you with the date (month and day), time (hour and minutes), and seconds. Turn your computer off and forget about the time — your battery supported TCU-50D won't, not for 3 months anyway. The correct date and time will be there when you power up.

The TCU-50D is shipped preset to your local time, but can be set to any time you want by a simple software routine.

AT $295
YOU CAN'T AFFORD TO IGNORE TIME

Time is only one way we can help you upgrade your LSI-11 or PDP-11 system. We'd also like to tell you about the others. So contact Digital Pathways if you're into -11's. We are too.

Digital Pathways Inc.
4151 Middlefield Road • Palo Alto, California 94306 • Telephone (415) 493-5544

Having Reservations About Your Software?

HUNT NO MORE!

Smoke Signal Broadcasting presents the

SG-1 SOURCE GENERATOR

Program for disassembly of object code into source code for direct editing and re-assembly.

- Output directed to tape or disk with either SWTPCo's co-resident assembler format, or Smoke Signal Broadcasting's Text Editing System format.
- Reports number of bytes in source code file, number of external labels, number of local labels, and number of variables for computing memory space necessary to assemble source code generated.

Only $24.95 (on cassette), $30.95 (on diskette)

We're the "CHIEF" in 6800 products software

Smoke Signal Broadcasting
6304 Yucca/Hollywood, CA 90028/(213) 462-5652

Circle 320 on inquiry card.

September 1978 © BYTE Publications Inc 143
ENTREPRENEURS

If you can program a main and own one, you may have almost everything to start your own systems house. Find out how, from this detailed manual by an EDP professional who successfully did it.

HOW TO START YOUR OWN SYSTEMS HOUSE
by Leslie Nelson
213 pages $36.00

HANDBOOK OF SMALL BUSINESS COMPUTER CONSULTANTS
Practical guide for programmers, accountants, engineers to become an independent SBC consultant. Systematic coverage of technical, marketing, financial and legal aspects.
196 pages $28.00

COMING TO ATLANTA IN OCTOBER
Plan To Exhibit:

<table>
<thead>
<tr>
<th>Name</th>
<th>Contact</th>
</tr>
</thead>
<tbody>
<tr>
<td>BizComp '78</td>
<td>Marriott Motor Hotel, Atlanta, Georgia</td>
</tr>
</tbody>
</table>

CROWDS. EXPOSURE. SALES.
Atlanta, The Computer City Of The South...

BizComp '78, The Reason For Being There!

Plan To Exhibit: Reserve Space Now!
BizComp '78 will highlight the relatively small but potentially important role computers can play in the independent business sector. A special computer house exhibit will feature new products, software, services and supplies. BizComp '78 will also be the first national forum for the small computer industry.

Plan To Attend: Daily Seminars!
At the door registration will be $2.00 per day. Reservations are $1.00 per day. Reservations will be honored at the door. Registration will expire October 20th. Wives attending for the first time are welcome. A limited number of tickets per day. All tickets must be non-cancelable. Early registration will secure a special copy of the Expo directory. Tickets will be mailed to the address on your order.

For Complete Details Write Or Call Today!

Felsburg Associates, Inc.
12033 Harlan Lane—P.O. Box 735
Bowie, Maryland 20715
(301) 262-0303

Circles 133 on inquiry card.

Turning Points Publishing Company

Clubs and Newsletters

1. Microcomputer Encounter Group
2. 207-885 Old Esquimalt Rd Victoria BC CANADA V9A 4W9
3. Varghese Cherian, secretary
4. Exchanging information and ideas.

1. Amateur Computer Club
2. 7 Dordells Basildon, Essex ENGLAND
3. Six times a year
4. Mike Lord
5. (0268) 411125
6. £ 2 PA or $4 (US currency)

1. Hobby Computer Club
2. Delftseka de 12
2266 A Leidschendam NETHERLANDS
3. Several towns in Belgium and the Netherlands.
4. Usually once each month
5. Hobby Computer Club Nieuwsbrief (Dutch), bimonthly
6. Dick Barnhoorns
7. Netherlands 070-273537
8. Netherlands: 15 Guilders; Belgium: 225 Franc
9. No bias to any system or microprocessor
10. Membership passed 800 in May 1978. Hardware service (cheap parts and reductions) and software library started in January 1978. HCC Computer Day in October. We’re taking part in several large scale exhibitions to promote the concept of personal computing.

1. Japan Microcomputer Club
2. Kikashinko-kalman, JEIDA 5-5-8, Shibakoen, Minato-ku Tokyo JAPAN
3. Same as above
4. Twice a month
5. Micom (Japanese version), Miccom Circular (Japanese version), Micro Computer News (English version)
6. Koji Yada, editor
7. 03-438-1869
8. ¥6,000 per year
9. All aspects of hobbyist computers for persons in Japan.

The listings follow this form:

1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

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1. Name of organization
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7. Contact phone number
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9. Special interests
10. Other comments
At first it might seem odd to review the *8080 Programmer's Pocket Guide* and the *8080 Hex Code Card* at the same time, but they both serve as quick references for 8080 assembler programming and hand assembly of the resulting programs. Either one alone is a great improvement over thumbing through the appendices of larger books; ideally you should have both.

The *8080 Programmer's Pocket Guide* is a small booklet (4.5 by 3.5 inches, 11.5 by 9 cm) intended as a quick reference to the 8080 instruction set. It has three sections. The first is a discussion of each instruction in the set describing what it does, what flags
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**6800 SOFTWARE**

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it affects, and the octal and hexadecimal values for it. The second part is a discussion of a program for loading Intel hexadecimal format paper tapes. The third section is a summary of the instruction set ordered by function. This gives the instruction, its octal and hexadecimal values, the number of cycle states, and the page on which the instruction is discussed.

I find this booklet very useful. There is, however, one minor blemish that may confuse some users. Parts of the booklet are adapted from Scelbi's *8080 Software Gourmet Guide and Cookbook*. This cookbook, like previous Scelbi publications, uses a set of mnemonics which were based on those for the 8008. Scelbi has since changed over to the standard Intel 8080 mnemonics, and they use the standard ones throughout the pocket guide. However, some of the discussions taken from the previous book still use the old mnemonics (eg: LBA rather than MOV B, A). Also, the text occasionally refers to appendices from the cookbook. But these are minor problems; the booklet is well worth having.

Tychon's 8080 Hex Code Card (15 by 8 cm) is a slide rule type summary of the 8080 instruction set. Also available is a card for those who prefer octal. The front of the card gives all the instructions and their hexadecimal values, and tells how each instruction affects the flags. The back of the card gives an ASCII chart, a hexadecimal to binary conversion chart, a chart of the register pairs, and one of the flag byte. The card itself is made of fairly heavyweight cardboard. If Tychon ever puts a plastic card out I'll be among the first to buy it, since the present card is used so much that I may wear it out. If you ever hand assemble programs for the 8080, I highly recommend this card.

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We have been using the Heathkit LSI-11 computer as supplied with their model H9 CRT terminal and recently ran into an interesting problem. Source programs that included lower case alphabetical ASCII characters would not read out on the terminal in an intelligible way; the 64 character generator just went bananas and interpreted these lower case characters as slashes, percent signs, etc.

I have also noted that some other devices, such as the Practical Automation DMTP-6-Up Printer, also use 64 character sets, and may be faced with the same problem.

The Heath terminal is easily modified so that both upper and lower case alphabetical characters read out as upper case. (Some form of this modification may also work with the above printer.)

Heath feeds the character generator chip, IC205, with a 6 bit signal latched through from the ASCII bus. The most significant data line is latched onto the character generator board but not run to IC205. A bit of study will show that changing the drive to the most significant bit of IC205 from ASCII bus line 6 to an inverted ASCII bus line 7 will cause the character generator to recognize lower case and upper case alpha characters as upper case (Tektronix uses this trick in their display terminals).

The modification is easily done by cutting the run from pin 15 of IC203 (bit 6) to pin 1 of IC206, soldering in a wire from pin 10 of IC203 (bit 7) to pin 11 of IC219, and soldering in another wire from pin 10 of IC219 to pin 1 of IC206. IC219 is a hexadecimal inverter, and the pins 10 and 11 are the output and input of an unused section of this IC.
Continued from page 65

Figure 3, continued: Notice that some of the diagrams, for example FACTOR, contain themselves in their own definitions. This is known as a recursive definition.

For instance:

\[
\text{mem}[i] = \text{mem}[j];
\]

reads the byte from the memory location \( j \) and writes it back to memory location \( i \). Machine language subroutines can be called from Pascal programs. The statement:

\[
\text{Call } (i);
\]

can be used to make a call to memory address \( i \).

The P-Machine

The p-machine is a stack oriented machine consisting of four registers and two memory storage areas. Memory is separated into program storage and data storage areas. The program storage area contains the program codes (p-codes), and remains unchanged during program execution. The data storage area contains the values of variables. It is also used to store temporary values during arithmetical and logical operations.

Though the variables can be fetched and stored in a random fashion, the data storage area operates as a stack with respect to arithmetical and logical operations and runtime storage allocation. Arithmetical and logical operations are done on the top elements of the stack, and the results of the operations are pushed back on the stack. In this respect, one might call it a zero address machine, since operations (except store and load instructions, which must specify an address) are done without reference to any address. Later we will discuss the use of the stack during runtime storage allocation.
The four registers in the p-machine are the program counter, P, which points to the next executable instruction in the program storage; the instruction register, I, which contains the current execution instruction; the stack pointer, T, which points to the top of the stack, and the base address register, B, which contains the current base address. The functions of the first three registers should be quite clear from the above discussion. The function of register B will become clear after we discuss storage allocation.

Each variable in a Pascal procedure has a scope and lifetime. The scope of a variable is the range within which it can be referenced. The scope of a Pascal variable is simply the procedure block to which it belongs. The lifetime of a variable is from the time storage is allocated for it to the time storage is disallocated. In Pascal, this is the time the procedure defining the variable is activated to the time a return is executed by the procedure. This is different from the way variables are treated in BASIC, where the scope of a variable is the entire program and its lifetime the entire execution time.
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Since procedure activation is strictly a first in, last out process, the use of stack is an appropriate strategy. When a procedure is activated, storage for its local variables is allocated on the top of the stack, and is disallocated when the procedure is terminated. Thus the stack contains all the variables of the currently active procedures. The variables of the last activated procedure are on the top of the stack, those of the second to last activated procedure next to it, and so on.

Since storage allocation is not static, addresses cannot be assigned at compile time, but must be calculated at runtime. The base register, B, always points to the starting location of the segment of the data block in the stack. The addresses generated by the compiler are not absolute addresses, but displacements from some base addresses. If the variable is local, then its address is the displacement from the current base register B; but if the variable is from an outer procedure, then the base address for that procedure should be calculated, and added to the displacement.

To do this, and to ensure proper procedure or function linkage, extra storage is allocated on the stack when a procedure is activated. Figure 4 shows the various quantities present in each of the procedure blocks. The function return value is used only for function calls, and storage is allocated for any parameters needed by the procedure or function. The base address contains the value of the current base register B, and the return address contains the program return address at the place of the call. The functions of the dynamic linkage and the static linkage need further explanation.

The dynamic linkage forms a chain that reflects the procedure activation history. It points back to the base address of the procedure that was activated immediately before this one. For instance, if procedure A calls procedure B, which calls procedure C, then the dynamic link chain points from C to B, and then to A. It is used to ensure that the program returns to its previous state when exiting a procedure. In particular, the base register B must be loaded with the correct base address of the calling procedure. This would be easy to do if we follow a step through the dynamic link chain.

The static link, on the other hand, reflects the static hierarchical structure of the procedures. Each active procedure has a link that points to the procedure (also active) that immediately contains it. The static links actually form a tree, with the
main program block as the root. These links, which in general are different from the dynamic links, are used to let programs have access to the correct base address of the variables in an outer procedure, since at compiler time, only the static relationship among the procedures are known. The compiler therefore generates the pair (static level difference, relative displacement from the base address) as addresses for variables. The calculation of the addresses from these pairs would presumably slow down the process, but it is a small price to pay for nice features like recursive procedure calls.

Figure 4: A typical activation record for a function. For a procedure, the function return value is omitted. Note that the procedure and function parameters, as well as the function return value, are below the base register B, and thus would have negative displacements.

Table 1: Basic p-codes. The \( v \) in call, load and store instructions is the difference in static level between the current procedure and the one being called or the one which contains the variable from the base address. An address in a p-code program is shown by \( a \). The condition code, \( c \), can either be 0 or 1.
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The P-Codes

The p-machine has only 11 basic instructions, which are listed in table 1. For the sake of simplicity and easy handling in this version of the implementation, all instructions are four bytes long. The contents of the four bytes are as follows:

- byte 1: op — the operation code.
- byte 2: can be (i) v — static level difference.
- or (ii) c - condition code in a jump instruction.
- or (iii) 255 — denotes absolute addressing.
- or (iv) not used for some instructions.
- bytes 3,4: can be (i) d — displacement from the base address.
- or (ii) n — numeric constant.
- or (iii) a — address in the p-code program.

The OPR (arithmetic and logical operations) and CSP (call standard procedure) are further subdivided into more instructions.

The complete set of instruction mnemonics and operations is listed in table 2. The LODX and STOX instructions are used to load and store array elements with the value of the array subscript on top of the stack.

The call standard procedure (CSP) instruction is primarily used for input and output (I/O) operations. Besides the basic function of inputting and outputting single characters, additional procedures have been implemented to relieve the user from writing I/O conversion routines in Pascal for numeric and hexadecimal numbers. In the future, more procedures can be added to handle the input and output of other data types such as floating point numbers and file records for tape or disk. Meanwhile these seven instructions are sufficient for convenient use in writing the bootstrap compiler and its related software.

Readers are urged to read the p-code interpreter listing which simulates the operations of the p-machine. The program statements are straightforward and self-explanatory. Familiarity with the p-machine instruction set is essential in understanding the code generation part of the p-compiler.

The P-Code Interpreter

Since the p-machine is a hypothetical computer, there has to be some method of executing the p-codes generated by the compiler. There are two simple solutions to this problem. One is to write an interpreter which can decode and execute the p-codes. The other solution is to write a trans-
The p-code interpreter is made up of two major modules:

- Main program.
- Procedure which simulates the p-machine.

Every call to the simulator will execute one p-machine instruction. Each p-machine instruction cycle can be divided into four stages:

- Fetch a p-code from memory.
- Increment the program counter.
- Decode the instruction.
- Execute the instruction.

Several global variables are used to hold the values of the p-machine registers such as program counter, stack pointer, current instruction, etc. A one-dimensional array represents the data stack. Functional operations of the various p-machine instructions are coded directly from the instruction set defined in Table 2. The main program simply initializes the program counter to zero and then calls the simulator repeatedly to simulate machine execution. This sounds simple but not useful, because the user has no control of the program during execution until it terminates.

In order to enable user control of an executing p-code program, the main program must accept commands from the user which instruct it to call the simulator a specified number of times. The simulator must be able to perform the following operations:

- Fetch a p-code from memory.
- Increment the program counter.
- Decode the instruction.
- Execute the instruction.

Table 3: Interpreter commands. All commands for the p-code interpreter are single characters. A command is entered after the interpreter prompts the user with a > on the video display. Additional information is needed for some commands such as breakpoint and stack addresses. On entry to the interpreter it will ask for the starting memory address of p-codes and initialize the program counter to zero. On exit it will display the number of p-codes executed.

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>LIT 0, n</td>
<td>load literal constant</td>
</tr>
<tr>
<td>OPR 0, 1</td>
<td>negate (sp)</td>
</tr>
<tr>
<td>OPR 0, 2</td>
<td>add (sp) to (sp-1)</td>
</tr>
<tr>
<td>OPR 0, 3</td>
<td>subtract (sp) from (sp-1)</td>
</tr>
<tr>
<td>OPR 0, 4</td>
<td>multiply (sp-1) by (sp)</td>
</tr>
<tr>
<td>OPR 0, 5</td>
<td>divide (sp-1) by (sp)</td>
</tr>
<tr>
<td>OPR 0, 6</td>
<td>low order bit of (sp)</td>
</tr>
<tr>
<td>OPR 0, 7</td>
<td>(sp-1) modulo (sp)</td>
</tr>
<tr>
<td>OPR 0, 8</td>
<td>test for (sp-1)&lt;(sp)</td>
</tr>
<tr>
<td>OPR 0, 9</td>
<td>test for (sp-1)&lt;(sp)</td>
</tr>
<tr>
<td>OPR 0, 10</td>
<td>test for (sp-1)&lt;(sp)</td>
</tr>
<tr>
<td>OPR 0, 11</td>
<td>test for (sp-1)&lt;(sp)</td>
</tr>
<tr>
<td>OPR 0, 12</td>
<td>test for (sp-1)&lt;(sp)</td>
</tr>
<tr>
<td>OPR 0, 13</td>
<td>test for (sp-1)&lt;(sp)</td>
</tr>
<tr>
<td>OPR 0, 14</td>
<td>logical (sp-1) OR (sp)</td>
</tr>
<tr>
<td>OPR 0, 15</td>
<td>logical (sp-1) AND (sp)</td>
</tr>
<tr>
<td>OPR 0, 16</td>
<td>logical NOT of (sp)</td>
</tr>
<tr>
<td>OPR 0, 17</td>
<td>shift left logical</td>
</tr>
<tr>
<td>OPR 0, 18</td>
<td>shift right logical</td>
</tr>
<tr>
<td>OPR 0, 19</td>
<td>increment (sp) by 1</td>
</tr>
<tr>
<td>OPR 0, 20</td>
<td>decrement (sp) by 1</td>
</tr>
<tr>
<td>OPR 0, 21</td>
<td>copy (sp) to (sp-1)</td>
</tr>
<tr>
<td>LOD v,d</td>
<td>load a word</td>
</tr>
<tr>
<td>LODX v,d</td>
<td>load a word with index address (sp)</td>
</tr>
<tr>
<td>STO v,d</td>
<td>store a word</td>
</tr>
<tr>
<td>STO v,d</td>
<td>store a word with index address (sp)</td>
</tr>
<tr>
<td>CAL v,a</td>
<td>procedure call</td>
</tr>
<tr>
<td>CAL 255,0</td>
<td>call procedure at absolute address (sp)</td>
</tr>
<tr>
<td>INT n</td>
<td>increment sp by n</td>
</tr>
<tr>
<td>JMP a</td>
<td>jump to location a</td>
</tr>
<tr>
<td>JPC a</td>
<td>jump to location a if low order bit (sp)&lt;0</td>
</tr>
<tr>
<td>JPC a</td>
<td>jump to location a if low order bit (sp)&gt;0</td>
</tr>
<tr>
<td>CSP 0,0</td>
<td>output 1 character</td>
</tr>
<tr>
<td>CSP 0,1</td>
<td>output 1 character</td>
</tr>
<tr>
<td>CSP 0,2</td>
<td>output an integer</td>
</tr>
<tr>
<td>CSP 0,3</td>
<td>output an integer</td>
</tr>
<tr>
<td>CSP 0,4</td>
<td>input a hexadecimal number</td>
</tr>
<tr>
<td>CSP 0,5</td>
<td>output a hexadecimal number</td>
</tr>
<tr>
<td>CSP 0,6</td>
<td>output a string</td>
</tr>
</tbody>
</table>

Table 2: The p-machine instruction set. The stack pointer, sp, points to the top element of the stack. The content of the stack element is represented by (sp). The operands of the OPR instructions are replaced by their results on the stack. The result of the six relational operations is l if the test is true and 0 if false. With the exception of single operand OPR instructions, all instructions adjust the stack pointer, sp, after execution.
North Star BASIC

A brief summary of North Star BASIC (version 6, release 3) is given for readers not familiar with its particular features.

Variable names are one or two characters long; an alphabetical character followed optionally by a decimal digit. There are four types of variables: numeric, string, array of numeric, and function. The string variables are names postfixed by an underscore, while function names are prefixed by FN. Functions (and their parameters) are defined by the declaration DEF, and ended by FNEND (for multiline function). The parameters in the function definition are local to the function, and would not affect variables in the calling program.

Strings cannot be dimensioned. The DIM declarations for strings Declare the maximum length of the string variables, not their dimensions. The notation A$[3, 5] denotes the substring of A$ from position 3 to 5. Thus if A$ = ABCDEFG, A$[3, 5] is the string CDE. This substring expression can be used both on the left and right hand side of an assignment statement.

Multiple statement lines are allowed. Statements within a line are separated by either colons, :, or back slashes, \.

Absolute memory locations can be accessed from BASIC programs. The function EXAM(I) returns the content of memory at address I; and the instruction "FNAME" assigns disk file "FNAME" to file unit #0. A subsequent READ of #0 as reads A$ from the disk file, and a WRITE of #0 as writes A$ to the disk file. A built-in function TYP can be used to check the type of data to be read.

Absolute memory locations can be accessed from BAS IC programs. The program logic is very similar to the BASIC version. Since the program was written in BASIC. While developing the p-compiler, different constructs of Pascal statements were tested one at a time using the interpreter to verify the correctness of the p-codes generated. After the compiler was debugged, the interpreter was rewritten in Pascal. The program logic is very similar to the BASIC version. Since the program number of times or to display register and stack contents. This is the simple idea of a debugging interpreter. The debugging aids commonly known include single step execution, set and reset of breakpoints, and display of register and stack contents. A number of these debugging facilities have been incorporated in the p-code interpreter. Table 3 shows the 13 interpreter commands and their functions. Note that the trace command is particularly useful in analyzing mysterious flow of a program, such as discovering the path along which a breakpoint is reached. This command is more convenient to use and much faster than single step execution. The limits on the number of breakpoints and the number of instructions traced can be changed easily in the program.

The first version of the p-code interpreter was written in BASIC. While developing the p-compiler, different constructs of Pascal statements were tested one at a time using the interpreter to verify the correctness of the p-codes generated. After the compiler was debugged, the interpreter was rewritten in Pascal. The program logic is very similar to the BASIC version. Since the program

Listing 1: Pascal source code for the p-code interpreter as output by the authors' system. This version implements all of the commands in table 3.
structure of the Pascal version is neat and highly readable, the debugging time is minimal. The Pascal source program is shown in listing 1. The program design is rather straightforward. Readers with some programming experience in any high level language should be able to read and understand it without the help of a flowchart or further explanation on program logic. Note that in the main program and procedure exec, the case...of statement is put to good use. In the BASIC version the interpreter commands have to be tested within a FOR loop by comparing the input character with a string array, and then an ON..GOTO statement is used to branch to various parts of the program.

It must be emphasized again that the interpreter executes p-codes and not Pascal statements. Therefore the user is required to know some knowledge of the p-machine and p-codes. In addition to this, the p-compiler should be instructed to list p-codes together with Pascal program statements during compilation. They will be cross-referenced when running the interpreter. Obviously this procedure is not as convenient and easy to use as an ordinary BASIC interpreter, but still it provides the only way for debugging Pascal programs in our present version. A new debugging scheme is being planned for the future which will enable the user to debug programs at the Pascal statement level. This means the user may refer to variables and arrays and statements rather than stack contents and p-code addresses. Part 2 will go into details of the design and implementation of the p-compiler.
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One definition of graphics might be "a means to convert data into information." Our computers create printed data at a great rate, but all this data is not information until it conveys to a person some trend or fact about the world we live in. A small part of graphics is the conversion of data representing the position in space of the surface of an object into a three-dimensional picture of that object. The picture may be useful for itself as computer art, or it may help understand something about the object.

Imagine looking down the length of a pencil, using only one eye. With the eraser held away from the viewer, the pencil appears as a polygon with a dark place in the center where the lead is. The length of the pencil and the eraser are invisible. Now imagine the pencil rotated about its point until it is pointed toward the viewer's shoulder. The length of the pencil and the eraser are now visible, and appear in the form of translations to the side and up of the surface of the pencil. The relation between the position of a point on the pencil, specified in three dimensions X, Y, and Z, and the apparent translation of that point as the pencil is rotated is expressed by standard equations. These can be written in an organized fashion using matrices. These matrices are called coordinate transform matrices. They are powerful tools because they separate the mathematics associated with the angle of observation from the data describing the surface of an object. The small computers available today make it easy to convert surface data to pictorial information using matrices. This article will show how.

Definitions

The Cartesian coordinate system will be used in this discussion. On a computer graphic screen, X is the horizontal dimension, Y is defined as the vertical dimension, and Z is depth into the screen. Positive values are to the right, up, and away from the viewer. The origin will usually be in the center of the screen. A plane is described by any two axes. Thus, the X,Y plane is the surface of the computer screen, the Y,Z plane is seen edge on as the Y axis, and the X,Z plane is seen edge on as the X axis.

An equation which does not specifically include a particular coordinate direction will be interpreted to mean that the described line or point may exist anywhere along the unmentioned axis. Thus, X=1 represents the entire Y,Z plane located at 1 along the X axis. The line defined by Y=X may exist anywhere along the Z axis; therefore this equation defines a plane tilted 45 degrees from the horizontal, seen edge on at Z equal to zero on the computer screen. A surface may be made parallel to an axis by omitting that axis, as above, or may be specified at all values of X, Y and Z. Thus, Y=X+Z is a surface defined for all space.

Two kinds of matrices will be used here. The first kind is a matrix which represents the coordinates of a point in space, described by X, Y and Z. This matrix, P, is a column matrix, with one column and three rows as shown in figure 1. It will be used to hold the values for a point on the surface, both before and after transformation. All drawing commands will use the X and Y from this matrix.

The second kind of matrix contains the standard equations which relate the transformed values for X, Y and Z to the original values. This matrix, C, has three rows and three columns. The numbers at each position in this matrix are derived from the standard equations for some specific coordinate transformation type, such as a rotation. If the angle of observation of the object is arrived at by two successive operations, such as a rotation in each of two planes, then the matrix, C, which controls this view may have numbers in it that are derived from two matrix equations. The procedure which produces a single matrix combining several operations is called matrix multiplication. Matrix multiplication is used both to produce the particular numbers in the 3 by 3 matrix, C, which describe a point of observation, and then to apply those numbers to derive a transformed 3 by 1 matrix, P, which gives the apparent position of some part of the object's surface.

Computing Procedure

Given the ability to do matrix multiplication (the details will be presented below),
the sequence of operations to produce a three-dimensional picture of an object is short and easily stated:

1. Generate an array of data consisting of the X, Y and Z coordinates of the object to be drawn. This may be either computed as the drawing progresses, or done all at once and stored. The latter way is faster if the viewpoint is to be adjusted to find the most pleasing picture.

2. Define the viewpoint. For this part, a matrix is generated for each motion required to arrive at the desired point of view. The matrices are then multiplied together to produce a single 3 by 3 matrix to be used in the main routine. The order of multiplication may be important.

3. Write a program to draw the object in its untransformed state. This will be a sequence of commands which move the graphic cursor to a spot on the object at the beginning of an edge or other feature, then draw (move leaving a line behind) to another spot on the object. Specify the move and draw coordinates in terms of a column matrix element rather than X, Y and Z. Define the elements at each spot by using each of the points in the array.

4. When the untransformed picture is accurate and understood, then the picture is reoriented by simply inserting a matrix multiplication between the specification of each column matrix and the associated graphic command. The original X, Y, Z coordinates of the spot on the object are thereby transformed into a new set of X, Y, Z numbers representing the spot seen from the new viewpoint. Each set of coordinates from step 1 is multiplied by the matrix generated in step 2.

4a. An alternate method is to do all the transformations at once, changing all the X, Y and Z points in the array formed in step 1 into transformed X, Y and Z numbers in the same array. Since the computer screen is really only two-dimensional, only the X and Y elements are used in step 3. After transformation, these numbers are shifted about and contain depth information. The drawing made in this fashion is a projected view rather than a three-dimensional drawing. The difference is that in the projected view all lines converge at infinity along the Z axis. The difference is minor. The observer perceives a three-dimensional picture in most cases; the projected view in some figures is perceived either as having relief or depth without the visual clue of lines meeting at infinity. This leads to some interesting optical illusions using projected views.

The rest of this article discusses some of the transformations available and shows the pictorial results of each.

---

### Matrix Multiplication

**What information is necessary to write a subroutine to perform the matrix transformations described in this article?** The general theory of matrix algebra and its interpretation is beyond the scope of this discussion. For more information and a very clear description of many other uses for matrices, the reader is referred to *The Mathematics of Matrices* by Philip J. Davis. Here are some brief notes on the subject:

Two aspects of matrices are important in matrix multiplication.

These are the order of the matrices being multiplied (which one comes first), and the shape of each matrix. The elements in the output matrix resulting from a multiplication of two matrices are each formed by combining numbers in the columns of the first matrix and rows of the second matrix, done in a standard order. All the necessary rows and columns have to exist for the output to exist. Thus, some matrices may be multiplied in one order, but not in the opposite order. The rule is: the number of columns of the first matrix must equal the number of rows of the second matrix.

In table 1, the two matrices may be multiplied in the order (C) (P) but not in the order (P) (C). The result of multiplying (C) (P) is a new column matrix P. A mathematician would say that two matrices are “conformable for multiplication” when the order and shape requirements are met. He would also say “(C) is multiplied by (P)” here. The requirement for conformability leaves one dimension of the shape of each matrix unrestricted. The unrestricted dimensions establish the shape of the output matrix. Tables 1 and 2 summarize the necessary arithmetic. The elements in (C) are numbers, which are each computed in various ways depending upon the desired transformation.

![Matrix Multiplication Formula](https://example.com/matrix_multiplication.png)

**Table 1: Matrix multiplication format.**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>J</th>
<th>K</th>
<th>L</th>
<th>M</th>
<th>N</th>
<th>O</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>E</td>
<td>F</td>
<td>P</td>
<td>Q</td>
<td>R</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[
A' = (A * B + C * D + E * F + G)
\]

**Table 2: 3 by 3 matrix multiplication format.**

<table>
<thead>
<tr>
<th>A'</th>
<th>B'</th>
<th>C'</th>
</tr>
</thead>
<tbody>
<tr>
<td>D'</td>
<td>E'</td>
<td>F'</td>
</tr>
<tr>
<td>G'</td>
<td>H'</td>
<td>I'</td>
</tr>
</tbody>
</table>
Types of Transformations

The operations possible using coordinate transform matrices are not limited to shifting and rotating the picture. A number of more drastic changes may be made to the picture. Some of these changes are: magnification, shear, stretching in one direction, and mapping onto a surface.

The following figures and tables show examples of several coordinate transform operations. Each operation is represented by the matrix, the equations for the output matrix elements, and a figure to show how a picture of a well-known object is changed by the operation.

Unit Matrix

Table 3 shows the unit matrix. This transformation reproduces the picture of the object in its original view as defined above. Figure 2 shows a side view of a coffee cup.

\[
\begin{pmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1
\end{pmatrix}
\]

Table 3: The unit matrix.

Figure 2: The standard view (untransformed).

\[
\begin{pmatrix}
X' = (X*1+Y*0+Z*0) \\
Y' = (X*0+Y*1+Z*0) \\
Z' = (X*0+Y*0+Z*1)
\end{pmatrix}
\]

Table 4: Expansion along the Y axis by a factor K.
Scaling

The object may be defined with some shape which is not quite the final version, but which uses easily verified dimensions. Thus, in our example, the height is equal to the diameter, and the square outline in figure 2 quickly shows that the array of data defining the cup is correct in the X and Y dimensions.

Selective magnification along any axis may be used to alter the proportions of the object to a shape that may be nearer that required by the user. Thus, table 4 and figure 3 are appropriate for users with large capacities; table 5 and figure 4 produce a cup for those with wide mouths, while table 6 and figure 6 produce a cup which could be used for filling a pie plate with whipped cream.

If the proportions are correct but the user wants to create several different sizes, table 7 will allow the same magnification to take place along all the axes. One such magnified cup is shown in figure 5.

![Figure 3: Expanded along the Y axis by a factor of 1.5.](image)

![Figure 4: Expanded along the X axis by a factor of 1.5.](image)

![Figure 5: Magnified by a factor of 0.5.](image)

![Figure 6: Rotated 90 degrees and expanded along Z axis by a factor of 1.5.](image)
Shear

The object in its original shape may be boring and conventional in shape and lack individuality. This failing may be rectified as in table 8 and figure 7. To shear the object, the position of a point on the object is displaced from its original position by a function of the point's position along an orthogonal axis. These figures displace the points upward by a value equal to half the horizontal distance to each point.

Table 9 and figures 8 and 9 show shears along the horizontal axis. Figure 9 shows the same object as figure 8 rotated 90° to illustrate that the third axis is unchanged by this operation. As in the other operations, shears along all axes may be combined.

| 1 0 0 |
| K 1 0 |
| 0 0 1 |

\[ X' = (X'1+Y'0+Z'0) \]
\[ Y' = (X'K+Y'1+Z'0) \]
\[ Z' = (X'O+Y'0+Z'1) \]

Table 8: Shear along the Y axis in the X, Y plane by a factor K.

| 1 K 0 |
| 0 1 0 |
| 0 0 1 |

\[ X' = (X'1+Y'K+Z'0) \]
\[ Y' = (X'O+Y'1+Z'0) \]
\[ Z' = (X'O+Y'0+Z'1) \]

Table 9: Shear along the X axis in the X, Y plane by a factor K.

Rotations

The object may be reoriented in space by rotating it about any axis. A particular angle of view may be arrived at by some sequence of rotations about each axis. This is easily accomplished using the matrices in the following tables.

A point of confusion occurs when using rotations. The order of multiplication of the matrices (or the order of applying the operations to the object) is important. The axes remain associated with the object, not the screen. This means, for instance, that if the rotation in the X, Y plane shown in table 10 is applied first to the object, then subsequent rotations in the other planes happen in the slanted planes (X,Z and Y,Z) shown in figure 10.

It required some care to accurately predict the final picture after several rotations, especially since projected views lack the visual clue due to lines converging at infinity. Tables 11 and 12 along with figures 11 and 12 show the effects of rotation in the other two planes.
\[
\begin{align*}
X' &= (X' \cos(T) + Y' \sin(T) + Z' \sin(T)) \\
Y' &= (X' \cos(T) + Y' \cos(T) + Z' \cos(T)) \\
Z' &= (X' \sin(T) + Y' \cos(T) + Z' \sin(T)) \\
\end{align*}
\]

Table 10: Rotation in the X, Y plane.

\[
\begin{align*}
1 & \quad 0 & \quad 0 & \quad X & \quad X' \\
0 & \quad \cos(T) & \quad -\sin(T) & \quad Y & \quad Y' \\
0 & \quad \sin(T) & \quad \cos(T) & \quad Z & \quad Z' \\
\end{align*}
\]

Table 12: Rotation in the Y, Z plane.

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Combinations

Table 13 shows an example of the sequential application of two rotations using the procedure shown in table 2 to define the elements. Figure 13 combines the three rotations, a magnification and two scale changes along individual axes. Figure 14 applies shear and rotation. Figure 15 shows just the rotation for comparison purposes.

$$\begin{bmatrix}
1 & 0 & 0 \\
0 & \cos(T) & -\sin(T) \\
0 & \sin(T) & \cos(T)
\end{bmatrix} \begin{bmatrix}
\cos(S) & -\sin(S) & 0 \\
\sin(S) & \cos(S) & 0 \\
0 & 0 & 1
\end{bmatrix} = \begin{bmatrix}
A' \\
B' \\
C'
\end{bmatrix}$$

$$\begin{bmatrix}
A' = (1 \cdot \cos(S) + O' \cdot \sin(S) + O' \cdot 0) \\
B' = (1 \cdot \sin(S) + 0 \cdot \cos(S) + 0 \cdot 0) \\
C' = (0 \cdot 0 + 0 \cdot 0 + 0 \cdot 1)
\end{bmatrix}$$

Table 13: Rotation in the X, Y and Z planes sequentially.

Figure 15: Rotated but not sheared.

Mapping

All of the examples shown so far have applied the same operation to every point on the surface of the object. The coordinate transform matrix contains the same numbers for all parts of the object. A more complicated operation results when the value \((X,Y,Z)\) associated with a point on the surface of the object is replaced by a function of \(X, Y, \) and \(Z\) at each point. The result maps the object onto some surface. Thus, if \(X\) is replaced by \(\sin(X)\), for instance, the object will experience a change in scale which changes with \(X\), and the output position of a point on the object which has a value of \(X\) equal to zero, and an arbitrary \(Y\) and \(Z\) is the same as a point with a value of \(X\) equal to 180 or 360 if the computer interprets the value of \(X\) as degrees.

The result of replacing \(X\) by \(\sin(X)\) pictorially is identical to the projected view of a cylinder, parallel to the Y axis, which has the original view (such as figure 2) painted onto its surface. If the dimensions of the object for this example are such that the width is equal to 360 units, then the cylinder is completely circumscribed by the original view of the object.

In order to make a three-dimensional picture of the mapped figure, the other two dimensions must also be specified. For the example here, the depth must also be mapped by setting \(Z\) equal to \(\cos(X)\). Since the new surface is a cylinder, \(Y\) is unchanged.

Table 14: Translation matrix.

$$\begin{bmatrix}
X + k \\
Y + m \\
Z + n
\end{bmatrix} = \begin{bmatrix}
X' \\
Y' \\
Z'
\end{bmatrix}$$

Translation

Moving the object sideways is not shown but is accomplished by adding the translation value to the original value for each axis as shown in table 14.
Mapping Example

Figure 16 shows a label to be pasted on the coffee cup. This label, like the cup itself, is defined by an array of data giving the X, Y and Z coordinates of each point. The standard view is in the Z equal to zero plane. A subroutine then replaces the X and Z values with the mapped values in all the points of the array. Since the standard view of the cup is a side view, and the label is to be pasted opposite the handle, 180° is added to X before computing the mapped functions. The lower left corner of figure 16 is coordinate (0,0).

The mapped array of data is now subjected to whatever coordinate transforms are applied to the cup. Figure 17 shows the result as applied to the label alone. Figure 18 shows the completed picture.
Illusions

Figure 19 shows the same object as figure 18, rotated 180°. While most viewers see the cup with the handle toward them, "looking down into it" in figure 18, many find that figure 19 alternates between looking down into it with the handle away from the viewer, and looking up at it from the bottom, with the handle at the top. This example shows that a relatively minor change in viewpoint may produce a great change in terms of the clarity of the information presented.

Mapping Uses

Mapping may be used to compress the picture of an object to fit it into a particular space, to selectively emphasize some part while compressing the rest, such as the region near X equal to zero or 180° in this example. Or it may be used to picture some complicated configuration which is more easily defined in a rectangular coordinate system. Thus, a simple rectangular electrode configuration expressed in Cartesian coordinates may be used to compute the electric field lines at each point in the configuration. Mapping processes plus the coordinate transforms may then be used to change the known field picture into one for a complicated electron gun in a cathode ray tube.

Excerpts from the BASIC program which produced the pictures in this article are shown in listing 1. The machine used is a Tektronix 4051 graphic computer with a 4662 plotter, with matrix read only memory. The matrix command AMPY B is specific to this equipment. The rest of the program is in a fairly standard BASIC.

Lines 2000 to 2490 comprise the main program which draws the coffee cup. The purpose of each subroutine is noted. The program defining the various matrices in terms of viewpoint parameters is shown in lines 2535 to 3010. The program to combine the matrices into a single 3 by 3 matrix, C4, which is applied to the drawing is listed in lines 3120 to 3200. The AMPY B format does the matrix multiplication. In a machine without this extension, a subroutine using the equation listed in the various figures would do the same job, but take much more space.

Lines 4000 to 4300 show part of the much longer listing which defines the cup: A1 (N,1) = X, A1 (N,2) = Y, A1 (N,3) = Z. The variable A1 (N,4) is a secondary address used with a form of the print command to make it move (21) or draw (20). This is a faster way to draw on the Tektronix machine. Lines 4050 to 4140 draw the top and bottom circle.

Lines 5240 to 5270 convert the cup dimensions to graphics display units (GDUs) which are required to use this style of drawing commands. This program, with all arrays, filled, uses about 28,500 bytes of memory. Incidentally, lacking a printer, I printed the program using the plotter.
2700 $3(2,2) = \cos(3)$
2710 $3(2,3) = -\sin(3)$
2720 $3(3,2) = \sin(3)$
2730 $3(3,3) = \cos(3)$
2740 REM B4 IS THE UNIT MATRIX
2750 B4(1,1) = 1
2760 B4(1,2) = 0
2770 B4(2,1) = 0
2780 B4(2,2) = 1
2790 REM B5 EXPANDS ALONG THE X AXIS BY K1
2800 B5(1,1) = K1
2810 B5(1,2) = 0
2820 REM B6 EXPANDS ALONG THE Y AXIS BY K2
2830 B6(2,1) = K2
2840 B6(2,2) = 1
2850 REM B7 EXPANDS ALONG THE Z AXIS BY K3
2860 B7(3,1) = K3
2870 B7(3,3) = 1
2880 REM B8 MAGNIFIES BY K4
2890 B8(4,4) = K4
2900 REM B9 REFLECTS IN THE Y=X PLANE
2910 B9(1,1) = 1
2920 B9(1,2) = 1
2930 B9(2,1) = 1
2940 B9(2,2) = 1
2950 REM C1 SHEARS ALONG THE X AXIS BY KS X/Y RATIO
2960 C1(1,1) = 1
2970 C1(1,2) = K5
2980 REM C2 SHEARS ALONG THE Y AXIS BY K6 X/Y RATIO
2990 C2(2,1) = 1
3000 C2(2,2) = K6
3010 RETURN
3020 REM THIS PART FORMS THE TOP AND BOTTOM EDGE OF THE CUP
3030 A1(1,1) = 10
3040 A1(1,2) = 0
3050 A1(2,1) = 0
3060 A1(2,2) = 10
3070 FOR N = 0 TO 360 STEP 9
3080 A1(N/9+2,1) = 10 • COS(N)
3090 A1(N/9+2,2) = 10 • SIN(N)
3100 A1(N/9+2,3) = 10
3110 A1(N/9+2,4) = 20
3120 NEXT N
3130 RETURN
3140 FOR N = 0 TO 180 STEP 9
3150 A2(N/9+86,1) = A1(N/9+2,1)
3160 A2(N/9+86,2) = A1(N/9+2,2)
3170 A2(N/9+86,3) = A1(N/9+2,3)
3180 A2(N/9+86,4) = A1(N/9+2,4)
3190 NEXT N
3200 FOR N = 1 TO 262
3210 PRINT A1(N,1), A1(N,2)
3220 NEXT N
3230 RETURN
3240 FOR N = 1 TO 262
3250 A2(N,1) = A2(N-1,1) + A2(N,2) + A2(N,3) + A2(N,4)
3260 NEXT N
3270 RETURN
3280 FOR N = 1 TO 262
3290 V1(N,1) = A1(N,1)
3300 V1(N,2) = A1(N,2)
3310 V1(N,3) = A1(N,3)
3320 V1(N,4) = A1(N,4)
3330 FOR V2 = 1 TO 4
3340 V2(N,1) = V1(N,1)
3350 V2(N,2) = V1(N,2)
3360 V2(N,3) = V1(N,3)
3370 V2(N,4) = V1(N,4)
3380 NEXT V2
3390 NEXT N
3400 RETURN
3410 FOR N = 1 TO 262
3420 A2(N,1) = A2(N,2) + A2(N,3) + A2(N,4)
3430 NEXT N
3440 RETURN
3450 FOR N = 1 TO 262
3460 V1(N,1) = A2(N,1)
3470 V1(N,2) = A2(N,2)
3480 V1(N,3) = A2(N,3)
3490 V1(N,4) = A2(N,4)
3500 FOR V2 = 1 TO 4
3510 V2(N,1) = V1(N,1)
3520 V2(N,2) = V1(N,2)
3530 V2(N,3) = V1(N,3)
3540 V2(N,4) = V1(N,4)
3550 NEXT V2
3560 NEXT N
3570 RETURN
3580 RETURN
3590 REM THIS PART DRAWS THE OUTSIDE OF THE HANDLE
3600 FOR N = 50 TO 180 STEP 9
3610 A1(N/9+86,1) = 10 • COS(N)
3620 A1(N/9+86,2) = 10 • SIN(N)
3630 A2(N/9+86,3) = 10 • COS(N)
3640 A2(N/9+86,4) = 10 • SIN(N)
3650 NEXT N
3660 RETURN
3670 FOR N = 1 TO 262
3680 A1(N,1) = A1(N,2)
3690 A1(N,2) = A1(N,3)
3700 A1(N,3) = A1(N,4)
3710 A2(N,1) = A2(N,2)
3720 A2(N,2) = A2(N,3)
3730 A2(N,3) = A2(N,4)
3740 NEXT N
3750 RETURN
3760 FOR N = 1 TO 262
3770 A2(N,1) = A2(N,2)
3780 A2(N,2) = A2(N,3)
3790 A2(N,3) = A2(N,4)
3800 NEXT N
3810 RETURN
Every computer owner likes to show his or her microcomputer to friends. The first question the friends usually ask is, "What does it do?" The software system presented here demonstrates what a computer can do in a manner simple enough for almost anyone to understand. Even if you have a larger, more capable system, it is often worthwhile to be able to demonstrate something that can be accomplished on a smaller scale. WADUZITDO is small enough to run on almost any microcomputer yet it allows even the novice user to make the computer "do something."

WADUZITDO is a complete high level language processor that fits in less than 256 bytes on either a 6800 or 8080 based system. The only other requirement is some kind of terminal. The system includes a text editor to allow a program to be entered and modified, and an interpreter to execute the program. The only external routines needed are single character input and single character output such as those provided by most system monitors.

The object of WADUZITDO is to run simple conversational programs. There are just five statement types, roughly derived from the PILOT language. To keep it small only the most essential capabilities are available. This also makes programming very easy. In fact, only a few minutes after my unsuspecting spouse had asked, "What does it do?", she had written the interactive dialogue program in listing 1 to help me make out a list of acceptable birthday gifts!

Programming in WADUZITDO is straightforward and uncomplicated. For example, to direct the computer to display a line of text on the terminal you use the type statement. The following example shows the format of the type statement.

T:WHAT COULD BE EASIER THAN THIS?

The T is the operation code for type. A colon always follows the operation code. The text after the colon is displayed exactly as shown.

The accept statement allows the program to receive one input character from the terminal keyboard. Normally it is used after a type that asks for a response. For example:

T:CAN YOU TELL ME WHAT 2 + 3 EQUALS?

A:

The accept statement is just the A operation code followed by a colon. When it is encountered execution pauses until the user keys in any single character. Then the input character is saved internally for use in subsequent match statements.

The match statement is used to test the character entered by the user on the previous accept. Match is coded as an M (the operation code), followed by a colon and one character. The character in the statement is compared to the last character entered by the user. The result of the comparison is recorded internally in the match flag: Y if the match is equal, N if it is not equal.

Once set the match flag can be used to conditionally execute or skip any subsequent statement. This is done by placing either a Y (yes) or N (no) immediately before any operation code. If the Y or N is the same as the match flag the statement is executed, otherwise it is skipped.

An elaboration of the previous example illustrates the use of match.

T:WHAT IS 2 + 3?

A:

M:5

YT:FIVE, RIGHT.

NT:NO, THE ANSWER IS 5.

Normally statements are executed se-
quentia ll y. The jump statement is used to alter the normal sequence. The format of the jump statement is J, followed by a colon, and a number from zero to nine. The statement J:0 causes a branch back to the last accept statement executed. Execution resumes from that statement. The J:0 statement can be used to allow the user to reanswer a previous question. For example:

T: HOW MANY FEET IN A YARD?
A: M: 3
YT: RIGHT.
NT: WRONG STUPID, TRY AGAIN.
NJ: 0

The second form of the jump makes use of program markers. A program marker is an asterisk, *, preceding any statement. The statement J:n, where n is a number from 1 to 9, causes a branch to the nth program marker forward from the jump. This form of the jump is shown in the sample program in listing 2 which plays NIM.

The last type of statement is stop. This statement merely terminates execution of the program and returns control to the program editor. The format of the stop statement is S:

To increase the versatility of the language the S: statement can, at the user’s option, be made to call a user written machine language subroutine from within the WADUZITDO program. To do this requires a one statement modification to the system which is detailed below. If you choose to make this modification you can consider S: to be the operation code for subroutine rather than stop. The format of the subroutine statement is S:x where x is any single character which serves as a parameter to the user written program. The value x will be stored in register A in both the 6800 and 8080 version. It can be used to select different functions to be performed by the program.

During execution any statement which does not fit the syntax of one of the five statement types is printed in its entirety, then execution resumes normally with the next statement. Table 1 summarizes the WADUZITDO instruction set.

When WADUZITDO is first entered con-
Type

Type text on the terminal.

Accept

Input one character from the terminal keyboard.

Match

Compare x to last input character and set match flag to Y if equal, N if not equal.

Jump

If n = 0 jump to last accept.
If n = 1 thru 9 jump to nth program marker forward from the J.

Stop

Terminate program and return to text editor.

Subroutine

Call user machine language program (requires modification).

Conditionals

May precede any operation code.
Execute only if match flag is Y.
Execute only if match flag is N.

Program Marker

May precede any statement, serves as a jump destination.

Table 1: Program instructions for the WADUZITDO language.

<table>
<thead>
<tr>
<th>EDIT CHARACTER</th>
<th>HEX</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>24</td>
<td>Start execution.</td>
</tr>
<tr>
<td>\</td>
<td>5C</td>
<td>Move edit pointer to program start.</td>
</tr>
<tr>
<td>/</td>
<td>2F</td>
<td>Display next line of program.</td>
</tr>
<tr>
<td>%</td>
<td>26</td>
<td>Pad inserted line with nulls.</td>
</tr>
<tr>
<td>bs or -</td>
<td>0B</td>
<td>Backspace to correct typing error.</td>
</tr>
<tr>
<td>cr</td>
<td>0D</td>
<td>End of statement.</td>
</tr>
<tr>
<td>any other</td>
<td></td>
<td>Character stored in program and edit pointer advances.</td>
</tr>
</tbody>
</table>

Table 2: Editing characters used by the built-in text editor.

Text continued after listings on page 173
Figure 7: Absolute loader format representation of the 6800 WADUZTD0 program of listing 3.

Listing 3: 6800 version of the WADUZTD0 language. A dump of the MIKBUG format of WADUZTD0 (shown in listing 3a, page 712) can be used for manual entry of the program. This version was run locally at BYTE using a Switch PC6800.
Figure 2: Absolute loader format representation of the 8080 WADUZITDO program of listing 4.

```
006E 81 00 CMP A $0D TO END OF STMT ?
0070 26 F9 BNE SKIP NOT TEL, SO LOOP
0072 29 E2 BRA LOOP1 AT NEXT STMT, GO DO IT

* PROCESS ACCEPT STATEMENT
0074 01 41 IA CMP A $41 A ?
0076 26 LL BNE XM NO
0076 FF 0102 STX LST YES, SAVE LOC OF LAST ACCEPT
0078 8D CD BSR JIN ACCEPT ONE CHAR FROM KYBD
007B 01 04 STA A CHR SAVE IT
007D 00 00 INX MOVE OVER A
0081 63 00 PCR LDA A #$0D CR
0083 8D CD BSR JOUT PRINT IT
0085 8D B7 BSR PLF PRINT LINE FEED
0087 28 CD BRA LOOP1 STEP OVER 1 AND GO ON

* PROCESS MATCH STMT
008B 81 00 IM CMP A #$4D M ?
0089 26 12 BNE IX NO
008D 06 INX STEP OVER M
008E 08 INI STEP OVER 1
0090 46 00 LDA A #$00 GET MATCH CHAR
0091 59 00 LDA A #$59 ASSUME T
0093 61 01 04 CMP A CHR COMP MATCH CHAR TO INPUT CHAR
0095 27 02 BEQ MX BRANCH IF IT MATCHES.XLY
0096 46 00 LDA B #$46 RESULT IS M
0099 01 05 MI STA B FLAG SET MATCH TO Y OR N
009B 80 00 INX STEP OVER MATCH CHAR AND GO ON

* PROCESS JUMP STATEMENT
009F 81 4A IJ CMP A #$4A J ?
00A1 26 17 BNE IX NO
00A3 06 02 LDA B 2:1 DESTINATION

00A5 40 00 AND B #$0F CLEAR ZONE
00A7 26 12 BNE JF ITS A JUMP FORWARD
00A9 FG 00 LDX LST JENO... JUMP BACK TO LAST ACCEPT
00AB 2A 09 BRA LOOP CONTINUE FROM THERE

* SKIP FORWARD UNTIL PASS N * "MARKER; N IS IN ACCB"
00AE 00 JF INX STEP PGM LOC
00AF 8D 00 LDA A #$01 NEXT CHAR
00B1 01 2A CMP A #$2A *"MARKER ?
00B3 63 F9 BNE JF NO KEEP LOOPING
00B5 0A 00 DEC B FOUND ONE. COUNT IT
00B6 06 F6 BNE JF LOOP IF NEED TO FIND MORE
00B8 2C 09 BRA LOOP DESTINATION FOUND, GO EXECUTE

* PROCESS STOP OR SUBROUTINE STATEMENT
00B8 81 53 XS CMP A #$53 S ?
00BC 26 0A BNE IX NO
00BD 06 INX STEP OVER 5
00BF 00 INX STEP OVER 1
00C0 80 00 LDA A #$00 PARAMETER TO REG A
00C2 00 INX STEP OVER PARAMETER
00C3 5E 0000 JMP SUB GO TO USER SUBR (OR TO EDITOR)
00C5 6F 00 BRA LOOP GO ON UPON RETURN FROM USER SUBR

* PROCESS TYPE STATEMENT AND SYNTAX ERRORS
00C8 81 54 XT CMP A #$54 T ?
00CA 26 02 BNE TE NO, ITS AN ERROR
00CC 00 INX YES; STEP OVER T
00CD 00 INX STEP OVER 1
00CE 05 TE BSR PRT PRINT UP TO CR
00DF 0D 03E JSR PLF PRINT LNE FEED
00E0 26 02 BRA LOOP DONE WITH T

* SUBRT TO PRINT UP TO NEXT CR
00E5 40 00 PRT LDA B #$40 COUNT OF 64
00E7 46 00 PRTA LDA A #$0X NEXT CHAR
00E9 04 00 DEC B DECREMENT SAFETY COUNTER
00EA 27 0A BEO PRTB EXIT IF OVER 64 TILL CR
00EC 00 04E JSR JOUT PRINT IT
00F0 40 00 LDA A #$0X RELOAD CHAR TO ACCA
00F1 00 INX STEP LOC PRT
00F2 81 00 CMP A #$00 CR
00F4 26 F1 BNE PRTA NOT CR, LOOP
00F6 39 PRTB RTS DONE, RETURN

* ABOVE IS END OF READ ONLY PORTION OF THE PROGRAM

* THE FOLLOWING IS CHANGEABLE DATA
0100 10 00 ORG $100 MOVE TO START OF DATA AREA
0108 01 06 LDC FDB $0106 ADDR OF SOURCE PROGRAM AREA
010B 00 00 LST FDB 0 PLACE TO SAVE LOC OF LAST A
0114 00 00 CHR FCB 0 PLACE TO SAVE LAST INPUT CHAR
0115 00 00 FLC FCB 0 PLACE TO SAVE MATCH FLAG

END
```
Listing 4: 8080 version of the WADUZITDO language. A hexadecimal dump (shown in listing 4a) is provided for manual entry. This version was run locally at BYTE using a SOL-20.

```
... REDACTED...
```

Listing 4a: Dump of the 8080 version of WADUZITDO. The format consists of 4 character hexadecimal address and 7 hexadecimalally coded bytes of information. There is no checksum computed for any of the information.

```
... REDACTED...
```
the index register (6800) or HL register pair (8080) contains the location of the next program statement and should be saved and restored before returning from the subroutine. In the 8080 version the DE register pair should also be saved. Register A will contain the one character parameter, x, of the S:x. Its use is totally up to the subroutine.

The system has been organized so that the six bytes of changeable data are isolated from the read only portion. This means the rest of the 256 byte system could be placed in read only memory. It would fit in a single 1702A EROM chip.

It is easy to see how this language could be used to write a question and answer conversation using multiple choice or true, false answers. It may not be so obvious that more complex logic is possible. The example in listing 2 is a computer versus user NIM game which demonstrates a way this can be done.

Although WADUZITDO is not the ultimate answer to personal computing, it is something that almost anyone can have almost out of 256 bytes of memory.

A Pascal WADUZITDO

Notes by Ray Cote
Program by Larry Kheriaty

Along with the assembly language versions of WADUZITDO, Larry Kheriaty sent us the Pascal version shown in listing 5. The program is basically self-documenting and very easy to translate into assembly level programs for any particular processor. The program is indented to show logical relationships between related areas of text. This is sometimes known as prettyprinting.

The first four lines of the program are definition lines for the main program. In Pascal, all variables must be defined completely at the start of the section in which they are used. "Completely" means name and data type. This is a great help since all variables must be explicitly defined. You can easily check to see what type of variable is being used.

WADUZITDO uses two types of var-

---

**Listing 4, continued:**

```
007E 02 0280 SHLD LST YES, SAVE LOC OF LAST ACCEPT
007E 02 4500 CALL JIN ACCEPT ONE CHAR FROM KB0
0081 5F MOV E,A SAVE IT
0082 23 INX H MOVE OVER A
0083 44 00 MVI B,00H CR
0085 0D 4000 CALL JOUT PRINT IT
0088 0D F300 CALL PLF PRINT LINE FEED
008B 03 5600 JMP LOOP1 STEP OVER ; AND GO ON

* PROCESS MATCH STM
008E FE 4D VM CPI 4DH M ?
008F CL 0100 JNZ IXJ NO
0093 23 INX H STEP OVER M
0094 23 INX H STEP OVER M
0095 7E MOV A,M GET MATCH CHAR
0096 34 59 MVI D,59H ASSUME T
0098 8B CMP E COMP MATCH CHAR TO INPUT CHAR
0099 CA 9E00 JMZ JS BRANCH IF IT MATCHES,FLGHT
009C 1A 4E MVI D,4EH RESULT IS N
009E FE 0300 JMP LOOP1 SET MATCH FLAG TO Y OR N

* PROCESS JUMP STATEMENT
00A1 4E 04 JX CPI 4DH J ?
00A3 C2 1000 JNZ XS NO
00A6 23 INX H STEP OVER J
00A7 23 INX H STEP OVER J
00A8 7E MOV A,M DESTINATION
00A9 65 0F ANL B,OFH CLEAR ZONE
00AB 47 MOV E,A NUMBER OF $'S TO SKIP
00AC C2 0500 MVI D,5FH BRANCH IF IT MATCHES
00AF 2A 0281 LSHL LST ZERO, JUMP BACK TO LAST ACCEPT
00B2 03 5700 JMP LOOP1 CONTINUE FROM THERE

* SKIP FORWARD UNTIL PASS N ='MARKERS ( N IS IN BREG )
00B5 23 JF INX H STEP PGM LOC
00B6 7E MOV A,M NEXT CHAR
00B7 FE 2A CPI IAH =MARKER
00B9 C1 F000 JNZ JF NO, KEEP LOOPING
00BB 05 DCR B FOUND ONE, COUNT IT
00BC C2 0500 MVI D,5FH JUMP IF NEED TO FIND MORE
00BD 03 5600 JMP LOOP1 DESTINATION FOUND, GO EXECUTE

* PROCESS STOP OR SUBROUTINE STATEMENT
00C3 FE 55 XS CPI 55H X ?
00C5 C2 0200 JNZ XT NO
00C8 23 INX H STEP OVER X
00C9 23 INX H STEP OVER X
00CB 7E MOV A,M PARAMETER TO REG A
00CD 23 INX H STEP OVER PARAMETER

* NEXT STM MAY BE MADE TO BE A CALL TO USER SUBR
00CC C3 0000 JMP SUB GO TO USER SUBR ( OR TO EDITOR )
00CF C3 5700 JMP LOOP1 DONE WITH T

* PROCESS TYPE STATEMENT AND SYNTAX ERRORS
00D0 FE 54 XT CPI 45H T ?
00D3 C2 5000 JNZ TE NO, ITS AN ERROR
00D7 23 INX H STEP OVER T
00DB 23 INX H STEP OVER T
00DC 0D 0F00 TE CALL PRT PRINT UP TO CR
00DD C3 5700 JMP LOOP1 DUNE WITH T

* SUB TO PRINT UP TO NEXT CR
00DE 0E 40 PRT MVI C,40H COUNT OF 64
00E1 66 PRTA MOV B,M NEXT CHAR
00E2 8D DCR C DECREMENT SAFETY COUNTER
00E3 CA F000 JZ PLF EXIT IF OVER 64 BEFORE CR
00E6 CD 4000 CALL JOUT PRINT IT
00E7 9E MOV A,M RELOAD CHAR TO ACCA
00EA 23 INX H STEP LOC PRT
00ED 0E 0000 CPI 40H CR
00EE C2 E000 JNZ PRTA NOT CR, LOOP

* SUBROUTINE TO PRINT LINE FEED AND PAD
00F0 0E 00 PLF MVI C,40H NUMBER OF NULLS TO PRINT
00F2 06 00 PLFL MVI B,00H NULL
00F4 CD 4000 CALL JOUT WRITE A NULL
00F7 8D DCR C DECREMENT COUNTER
00F8 0F 2C00 JP PLF LOOP TILL ENOUGH NULLS
00F9 06 8A MVI B,00H LINE FEED
00FB 0C 4000 JMP JOUT PRINT THEN RETURN

* ABOVE IS END OF READ ONLY PORTION OF THE PROGRAM

* THE FOLLOWING IS CHANGEABLE DATA
0100 0001 LOC DW 0100H ADDR OF SOURCE PROGRAM AREA
0102 0000 LST DW 0000H PLACE TO SAVE LOC OF LAST A
0104 0000 CHAR DB 00H UNUSED, LAST INPUT CHAR IN EREG
0105 00 FLC DB 00H UNUSED, MATCH-FLAG IN DREG

END

September 1978 ©BYTE Publications Inc 173
variables: integer and character. There is also a definition for constants (CONST). CONST informs the compiler that the value being assigned to this variable will not change. Integer variables will only take on whole number values.

The type character (CHAR) means that the variables will take on the values of ASCII characters, including all letters, numbers and special symbols.

The last line of the definition section defines a variable PROG as an array of characters.

Listing 5: Pascal listing of WADUZITDO. See notes by Ray Cote.

```
VAR
  LOCAL: INTEGER;
  FI: BOOLEAN;
  FI: CHAR;
  PROC array[1..P2] of CHAR;

PROCEDURE LIST BEGIN
  IF FI = "\r" THEN LOC := LOC + 1
  IF FI = "\n" THEN LOC := LOC + 1
  IF FI = " " THEN I := I + 1
  REP FI := PROG[LOC]; LOC := LOC + 1; I := I + 1
  IF LOC > CEOL THEN CBUF := "\n"
  IF LOC = CEOL THEN NEWLINE
  IF LOC < CEOL THEN CBUF := PROG[LOC]; LOC := LOC + 1
END;

PROCEDURE EXECUTE BEGIN
  VAR
    N: INTEGER;
  BEGIN
    WHILE I < 64 AND (PROG[LOC] <> CEOL) DO
      BEGIN
        PROG[LOC] := PROG[LOC] + 1; LOC := LOC + 1
        IF LOC = CEOL THEN NEWLINE
      END
    END;
    CBUF := PROG[LOC]; LOC := LOC + 1
  IF CBUF = CEOL THEN NEWLINE
  EXIT
END;
```

After defining our variables we are ready to start the first executable part of the program. In Pascal, the logical parts of the program are broken into procedures, equivalent to subroutines in languages such as FORTRAN. Every procedure is blocked off by BEGIN and END statements. The name of the first procedure is CHIN. After we have determined the name, we are told to begin executing procedure ACCEPT (which will return to us input values in variable CBUF). This is a subroutine which is not shown since it is specific to the processor being used. The next two procedures are also calls to subroutines used to DISPLAY the contents of the buffer and move the output to a new line. These two procedures are also machine dependent. Notice that Pascal allows you to use descriptive names. This is very important when writing a program that you want other people to read or that you want to understand at a later date.

The next procedure, LIST, first defines its own local variables, which it will use only within the LIST routine. As before, the procedure is delimited by BEGIN and END statements. This procedure introduces us to the concept of loops. Here we have a related pair of commands: REPEAT and UNTIL. These two commands cause the one line of three instructions and the call to procedure CHOUT to execute until either the value I is greater than 64 or the variable CBUF is equal to CEOL. Once either of these two conditions occurs, the program logic proceeds to call procedure NEWLINE. At this point the LIST procedure ends and returns to whatever procedure called it.

Procedure EXECUTE looks structurally the same as procedure LIST. There is a definition of variables, the BEGIN and END delimiters, and a REPEAT-UNTIL structure. This time the REPEAT-UNTIL statement is not waiting for a relation to be true, but is rather checking against one variable. Looking at how DONE was defined at the beginning of the procedure, we see that its designation is BOOLEAN. This means that the variable is being used as a logical variable and can take on the value true or false. The REPEAT-UNTIL instruction waits to see if the variable DONE is true. If so, we have finished this procedure and can stop it.
Procedure EXECUTE also contains an IF-THEN-ELSE statement. If the value of CBUF is not contained within the brackets, perform procedure LIST. If the value of CBUF is somewhere within the square brackets, we want to perform an operation related to that value. We now come to another Pascal instruction, the CASE statement.

We are given a set of cases to choose from. The CASE statement tells us that we will be using the value in variable CBUF to determine what is to be done. We scan down each of the cases and find the one labeled with the value in CBUF. Since CBUF is type character we are looking at ASCII characters. Once we find the value of CBUF we execute the statements associated with it that are blocked off by another set of BEGIN and END statements. After we have finished, we move to the end of the CASE statement and then the last line of REPEAT-UNTIL statement.

The next section of the program does not look like the preceding sections. It does not start with a PROCEDURE statement, but has a BEGIN statement. So far we have discussed procedures. Any of the procedures that needed to use variables have defined their own. So why did we define those variables at the very beginning of the program? The reason is not to use them in a procedure, but to use them in the main program. This BEGIN statement is nothing more than the start of the mainline logic for program WADUZITDO. The mainline logic inputs characters and either stores them in an array as program or executes them as commands. This routine will not jump out of the loop and will have to beinterrupted to stop. Of course it is possible to create another command that will allow you to exit from this cycle.

Now that we have looked at the Pascal version of WADUZITDO, the reader should refer back to either of the assembly versions. The Pascal version performs the same function as the assembly versions.

The assembly language versions need to be heavily commented for the reader to understand what is happening. Even liberal comments will not help when converting from one assembly language to another. The Pascal version can be easily converted into any machine language. It is also self-documenting. Notice that even without a single comment, the Pascal listing is extremely easy to decipher. . . . RGAC•
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Is It a Plot?

Here is one of the most exciting peripherals available for the personal computer user who is interested in graphic arts applications: a very affordable ($1085) digital plotter from Houston Instrument called the Hi Plot. The statistics on this machine are impressive to say the least. The resolution of the pen tip is either .005 inch or 0.01 inch giving a total of 1400 by 2000 picture elements or 700 by 1000 picture elements respectively in its 7 by 10 inch (17.8 cm by 25.4 cm) plotting area. Standard ink cartridges are available in four colors, allowing the user to switch cartridges to produce mixed color plots. According to Tom Hall of Houston Instrument it is also possible for the individual user to kludge a standard drafting ink pen into the plotter, allowing a much wider selection of colors to be used in the form of personally chosen inks.

Many of the plotting samples seen in this issue should be reproducible by the small system owner who uses this peripheral, a typical personal system with a high level language and floppy disks, and some imagination.

Complete and ready to plot, the Hi Plot costs $1085. Contact Houston Instrument, One Houston Square, Austin TX 78753.

Photo 1: The new Houston Instrument's HI Plot plotter is shown here in a typical analytical situation: plotting a polar coordinate function in the plane of the paper with Cartesian axes for reference.

Photo 2: The interface to the user's computer is via a standard DB-25 connector located on the lower edge of the rear panel of the plotter.

Write for Free North Star Newsletter and Catalog

North Star Computers Inc, 2547 Ninth St, Berkeley CA 94710, is offering the latest issue of its newsletter free on request. In this issue North Star announces eight new application software diskettes and lists more than 50 commercially available application programs ready for use on North Star equipment. In addition, North Star's 16 page product catalog is also available free of charge.

Photo 3: Inside the HI Plot plotter, we find this pair of stepper motors which drive the mechanism through cable linkages.
Double sided floppy disk drives are now available on two of Micropolis Corp's OEM series. The company's Mega-Floppy series, Models 1015 and 1055, features an intelligent controller that facilitates interconnection of four subsystems to a common host interface for a total on line storage capacity of more than 15 M bytes.

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The 35 track configuration single drive, double sided 1015 Model III with 287 K bytes of formatted capacity is priced at $330 in quantities of 500. A quad density version, the 1015 Model IV, which has 77 tracks per surface and a track density of 100 tracks per inch with up to 946 K bytes formatted capacity, is $396. The Micropolis intelligent controller is a $369 option on the quad density version when purchased in quantities of 500. The Model 1055 Model IV, which includes the intelligent controller, power supply, bidirectional interface, enclosure and almost 2 M bytes of online capacity, is priced at $1796 in quantities of 50.

For further information, contact Micropolis Corp, 3959 Deering Av, Canoga Park CA 91304.

Contact PerSci Inc, 12210 Nebraska Av, W Los Angeles CA 90025.

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The System 88 text editor now permits the user to move, copy, or delete an entire block of text. Cursor movements are now two-dimensional; the original cursor movements have been retained. For further information, contact PolyMorphic Systems, 460 Ward Dr, Santa Barbara CA 93111.

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VATIC Circuit Card only, with interface boards $39.95
Acoustic Coupler $29.95
DAA Kit (private line only) $14.95

BELL 202 SPECIFICATIONS:
- DATA TRANSMISSION: 0-1200 baud rate over 2-wire lines, 0-1800 baud rate over conditioned lines.
- HALF-DUPLEX operation over 2-wire lines: FULL-DUPLEX over 4-wire lines.
- MARK FREQUENCY: 1200 Hz, SPACE FREQUENCY: 2200 Hz.
- REVERSE CHANNEL COMMUNICATION over 2-wire lines at 5 Baud (387 Hz.).
- Transmission Filter for echo suppression & noise reduction.
- LED Display of status and signals: Power, Terminal Ready, Modem Ready, Request To Send, Clear To Send.

OPTIONS:
- Auto Answer operation.
- Self Test Mode provides analog or digital loop-back of signals for modem diagnostics.
- LED Display of signals or status as specified by user.
- Multiple housing for up to six modem circuit cards (including combinations of Bell 103 & 202 style).

PRICES:
Standard Features, includes Reverse Channel $218.95
Standard Features, with Rev. Ch. and Auto Answer $249.95
VATIC Circuit Card only, with interface boards: with Reverse Channel, Manual DAA $149.95
with Reverse Channel, Auto-Answer DAA $170.95

PACIFIC OFFICE SYSTEMS, INC.
2600 El Camino Real, Suite 502
Palo Alto, Calif. 94306
(415) 321-3866

---

ELECTROLABS

PO Box 6721
Stanford, CA 94305
415-321-5601

...HARD AND SOFT... A NEW 32 K, S-100 Universal Static Store. Accepts 2114 RAMs or 70 ns, 3625 PROMs paging up to 8 Mbyte. Board only with manual and paging software $59.95. 32 Kby RAM $679.00, 250 ns $789.00. We have software application notes for multi-task/multi-user applications utilizing paging feature.

MINDISKETTES (5.25") 1-9 10-24 25+$
10, 16 or Soft Sector $4.79 4.50 4.25

STANDARD (8") DISKETTES

Hard or Soft Sector $5.99 4.99 4.50

CASSETTETS

R-300 Certified Phillips Type $5.25 4.99 4.35
I-150 Certified for audio decks $4.60 4.30 3.90

("Kansas City" & "SWTP format)

NEW! 32 K, S-100 Universal Static Store. Accepts 2114 RAMs or 10 ns, 3625 PROMs paging up to 8 Mbyte. Board only with manual and paging software $59.95. 32 Kby RAM $679.00, 250 ns $789.00. We have software application notes for multi-task/multi-user applications utilizing paging feature.
### PLACE ORDERS TOLL FREE:

**800/262-1710** inside California
**800/421-5809** all other states

<table>
<thead>
<tr>
<th>Description</th>
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<tr>
<td><strong>VIRTUAL COMPUTER</strong></td>
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### COMPUTER MAINFRAME

Includes 128K Power Supply +8V at 12amps. 416K to 256K. Mother Board - 12 slots for connectors. Assembled and Tested. Has Whisper Quiet Fan & A/C Line Filter. Cabinet size 18"H x 12"W x 22"D.

### DYNAMIC RAM BOARD

with 32K Exceeding write. 8K KIT $135.00 ea. 24K KIT $325.00 ea. 16K KIT $400.00 ea. EXPANDABLE 32K $411.00 264K $1344.00 64K $2100.00 256K $3750.00 1MB $750.00 2MB $1500.00 4MB $3000.00

### JADE VIDEO INTERFACE KIT

with PROVISIONS for ONBOARD and POWER ON JUMPING:

- **2MHZ** $135.00 ea. Assembled and Tested $170.00 ea.
- **4MHZ** $149.95 ea. Assembled and Tested $184.95 ea.
- Bare Board $35.00 ea.

### JADE PARALLEL/SERIAL INTERFACE KIT

**KIT** $24.95 ea. Assembled and Tested $149.95 ea.

### JADE Z80 KIT

with 2708 POWER ON JUMPING:

- **2MHZ** $135.00 ea. Assembled and Tested $170.00 ea.
- **4MHZ** $149.95 ea. Assembled and Tested $184.95 ea.
- Bare Board $35.00 ea.

### JADE 8080A KIT

**KIT** $100.00 ea. Bare Board $30.00 ea.

### JADE Computer Products

4901 W. Rosecrans - Hawthorne, Calif. 90250

Freight Charge $2.00 less than 10-lbs.

NEW CATALOG NOW AVAILABLE
Ampex MCM-8080 Core Memory Board

This 16 K byte core memory for 8080 microcomputers is now available from Ampex Corp, 200 N Nash St, El Segundo CA 90245. Fully compatible with SBC 80 single board computers, the MCM-8080 provides nonvolatile storage for 16 K bytes with a data access time within 325 ns. The read and write cycle times are 780 and 1240 ns, respectively.

Each memory board includes electronics and inhibits operation when out of tolerance. The microcomputer is a pin compatible alternative to the SBC 016, SBC 046, SBC 416 and MDS 016 memory boards used with Intel SBC 80/05, 80/10 and 80/20 or equivalent computers. It can be used to provide up to 64 K bytes of addressable locations for either 8 bit or 16 bit applications.

The board measures 12 by 6.75 by 0.50 inches (30.48 by 17.14 by 1.27 cm) and utilizes the +5 V and +12 V power available. Single unit price is $885.

Circle 582 on Inquiry card.

Building Block for Cartridge Memories

The Model 650 cartridge transport from North Atlantic's Qantex Division, 200 Terminal Dr, Plainview NY 11803, is designed as an original equipment manufacturer (OEM) memory building block for instruments, word processors, data processing systems for small businesses and other computer based equipment. The unit lists singly for $475, complete with "intimate electronics," stores up to 23 million bits of unformatted digital data on the four tracks of a DC300A tape cartridge. Optical tachometer holds tape speed at 30 inches per second for read and write operations, giving 48 K bps data transfer rate at 1600 bpi recording density. Tape is accelerated to 90 inches per second for rewind and fast search, permitting any stored data to be accessed in about 20 seconds. The transport can also be supplied with read after write heads for data validation during the actual recording process.

Circle 594 on Inquiry card.

Cl-6800 Microprocessor Memory

The microprocessor memory Cl-6800 is a 16,384 word, 8 bit dynamic random access memory. The memory module plugs directly into the EXOR-ciser and is plug compatible with the Mex-6812, 6815, 6816-1. Through the use of the 16,384 by 1 bit NMOS dynamic memory parts the memory module capacity can be increased up to 64 K bytes on a single board. An access time of 300 ns accomplished with on board hidden refresh permits maximum utilization of processor speed. The memory is addressable as a contiguous block in 4 K word increments thru 64 K. The on board dual in line package switch assigns the addresses for customer configuration. Prices are $390 for 16 K by 8 and $1230 for 64 K by 8. Contact Chrislin Industries Inc, 31312 Via Colinas #102, Westlake Village CA 91361.

Circle 593 on Inquiry card.

Non-Volatile High Speed Semiconductor Programmable Memory

The ElectriCom 4020 is a single card memory designed to meet the requirements for short and long term non-volatile high speed programmable memory systems. Memory data is maintained for a minimum of 3 months (6 months typical) after the primary board power is removed. The long data retention time allows the 4020 to be used for high speed program and data files that may be removed and stored away from the host processor. On-board nickel-cadmium batteries, battery charger and power states monitors eliminate the need for external support circuitry. The primary input power disturbance level at which the 4020 will no longer respond to read or write commands is user set with an onboard potentiometer and LED indicator. Connection to the card edge connector from the IO headers is made with wire wrap allowing the 4020 to be used with all bus structures including the Altair (S-100). The 4020 is priced at $287 and may be purchased from ElectriCom, 12567 Crenshaw Blvd, Hawthorne CA 90250.

Circle 595 on Inquiry card.

Battery Backup for Memory Board

Two static programmable memory boards capable of battery backup and compatible with Intel's SBC 80/05, SBC 80/10 and SBC 80/20 have been announced by Electronic Solutions Inc, 7969 Engineer Rd, San Diego CA 92111. The two versions are the RAM-4L containing 4 K bytes of memory and the RAM-8L containing 8 K bytes of memory. The RAM-8L uses a single 5 V supply and draws 1.2 A typical, 1.7 A maximum under operation. During battery backup at 1.7 V, the battery current is 0.5 A typical, 0.8 A maximum. Three alkaline D cell batteries can back up 8 K bytes of memory for 11 hours, according to the company. The RAM-4L is priced at $312 and the RAM-8L is $428.

Circle 596 on Inquiry card.
2708/2716 EPROM MEMORY BOARD

* S-100 BUS
* 1-32 KBYTES USING EITHER 2708 OR 2716 EPROMS
* HIGH/Low LIMIT ADDRESS RANGE SELECTION
* MEMORY BANK SELECT OPTION
* SOL™ COMPATIBLE MEMORY DISABLE
* SELECTABLE WAIT STATES
* FULLY BUFFERED INPUTS AND OUTPUTS
* DOUBLE SOLDER MASK
* SILK SCREENED PARTS LAYOUT
* COMPLETE DOCUMENTATION

$30. BARE
$100. KIT (LESS EPROMS)
TESTED AND ASSEMBLED $130. (LESS EPROMS)

DEALER INQUIRIES INVITED UNIVERSITY DISCOUNTS AVAILABLE

ITHACA AUDIO
THE OEM MARKETPLACE

Ithaca Audio Boards

Are fully S-100 compatible, featuring gold edge connectors and plated-through holes. All boards (except the Protoboard) have fully buffered data and address lines, DIP switch addressing, solder mask and parts legend.

2708/2716 EPROM Board Indispensable for storing dedicated programs and often used software. Accepts up to 16K of 2708’s or 32K of 2716’s. $25.00

2708/2716 EPROM Board Indispensable for storing dedicated programs and often used software. Accepts up to 16K of 2708’s or 32K of 2716’s. $25.00

8K Static RAM Board High speed static memory at the lowest cost per bit. Includes memory protect/unprotect and selectable wait states. $25.00

32K for $319.00
Ithaca Audio is now stocking the Mostek 4115 for S.D.’s Expandoram. Buy their basic kit, 24K of add-on RAM from us and SAVE.

S.D. SALES Expandoram Kit w/ 8K
Ithaca Audio 24 4115’s @ $7.00 ea. $151.00
TOTAL $168.00

S.D. SALES Expandoram Kit w/ 32K
YOU SAVE $475.00
TOTAL $156.00

Quality Components

ZILOG Z-80 $19.00
ZILOG Z-80A 23.00
Intel 2708 11.00
FAIRCHILD 2102 LHPC 1.60
FAIRCHILD 2102 LIPC 1.35

IMSAI 8080 Kit with 22 Slot M.B. $560.00
plus $10.00 shipping

HOW TO ORDER
Send check or money order, include $2.00 shipping per order N Y S. Residents include tax

For technical assistance call or write to:
ITHACA AUDIO
P.O. Box 91
Ithaca, New York 14850
Phone: 607/273-3271
New EROM Erasing Lamps

Two new EROM erasing ultraviolet lamps have been introduced by Spectronics Corp, 956 Brush Hollow Rd, Westbury NY 11590. The Spectroline PE-14 is a small ultraviolet lamp designed especially for the small systems users and personal computer enthusiasts. The PE-14T is the same as the PE-14, but has a 60 minute timer for automatic shut off. Both lamps will erase up to six programmable read only memory chips at one time in 14 minutes. Both UV erasing lamps feature a high intensity, shortwave UV tube, a specular reflector, and a V shaped holding tray that maintains up to six chips at a constant exposure distance. The high intensity tube is fully protected within the anodized aluminum housing, and a safety interlock prevents the unit from operating when the tray is not fully inserted. The conduction foam pad holds the chip in place during exposure and prevents electrostatic build up, while protecting the chip from possible static charge.

Attention Paper Tape Tearers

This advanced splicer punch gauge for all 8, 7-6, and 5 channel perforated tapes is being marketed by Telex Marketing Company, 6464 Sunset Blvd, Los Angeles CA 90028. The Telex Splicer/Punch is said to make perfect splices and to repair tears up to 8 inches long. Utilizing a precision scissors type cutting shear, it works with all paper and Mylar tapes. Also featured are a data patch storage compartment, precision code hole punch, precision tape gauge, hold down arms, precision registration pins, and a punch position guide. For $169.50 Telex is offering a starter kit which includes the Splicer/Puncher and 300 data patches.

All Circuit Evaluators

These new Powerace all circuit evaluators have been introduced by A P Products Inc, POB 110, 72 Corwin Dr, Painesville OH 44077. The Powerace line includes three power breadboards, Models 101, 102 and 103. All three models offer 256-5 tie point terminals and 16-25 tie point buses, fused power supply and ground plane. All models feature Super-Strip SS-2s and will accept all DIP sizes plus TO-5s and discretes with leads to .032 inch diameter. Prices are $84.95 for the 101, $114.95 for the 102, and $124.95 for the 103. For further information about the different models, contact the company.

TR 1983 Bus Oriented UART Replacement for 8251 UART

The TR 1983 bus oriented universal asynchronous receiver transmitter (or UART) that is fully compatible with the asynchronous capabilities of the 8251 UART is now available from Western Digital Corp, 3128 Red Hill Av, POB 2180, Newport Beach CA 92663. It has a 28 pin package pinout that allows direct replacement of the 8251. The TR 1983 features full or half duplex operation, and is powered by a single +5 V supply. For further information, write to the company.

Pocket-Sized Solderless Breadboards

The Continental Specialties Corp carries a line of Experimenter socket solderless breadboards. The smallest of these is 3.6 inches by 2.1 inches by .3 inches, about the size of an audio cassette. No soldering, drilling or tooling is required. Parts simply plug right into the breadboard and interconnections are accomplished by pushing short lengths of hookup wire into adjacent holes. Prices range from $4 to $10.95. Contact Continental Specialties Corp, 70 Fulton Ter, New Haven CT 06509.

CSC Proto-Clip Integrated Circuit Test Clips Used to Protect MOS Devices from Static

The CSC Proto-Clip integrated circuit test clips clip gently onto DIP integrated circuit packages and bring their pin connections to the top end of the clip. Cabled versions of this tool include a connecting cable preattached to the top or business end of the integrated circuit test clip. By attaching all leads at the far end of the clip to a good working ground, each integrated circuit pin is effectively shorted to ground and the problem of static discharge during handling is eliminated. The clips are available in 14 pin, 16 pin, 24 pin and 40 pin configurations; 18, 24 and 36 inch cables are available in each clip size. Prices for each clip and cable assembly range from $7.75 to $21.75 (unit quantities). For further information contact Continental Specialties Corp, 70 Fulton Ter, New Haven CT 06509.

CSC Proto-Clip integrated circuit test clips used to protect MOS devices from static.
Hazeltine 1400
cost effective
CRT TERMINAL
$6.59 plus shipping

The Hazeltine 1400 Video Display Terminal is designed to optimize interactive real-time operations. The interface is capable of either local or remote connection through an EIA RS-232-C interface at baud rates that are switch selectable up to 9600 bits.

- All 128 ASCII Codes
- 64 Displayable Characters
- 19 Lines 12 inch Screen
- 92 Characters per Line
- Self Diagnostic Year

Quality pricing upon request.

S-100 Mother Board
Quiet Bus
$29.95
16 slot IMSA

HEXADECIMAL KEYBOARD
This 16-key hexadecimal keypad is designed for memory豪门 access that require 4-bit output.
Each key displays a hexadecimal number on LED display which can be translated into a 4-bit binary number.

MAXI-SWITCH ASCII KEYBOARD
Assembled $64.97

NEW
Definitely the best small system keyboard that we have seen. Maxi-Switch has incorporated all the important keyboard features at a reasonable price. Pull 128 ASCII functions, "F" key rollover, automatic repeat, user defined special function keys, erase, control & lock of others. Data sheet upon request.
PERIPHERALS

Timing Control Unit Available for LSI-11/2

Use This for a Compact Extension Terminal

The Transactor III data terminal utilizes a microprocessor in its design. Features available include synchronous or asynchronous communications line support for both dedicated or polled multidrop environments. The terminal includes a single line 32 character gas discharge display and a 53 key Teletype style keyboard. It can be directly attached to any computer with an RS-232 or 20 mA current loop interface or can be attached to a communications line through a modem. Switches allow the user to select the operating mode including: 110 to 9600 bps transmission speeds, full or half duplex, even, odd or no parity, and the station address. The unit supports ASCII coded data with EBCDIC coded data available as an option. Other options include an expanded 256 byte data buffer and an addressable RS-232 port. The terminal can be provided with any line protocol for direct replacement of IBM 2260, 3275 or other types of terminals. Price is $995 from Computerwise Inc, 4006 E 137th Ter, Grandview MO 64030.

High Resolution Graphics

Although this Vector high resolution graphics board has been designed to operate with all Vector Graphic computers with 8 K bytes of static programmable memory, the manufacturer says it is fully compatible with any S-100 bus computer. The board is designed to operate in one of two modes: digital output or 16 level gray scale. It requires +8 VDC and a minimum of 8 K programmable memory and will produce digital graphic displays of 256 pixels horizontal by 240 pixels vertical in the digital mode or gray scale pictures 128 pixels horizontal by 120 pixels vertical. The video output conforms to RS-170 and will interface to standard raster scan monitors. The board is priced at $225 fully assembled and tested, $195 as a kit, and 8 K bytes of memory must be available in the user's system for a screen buffer. From Vector Graphic Inc, 790 Hampshire Rd, Westlake Village, CA 91361.

Intelligent Communication Interface from Apple

Low cost telephone communication for the deaf; inexpensive high speed message transfer; computers challenging each other at chess; remote system failure diagnosis; access to data banks and program libraries by phone...are only a few of the applications made possible by the newly announced intelligent communications interface from Apple Computer Inc, 10260 Bandley Dr, Cupertino CA 95014.

This dual size peripheral board, designated TCU-50D, provides calendar and real time functions for DEC's LSI-11 and LSI-11/2. The unit, equipped with rechargeable battery back up capability, will keep track of the correct date and time for up to three months after the computer's power is turned off. This feature also enables the user to keep track of system down time during power failures. The board will present the date (month and day) and the time (hours, minutes and seconds) when a read instruction is given by the user. The units are shipped working and preset to the correct date and local time at the customer's location. A simple routine can reset the date and time. The TCU-50D costs $295 and is available from Digital Pathways Inc, 4151 Middlefield Rd, Palo Alto CA 94306.

Intelligent Communication Interface from Apple

The new card, Model A2B0003X, can be connected to any device which will accept the industry standard RS-232C serial interface, including the 103 A type modems manufactured by various companies. It operates at 110 or 330 bits per second. The price of the card is $180. It is supplied complete, with operating system built in, with cable and operation manual.

Circle 571 on inquiry card.

Circle 572 on inquiry card.

Circle 573 on inquiry card.

Circle 574 on inquiry card.
16K E-PROM CARD
IMAGINE HAVING 16K OF SOFTWARE ON LINE AT ALL TIME!
S-100 (Imsai/Altair) Buss Compatible!

KIT FEATURES:
1. Double sided PC board with solder mask and silk screen and gold plated contact fingers.
2. Selectable wait states.
3. All address lines & data lines buffered.
4. All sockets included.
5. On card regulators.

KIT INCLUDES ALL PARTS AND SOCKETS (except 2708's). Add $25. for assembled and tested.

187

PRICE CUT!

$57.50 kit

SPECIAL OFFER:
Our 2708's (450NS) are $12.95 when purchased with above kit.

8K LOW POWER RAM KIT-$149.00
S-100 (Imsai/Altair) Buss Compatible!

2 KITS FOR $279
Fully Assembled & Burned In
$178.00
Blank PC Board w/ Documentation
$29.95
Low Profile Socket Set .... 13.50
Support IC's (TTL & Regulators)
$9.75
Bypass CAP's (Disc & Tantalums)
$4.50

USES 21L02 RAM'S!

450 NS!
2708 EPROMS
Now full speed! Prime new units from a major U.S. Mfg. 450 NS. Access time, 1K x 8. Equiv. to 4-1702 A's in one package.

$15.75 ea.

4 FOR $50.00

INTEL 2102 RAM SALE!
BRAND NEW 2102A-4. FACTORY PRIME!
WE MADE ANOTHER SUPER SURPLUS BUY!

450 N.S.

8 FOR $7.95
32 FOR $28

4K STATIC RAM'S
2114. The new industry standard. Arranged as 1K x 4. Equivalent to 4-21 L02's in 1 package. 16 pin DIP. 2 chips give 1K x 8.

$2.54
8/$85.

OPCBA LED READOUT
SLA-1. Common Anode. .33 inch character size. The original high efficiency LED display. 76 ea.

4 FOR $2.50

Z-80 PROGRAMMING MANUAL
By Mostek. The major Z-80 second source. The most detailed explanation ever of the working of the Z-80 CPU CHIPS. At least one full page on each of the 158 Z-80 instructions. A MUST reference manual for any user of the Z-80. 300 pages. Just off the press.

$12.95

NATIONAL SEMICONDUCTOR
JUMBO CLOCK MODULE

MANUFACTURER'S CLOSEOUT

$6.95

FOR $5.95

DIGITAL RESEARCH CORPORATION

OF TEXAS

P. O. BOX 401247 GARNALD, TEXAS 75040 (214) 271-2461

Circle 100 on inquiry card.
YOUR BEST BUY IN WIRE WRAP SUPPLIES

**PRECUT WIRE**
*WHY BUY WIRE ON ROLLS?*
- Fast - No more cutting & stripping by hand
- Good - Clean, uniform strip
- Economical - Cheaper than using bulk wire

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**SOLDERLESS BREADBOARDS**
*SK 10 $16.50*
- Over 100 pieces of precut wire in assorted colors
- Choose color: Red, Blue, Yellow, White, Orange, Or Assorbment

**INTERCONNECT CABLES**
(Ribbon cable connectors for connecting boards to Ivan ports or board to board)

**WIRE WRAP TOOLS**
*SAVE 30¢

**WIRE KITS**

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**PAGE DIGITAL ELECTRONICS**

Ordering Information:
- Orders under $25 and COD's, add $2
- All others, shipped Ppd in U.S. via UPS
- For Blue Label (Air) or 1st Class, add $3
- We accept Viss & Mastercharge
- Credit orders shipped same day
- Dealer Inquiries Invited

**EDGE CARD CONNECTOR SALE!**

**WIRE WRAP SOCKETS**

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</tr>
<tr>
<td>24 pin</td>
<td>$5.40</td>
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</tbody>
</table>

**FREES**
- Send for your copy of our NEW 1976 QUEST CATALOG
- Include 20c stamp.
APPLE II SERIAL I/O INTERFACE *
Part no. 2
Baud rate is continuously adjustable from 0 to 30,000. Plugs into any peripheral connector. Low current drain, RS-232 input and output. On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even. Jumper selectable address. SOFTWARE Input and Output routine from monitor or BASIC to teletype or other printer. Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. Board only $15.00, with parts $42.00, assembled and tested $62.00.

MODEM *
Part no. 109
- Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • equate: only low cost components • TTL input and output—serial • Connection 8 ohm speaker and crystal mic. directly to board • Uses XR FSK demodulator • Requires +5 volts • Board $7.60, with parts $27.50.

DC POWER SUPPLY *
Part no. 6085
- Board supplies a regulated +5 volts at 3 amps, +12, -12, and -5 volts at 1 amp. Power required is 58.8 volts AC at 13 amps., and 24 volts ACCT at 1.5 amps. Board only $12.50; with parts excluding transformers $42.50.

TAPE INTERFACE *
Part no. 111
- Play and record Kansas City Standard tapes • Converts a low cost tape recorder to a digital recorder • Works up to 1200 baud • Digital in and out are TTL—serial • Output of board connects to mic. in of recorder • Earphone of recorder connects to input on board • No coils • Requires +5 volts, low power drain • Board $7.60; with parts $27.50.

TIDMA *
Part no. 112
- Tape Interface Direct Memory Access • Record and play programs without bootstrap loader (no prom) has FSK encoder/decoder for direct connections to low cost recorder at 1200 baud rate, and direct connections for inputs and outputs to a digital recorder at any baud rate. S-100 bus compatible • Board only $39.00; with parts $145.00.

UART & BAUD RATE GENERATOR *
Part no. 101
- Converts serial to parallel and parallel to serial • Low cost on board baud rate generator • Baud rates: 110, 150, 300, 600, 1200, and 2400 • Low power drain +5 volts and -12 volts required • TTL compatible • All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity. All connections go to a 44 pin gold plated edge connector • Board only $12.00; with parts $35.00 with connector add $3.00.

RF MODULATOR *
Part no. 107
- Converts video to AM modulated RF, Channels 2 or 3. So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple. Power required is 12 volts AC or +5 volts DC • Board $7.60, with parts $13.50.

RS 232/TTY *
Part no. 600
- Converts RS-232 to 20mA current loop, and 20mA current loop to RS-232 • Two separate circuits • Requires +12 and -12 volts • Board only $4.50, with parts $7.00.

8K STATIC RAM *
Part no. 300
- 8K Altair bus memory • Uses 2102 Static memory chips • Memory protect • Gold contacts • Wait states • On board regulator • S-100 bus compatible • Vector input option • TRI state buffered • Board only $22.50, with parts $19.00.

8K STATIC RAM *
Part no. 43
- Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • No coils, only low cost components • TTL input and output—serial • Connects 8 ohm speaker and crystal mic. directly to board • Uses XR FSK demodulator • Requires +5 volts • Board $7.60; with parts $145.00.

RS 232/TTY *
Part no. 53
- Converts RS-232 to 20mA current loop, and 20mA current loop to RS-232 • Two separate circuits • Requires +12 and -12 volts • Board only $4.50, with parts $7.00.

RS 232/TTL *
Part no. 232
- Converts TTL to RS-232, and converts RS-232 to TTL • Two separate circuits • Requires +12 and -12 volts • All connections go to a 10 pin gold plated edge connector • Board only $4.50, with parts $7.00 with connector add $2.50.

To Order:
Dept. B, P.O. Box 21638, San Jose, CA. USA 95151

ELECTRONIC SYSTEMS

Circle 125 on inquiry card.

BYE September 1978 189
What’s New?

PERIPHERALS

Pocket-Sized Terminal

An alternative to the Teletype has been developed by Gleichmann & Co, Wormser Str 9, D 6710 Frankenthal, WEST GERMANY. The pocket-sized terminal has the same electrical interface but according to the company costs about one tenth as much as the conventional solution.

The size of a pocket calculator, the device has a built-in microprocessor, works fully electronically, and is noiseless. It has a keyboard for 64 alphanumeric characters, produces serial ASCII code and is compatible with any equipment that operates on a 20 mA current loop. It has a 9 digit display. The IO lines are galvanically separated by optoelectronic couplers. Transmission speed is 110 bps or, optionally, 300 bps. The device measures 3 by 6 by 1 inches (7.5 by 15.5 by 2.5 cm) and has a power consumption of 400 mA from the 5 V supply and 140 mA from the 12 V supply.

The US distributor is Sedillo Company Inc, 225 E Sunnyoaks Av, Campbell CA 95008.

Circle 633 on inquiry card.

Interface for Teletype Model 40 Printer

The C/D-40 interface board allows the 300 line per minute Teletype Model 40 printer to connect to a host computer or terminal that offers a Centronics or Dataproducts Interface. Complete hardware and software transparency is provided so that plug to plug compatibility exists without making system modifications. The C-40 allows for the replacement of any Centronics printer and the D-40 provides for Dataproducts replacement.

The board is self-contained and does not require external power when mounted within the printer cabinet, since power is derived from the printer. The board may also be mounted inside the host system. This allows for computer and printer separation, via two wire pairs, of up to 2000 feet.

Standard features include field selectable control character code conversion, parity selection, extended ASCII, and variable motor time out after last character received.

The C-40 is priced at $795 and can be obtained from Innovative Electronic Systems Inc, 15200 NW 60 Av, Miami Lakes FL 33014.

Circle 636 on inquiry card.

Plotter Controller

The Serial Language Independent Plotter Controller (SLIP) is installed between your terminal and a modem on a time shared network or between your terminal and a local computer. With the connection of an XY recorder to SLIP, you have plotting and graphics capability. Any teleprocessing site utilizing standard RS-232 serial communications can become a remote graphics facility.

SLIP contains a microprocessor to provide internal vector and character generation features, allowing a maximum of plotting with a minimum of data exchange. SLIP55 capabilities include the support of two way user and computer communications during a plot, and an off line mode which assists in plot layout and design. It also detects and indicates character format errors.

During plot generation SLIP intercepts the plot data from the computer and generates XY signals to the plotter. The X and Y outputs from SLIP are user programmable for horizontal and vertical dot resolutions up to 128 dots per inch. Once the fields have been defined, the EX-820 automatically formats graphic and alphanumeric printouts to user specifications. Vertical dot resolution is fixed at 65 dots per inch. There is also provision for automatic histogram generation.

Standard features include: RS-232C serial input as well as parallel ASCII; driven by an Intel 8048; 512 character multiline asynchronous input buffer, optionally expandable to 2 Kbyte characters; 96 character ASCII standard, optionally expandable to 256 characters with user programmable fonts; software selection of three character sizes to give 80, 40 or 20 column printing; software selection of reverse printing, where light characters are formed on a dark background; 2 K bytes of user programmable read only memory (low cost option) which converts the printer into an intelligent printer.

Dimensions are 11 by 4 1/4 by 12 inches (28 by 10.8 by 30.5 cm). It weighs 12 pounds (5.4 kg), including a 230 foot roll of paper.

Circle 634 on inquiry card.

Micrographics Printer Combines Graphics and Alphanumerics

A MicroGraphics printer, the EX-820, which can mix high resolution graphics and full ASCII alphanumeric, is now available from Axion, 5932 San Fernando Rd, Glendale CA 91202, at the single quantity price of $795.

Under software control, users have flexibility in mixing alphanumeric ASCII fields and graphic fields on any line. The user can define the size of each graphic field and can choose from four preprogrammed horizontal dot resolutions up to 128 dots per inch. Once the fields have been defined, the EX-820 automatically formats graphic and alphanumeric printouts to use specifications. Vertical dot resolution is fixed at 65 dots per inch. There is also provision for automatic histogram generation.

Standard features include: RS-232C serial input as well as parallel ASCII; driven by an Intel 8048; 512 character multiline asynchronous input buffer, optionally expandable to 2 Kbyte characters; 96 character ASCII standard, optionally expandable to 256 characters with user programmable fonts; software selection of three character sizes to give 80, 40 or 20 column printing; software selection of reverse printing, where light characters are formed on a dark background; 2 K bytes of user programmable read only memory (low cost option) which converts the printer into an intelligent printer.

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Circle 634 on inquiry card.

Where Do New Product Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the neat new whizbang glitzy or save the world software package is of interest to the personal computing experimenters and homebrewers who read BYTE, we print the Information in some form. We openly solicit such information from manufacturers and see to it that this marketplace is printed more or less as a first in first out queue, subject to occasional priority modifications.

Circle 636 on inquiry card.
The EW-2001 A “Smart” VIDEO BOARD KIT At A “Dumb” Price!

STATE OF THE ART TECHNOLOGY USING DEDICATED MICROPROCESSOR I.C.
NUMBER OF I.C.s REDUCED BY 50% FOR HIGHER RELIABILITY
MASTER PIECE OF ENGINEERING
FULLY SOFTWARE CONTROLLED

Price: $199.95

SPECIAL FEATURES:
- Programmable no. of scan lines
- Underline blinking cursor
- Cursor controls: up, down, left, right, home, carriage return
- Composite video
- *Min. 2K required for operation of this board.

DISPLAY FEATURES:
- 128 displayable ASCII characters (upper and lower case alphanumeric, controls)
- 64 or 32 characters per line (jumper selectable)
- 32 or 16 lines (jumper selectable)
- Screen capacity 2048 or 512
- Character generation: 7 x 11 dot matrix

OPTIONS:
- Sockets ............... $10.00
- 2K Static Memory (with Sockets) ........ $45.00
- 4K Static Memory (with Sockets) ........ $90.00
- Complete unit, assembled and tested with 4K Memory ........ $335.00
- Basic software on ROM ...... $20.00
- Text editor on ROM .... $75.00

ASCII 3rd GENERATION *ONLY KEYBOARD KIT $68.00

- TTL Logic Circuits
- Power: +5V 275mA
- Upper and Lower Case
- Full ASCII Set (Alpha Numeric, Symbols, Control)
- 7 or 8 Bits Parallel Data
- Optional Serial Output
- Selectable Positive or Negative Strobe, and Strobe Pulse Width
- ‘N’ Key Roll-Over
- Fully Degrounded
- Carriage Return Key
- Repeat Function Key
- Shift Lock, 2 Shift Keys
- 4 User Defineable Keys
- P.C. Board Size: 17-3/16” x 5”

OPTIONS:
- Metal Enclosure
  Painted IBM Blue and White $25.00
- 18 Pin Edge Con. $2.00
- I.C. Sockets $4.00
- Serial Output (Shift Register) $2.00
- Upper Case Lock Switch for Capital Letters and Numbers $2.00

KIT INCLUDES: Keyboard, P.C. Board, all required components & assembly manual.

NOTE: If you have this 63 Key Teletype Keyboard you can buy the Kit without it for only $44.95.

** DEALER INQUIRIES WELCOMED **

** ELECTRONICS WAREHOUSE Inc. **
1603 AVIATION BLVD.
REDONDO BEACH, CA. 90278
TEL. (213) 376-8005
WRITE FOR FREE CATALOG
Minimum Order: $10

** California residents add 6% sales tax **

Circle 130 on inquiry card.
The Algorithmics PR-DW1 Daisy Wheel Printer is a printer designed for use with microcomputer systems for high quality printing and plotting applications. This printer operates under control of an internal microprocessor and communicates with the host microprocessor over a high speed asynchronous parallel interface. It prints bidirectionally at rates of 45 characters per second. The carriage can be positioned left and right in increments as fine as 1/4 of an inch (0.53 mm). Hardware options include 55 characters per second version, metal print wheel, cam feed platen and forms tractor. The interface to the host computer consists of both hardware and software. The hardware component is a custom 50 conductor cable that terminates at the host machine in standard 25 pin connectors. The software consists of two applications packages. One package is for text printing and features bidirectional printing, automatic tabbing, and high speed travel over character spaces and blank lines. The second package is a graphics package that utilizes the 1/120 inch horizontal and 1/48 inch vertical precision print head positioning to achieve full graphics capabilities. Price is $2678 from Algorithmics Inc, POB 56, Newton Upper Falls MA 02164.
DIODES/zensers
1N914 100V 10mA .06
1N4905 600V 1A .08
1N4007 1000V 1A .15
1N4148 75V 10mA .05
1N4733 5.1V 1 W Zener .05
1N753A 6.2V 500 mW Zener .25
1N581A 12V .25
1N759A 12V .25
1N5243 13V .25
1N5244B 14V .25
1N5245B 15V .25

Sockets/bridges
8-pin pcB .20 wW .35
14 pin pcB .20 wW .40
16 pin pcB .20 wW .40
18 pin pcB .25 wW .75
22 pin pcB .35 wW .95
24 pin pcB .35 wW .95
28 pin pcB .45 wW 1.26
40 pin pcB .65 wW 1.80
Molex pins .01 To-3 Sockets .25
2 Amp Bridge 100-prv .95
25 Amp Bridge 200-prv 1.95

Transistors, LEDs, etc.
2N2227 NPN (2N2227 Plastic .10) .15
2N2007 PNP .15
2N3906 PNP (Plastic - Unmarked) .10
2N3904 PNP (Plastic - Unmarked) .10
2N3904 PNP .35
2N3955 NPN 15A 60V .35
2N3914 NPN Darlington .35
LED Green, Red, Clear, Yellow .15
D.L.477 7 seg Back-cathode (.50) 1.95
MAN77 7 seg Back-cathode (Red) .25
MAN3601 7 seg Back-cathode (Red) .25
MAN80A 7 seg Back-cathode (Yellow) .25
MAN74A 7 seg Back-cathode (Red) .15
FDN339 7 seg Back-cathode (Red) 1.25

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MCM14 3.00 8228 6.30
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2114 9.50 8723 1.50
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74LS28 5.35 8724 2.20
TMS4044-5 9.55 8797 1.00
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4030 .35 7445 .45
4033 .45 7444 .45
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NEW! BULB-ENERGY SAVER
Bulb energy savers will last for years in most normal use. Now available in 3-100 watt sizes. (Save from 50 to 70% in energy costs.) Easily installs in any standard lamp socket. A normal 60-watt bulb, when using a bulb energy saver, will last for 1500 hours.

<table>
<thead>
<tr>
<th>Incandescent Bulb Size</th>
<th>Wattage</th>
<th>Life (in hours)</th>
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<tr>
<td>Standard 60W</td>
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<td>1500</td>
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<td>Bulb Energy Saver 60W</td>
<td>15</td>
<td>1500</td>
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Bulb Energy Saver 60W: $3.99 each

KEYBOARDS

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<th>Model</th>
<th>Description</th>
<th>Key Switch Options</th>
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<td>63K</td>
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KEYBOARDS: Hexadecimal Encoder

STOP WATCH CHIPS

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<th>Chip Type</th>
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ELECTRONICS

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<td>1525 PARALLEL CABLE</td>
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DIGITAL STOPWATCH

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PHONE BOARDS

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PROBE BOARDS

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</table>

Circle 200 on inquiry card.

BYE2017 September 1978  195
GETTING STARTED WITH YOUR PET

A complete line of miniature (7/8 inch diameter bushing) oil tight pushbuttons, selectors and pilot lights is described in Alcoswitch's new 12 page catalog, publication T278. Over 20 basic models are listed with details concerning control function options and color choices. The contact blocks offered range from logic types to 600 VAC models. This catalog will be sent free of charge to all inquiries. Contact Alco Electronic Products Inc., 1551 Osgood St., North Andover MA 01845.

New Products for the Commodore PET 2001

This beginner's workbook is intended for PET users who are anxious to put their PET to work. This beginner's workbook is said to supplement the documentation provided by Commodore. It covers the fundamentals of PET BASIC and explains its characteristics, limitations and useful features. The descriptive text is said to include step by step, detailed exercises including the expected PET responses. In addition to this beginning text, workbooks on advanced topics are said to be available as well as software applications for the PET. No price was given, so for more information write TIS, POB 921, Los Alamos NM 87544.

New Catalog from Alcoswitch

A complete line of miniature (7/8 inch diameter bushing) oil tight pushbuttons, selectors and pilot lights is described in Alcoswitch's new 12 page catalog, publication T278. Over 20 basic models are listed with details concerning control function options and color choices. The contact blocks offered range from logic types to 600 VAC models. This catalog will be sent free of charge to all inquiries. Contact Alco Electronic Products Inc., 1551 Osgood St., North Andover MA 01845.

MicroAge Product Information

Literature describing MicroAge's printers, video boards, CRTs, monitors and keyboards is now available from the company. Included with the product descriptions is a complete price list. For this literature write MicroAge, 14250 12th Pl #01, Tempe AZ 85281.

PRACTICAL MICROCOMPUTER PROGRAMMING:

THE INTEL 8080 by Weller, Shatzel, & Nice

Here is a comprehensive source of programming information for the present or prospective user of the 8080 microcomputer, including moving data, binary arithmetic operations, multiplication and division, use of the stack pointer, subroutines, arrays and tables, conversions, decimal arithmetic, various I/O options, real time clocks and interrupt driven processes, and debugging techniques. This 306 page hardcover book is well worth its $21.95 price and should be in every 8080 or Z-80 user's library.

THE M6800 by W J Weller

This second volume of the Practical Microcomputer Programming series addresses the problems of applications programming at assembly level for the M6800. In 16 chapters and more than 100 formal examples, the fundamental techniques of assembly level programming are applied to the solution of specific problems with the 6800. Nowhere theoretical, it is a thorough and detailed methods text for the beginning and intermediate application programmer using the 6800. $21.95. Hardcover.

For your convenience in ordering please use this page plus the order form on p. 111.

Dial your bank card orders TOLL-FREE: 800-258-5477
**SOFTWARE**

**Compiler Basics**

**Business, Control Applications on Microprocessor Systems**

Software Dynamics BASIC, a compiler version of the programming language, is now available for 6800 microprocessor systems. Decimal arithmetic, formatted output and file IO is said to make SD BASIC ideal for microprocessor business applications such as payroll and inventory. High speed, built-in transcendental functions, assembly language interface and the performance resulting from compiling BASIC programs makes SD BASIC a tool for building process control programs. According to the company, the software is currently available on American Micro systems MDC, Smoke Signal Broadcasting, BF-68, S/WPC DOS and Wave MATE microcomputers. The IO Interface Package concept allows you to customize SD BASIC to your DOS system. Further information can be obtained from Software Dynamics, 18914 S. Laurelbrook PI, Cerritos CA 90701.

**Multitasking Executive Added to Microbench Software**

MTX-11, a multitasking executive for PDP-11 and LSI-11 computers, is the latest addition to Microbench software. The MTX-11 is said to execute multiple tasks on an interleaved basis with software priorities determining which task to execute if competition exists for processor and system resources.

The MTX-11 is priced at $1395 plus $100 per processor and is available from Virtual Systems Inc, 1500 Newell Av, Suite 406, Walnut Creek CA 94595.

**Data Base and Query System Responds to Pidgin English**

It is said that your home or business computer can manage a data base of stored information and respond to your queries in pidgin English, using a new microcomputer software package called WHATSIT. The system runs in BASIC on a modest personal computer yet it brings the power of a data base manager. Data is stored and retrieved by typing pidgin English requests, and disk space allocation is handled automatically. The file structure is never frozen but develops automatically through normal use to adapt to user requirements. Stored information is automatically cross-indexed under any desired headings, and headings may be added or changed at any time. Available in North Star BASIC, the system runs in 24 K of memory. It is offered with three ready to run programs on a mini-disk for $75. A manual written in non-technical language is $25. It is available from information Unlimited, 694 W 70 S Private Rd, Hebron IN 46341.

**Communications Software for LSI-11 Announced**

The RT-11 compatible software driver for the Mighty-Mux 11L, direct memory access (DMA) serial line multiplexer, has been announced by Educational Data Systems, Inc, 1682 Langley Av, Irvine CA 92714.

Providing efficient IO for any RT-11 based LSI-11 system, this new package simultaneously supports full duplex asynchronous IO to as many as 128 ports on the multiplexer. Control requests are provided to determine port status, set port characteristics (bps rates, parity, etc), assign logical and physical port mapping, and abort IO requests. For stand alone multiplexing operations, modules are provided which may be linked directly to an applications package. This avoids the intervention and overhead of the RT-11 IO subsystem. A second configuration loads the package as a standard RT-11 driver. The driver will function with any V02 system and is provided at no charge to users of the Mighty-Mux 11L.

**Assembly Language Development System for 8080 and Z-80**

The Program Development System (PDS) is an assembly language development system for 8080 or Z-80 microcomputers with at least one disk drive. PDS is said to include a unified assembler/editor, a macro assembler combining the features of a relocating linker loader, a string oriented text editor, and a trace debugger/diassembler. The assemblers favor the Intel instruction mnemonics treating the Z-80 superset as a logical and syntactical extension. Source modules are available for floating point arithmetic, floating point IO, trigometric functions, numerical and alphabetic sorting, disk I/O, integer I/O, 100 line program, fast Fourier transform, and a full function expression evaluator. For further information contact Allen Ashley, 395 Sierra Madre Villa, Pasadena CA 91107.

**Software for Users of North Star BASIC**

A series of programs for users of North Star BASIC is available on North Star diskette with user instructions. Word processing, investments, inventory and other business oriented programs are offered. A complete catalog of North Star software is now available, including not only California Software material, but programs available from firms around the world. For further information contact California Software, POB 275, El Cerrito CA 94530.

**A New DOS for Poly 88 and North Star Disk Systems**

The Lazy Man's DOS (disk operating system) for Poly 88 owners with North Star Disk Systems has been announced by Cardinal Products, 1600 Tilden St, Wichita Falls TX 76309. According to the company, control character commands let you quickly and easily load and start BASIC, jump back to DOS, restart BASIC cold (initialized) or warm (retaining some user program data), list directory while in DOS or BASIC and list source text in any convenient format and TEXT will format the output as desired. For further information contact Chuck Bennett, Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110.

**Compiler Basics**

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**Communications Software for LSI-11 Announced**

The RT-11 compatible software driver for the Mighty-Mux 11L, direct memory access (DMA) serial line multiplexer, has been announced by Educational Data Systems, Inc, 1682 Langley Av, Irvine CA 92714.

Providing efficient IO for any RT-11 based LSI-11 system, this new package simultaneously supports full duplex asynchronous IO to as many as 128 ports on the multiplexer. Control requests are provided to determine port status, set port characteristics (bps rates, parity, etc), assign logical and physical port mapping, and abort IO requests. For stand alone multiplexing operations, modules are provided which may be linked directly to an applications package. This avoids the intervention and overhead of the RT-11 IO subsystem. A second configuration loads the package as a standard RT-11 driver. The driver will function with any V02 system and is provided at no charge to users of the Mighty-Mux 11L.

**Assembly Language Development System for 8080 and Z-80**

The Program Development System (PDS) is an assembly language development system for 8080 or Z-80 microcomputers with at least one disk drive. PDS is said to include a unified assembler/editor, a macro assembler combining the features of a relocating linker loader, a string oriented text editor, and a trace debugger/diassembler. The assemblers favor the Intel instruction mnemonics treating the Z-80 superset as a logical and syntactical extension. Source modules are available for floating point arithmetic, floating point IO, trigometric functions, numerical and alphabetic sorting, disk I/O, integer I/O, 100 line program, fast Fourier transform, and a full function expression evaluator. For further information contact Allen Ashley, 395 Sierra Madre Villa, Pasadena CA 91107.

**Software for Users of North Star BASIC**

A series of programs for users of North Star BASIC is available on North Star diskette with user instructions. Word processing, investments, inventory and other business oriented programs are offered. A complete catalog of North Star software is now available, including not only California Software material, but programs available from firms around the world. For further information contact California Software, POB 275, El Cerrito CA 94530.
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Apple BASIC Instructions... 

It is typically printed on the matrix printer and reproduced photographically as white on black to emphasize the image of a television screen. Full color reproduction is used for the several pages where actual Apple II output to a color TV is given.

The manual begins with an introduction on the basics of the hardware and its interconnection. There is a description of the built-in 5 K Integer BASIC. The introduction concludes with operation of one of the standard games supplied on cassette with the machine. Breakout. The next chapter is entitled Beginning BASIC, which in turn is followed by Elementary Programming. The formal presentation ends with Strings, Arrays and Subroutines as the last chapter. Several appendices complete the book. Photo 2 illustrates several points about the Apple II BASIC Programming Manual. First, note the light type and the heavy type in the photograph. The lighter printing is green in the original, the heavier printing is black. Second, there is Jef Raskin's inimitable sense of humor which makes the manual an enjoyable experience. Look at page 24 of the Apple II BASIC Programming Manual at a local computer store for one of the most elegant modifications of a standard typing test string ever seen. (The string begins "THE QUICK BROWN FOX . . ." and in its original form is known to everyone, but in its modified form shows a certain humorous familiarity with the urban geography of the northeastern United States.)

While not a reference document by intent, users of Apples will find much information and a verbal delight in the form of this BASIC manual by Jef Raskin... 

Software for the North Star Disk System

According to its developers, the Comprehensive Mailing List Program Package, #ML-1NS, is a modular program set which enables the user to start and maintain one or more mailing lists. Operations include: add, delete, search, sort, auto-sort, and sequential printout. Features include: user selectable defaults for ease of entry, user selectable number of labels across page for different printers and label sheets, and user selectable 3 or 4 line address for each independent entry. The software is available with documentation and diskette for $25 from Williams Radio and TV Inc, Computer Division, 2052 Liberty St, POB 3314, Jacksonville FL 32206. 

Utility Package for North Star Micro Disk System

A complete disk utility package for the North Star Micro Disk System is now said to be available from Micro Logistics, POB 922, Madison Square Station, New York NY 10010. PKGUT1 on diskette includes the following four 8080 machine language programs originated at 0: Packit: packs and unpacks disk files so you can get more storage per disk; Changlit: prints, dumps and/or changes data in disk files up to a global level; Sortit: a generalized sorting utility; Compit: file comparison utility which will compare disk files sequentially or by key and display differences. Diskette with full user's documentation is priced at $80.

EMPI Interpreter for 8080

EMPL is a micro version of APL for the Intel 8080. It resides in the first 5632 bytes of memory. EMPL has numeric and character vectors, user defined niladic, monadic and dyadic functions, 22 primitive functions and nine system commands. It can be run either in the ASCII or APL character set. The range is ±32767 and double byte integer arithmetic is used. EMPL comes with a user's manual that includes information on implementing it on any system using Z-80 or 8080 processors with at least 8 K of memory. EMPL is $10 on Tarbell cassette; $20 on paper tape, North Star disk, CUTS cassette, or MITS cassette from Erik T Mueller, Britton House, Roosevelt NJ 08555.

Photo 1.

Photo 2.

Circle 598 on inquiry card.

Circle 599 on inquiry card.

Circle 597 on inquiry card.

Circle 600 on inquiry card.
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1/2" high LED Display uses 3V battery. LED Display with Alarm, and snooze function. Direct drive. Use in Pin-on plug, un-wire with Garnet Abbram, Power and L.O.I.
SUITE $2.95 or $16.00

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1/2" high LED Display uses 3V battery. LED Display with Alarm, snooze function. Direct drive. Use in Pin-on plug, un-wire with Garnet Abbram, Power and L.O.I.
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22 pin* $8.30 $7.60 $7.00 $6.30 $6.30 $6.30
24 pin* $9.80 $8.40 $7.80 $6.80 $6.80 $6.80
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Compact Yet Versatile

The ZMS-70 contains a microcomputer system with up to 64 K bytes of memory, a 15 inch diagonal video display, an extensive keyboard, a telecommunications interface and 143 K bytes of on line disk storage. An optional internal hard copy printer interface and external printer is also available. The system is said to include an extensive set of software for both application program development and the day to day operational use of the system. This software comprises a general purpose disk based executive, a file manager, and a complete assembly language development package. In addition, a full set of test, diagnostic and utility programs are provided. Price is less than $5000 from Zentec Corp, 2400 Walsh Av, Santa Clara CA 95050.

Circle 588 on inquiry card.

Sirius II Complete Computer System

The Sirius II computer system features two processors: the Mostek Z-80 for main computations and a Fairchild 3870 that handles all keyboard and video interfacing. Also included are 32768 K bytes of programmable memory, an RS-232 interface for IO, 8192 K bytes of programmable read only memory with a 1 K byte monitor supplied, minifloppy disk drive, a 64 key keyboard with alphanumeric and graphic capabilities, and a video interface. Other features include a full disk operating BASIC Interpreter, monitor and software programs ranging from home management, personal finance, educational learning programs and process control to business software and games.

The Sirius II sells for $1850. For more information contact Digital Sport Systems, 7th and Elm Sts, West Liberty IA 52776.

Circle 590 on inquiry card.

A New Desktop System

This new microcomputer system, designated System 88, is designed for professional and small business problem solving. The hardware consists of a main unit, upper and lower case keyboard with control keys, and quick updating video monitor. Hardware features include full eight level vectored interrupts and full graphics. The main unit uses an 8080 processor and accommodates from one to three minifloppy drives. The system includes complete operating software on disk plus word processor, BASIC and assembler. Software features include: system software with a file system and built-in application aids; BASIC on disk that has multidimensional strings and numeric arrays, MAT statement, PLOT statement to support graphics, program CHAINing, variable cross-reference listing by line number, inverse trigonometric functions, array functions SUM, PROD, MEAN, STD; text editor; integral RS-232 printer interface; and complete macroassembler on disk. The main unit of the System 88 has a walnut cabinet with a brushed aluminum front panel. Price for the system, excluding printer, starts at $2795. Contact PolyMorphic Systems, 460 Ward Dr, Santa Barbara CA 93111.

Circle 589 on inquiry card.
**What's New?**

**System Memory Interface Forms**

2 Chip Microcomputer

A single integrated circuit for microprocessor interfaces which incorporates its own memory, internal timing and IO ports is now available from Signetics. The 2656 system memory interface (SMI) can be combined with the Signetics 2650 processor to form a 2 chip microcomputer that provides system flexibility and additional memory and IO port expansion capabilities. The unit is useful for applications where both reduced chip count and system flexibility are necessary.

The Signetics SMI is a mask programmable circuit that offers 2 K by 8 bit programmable read only memory, 128 by 8 bit static random access memory, eight multipurpose IO pins for external chip select or IO data port bits, an 8 bit latch for output data, and an internal clock generator programmed with crystal, RC or external input.

As an aid to system designers Signetics offers an SMI emulator on a single PC card that duplicates all the functional capabilities of the 2656 SMI chip. The emulator is priced at $250. The SMI chip is available in quantities of 1000 for $17. Contact Signetics, POB 9052, 811 E Arques Av, Sunnyvale CA 94086.

**Hexadecimal Label Switches Break Keyboard Cost Barriers**

Stuck on any panel by its self-adhering backing, this microprofile keyboard avoids the congestion and the mounting hardware difficulties of mechanical keyboards. Label switches produce matrix coded output directly and will interface directly with integrated circuit 74C922 for conversion to a binary code. Labels do not bounce and so do not require the usual debounce electronics. Label switches are gold plated inside and outside and are sealed against the entry of dust or soft drinks. Life is estimated at 100 million operations. A self-contained flexible cable plugs into standard 0.1 inch (2.54 mm) spacing socket. Price is $3.95 in single quantities from Comptronics Engineering, 7235 Hollywood Blvd, Hollywood CA 90046.

**Optical Comparator for Rapid PC Board Inspection**

An optical comparator for inspection of printed circuit boards or other flat electrical and mechanical assemblies is now available from TM Systems Inc, 25 Allen St, Bridgeport CT 06604. The Model 1013 optical comparator is a fully portable, compact device which optically compares production circuit boards with a master or standard assembly. Both boards are placed in the comparator and alternating images are superimposed for viewing by the inspector. Any errors are immediately identified and located. An image sequence from 1 to 10 per second can be front panel selected and the illumination intensity is infinitely variable. The comparator features all solid state electronics and is designed for operation under all lighting conditions at any assembly station. Power requirements are 115 V ±10%, 50/60 Hz, at 1 A.

**Easy to Interface Chip Select USART**

This Astro universal synchronous asynchronous receiver transmitter (USART), the UC 1971 Astro-Chip Select, is now available from Western Digital, 3128 Red Hill Av, POB 2180, Newport Beach CA 92663. This UC 1971 has many of the features of Western Digital's UC 1671 Astro Multiplexed Address: biosynchronous, asynchronous or isochronous modes, double buffered receiver and transmitter data, convenient interface to data sets and parallel processors. The UC 1971 Astro will interface with all popular microprocessors on the market.

The UC 1971, now second sourced, features the generalized computer interface control signals CS, AO, A1, RE and WE. Another design and operational plus for the UC 1971 Astro is the receiver clock and last transmitter bit outputs for external CRC generation and checking. The operating speed is DC to 1 M bps. For further information and price contact Western Digital.

**New .6 Inch LEDs from IEE**

A line of red .63 inch LED digital displays designated as IEE-Hercules Series 1800 has been announced by Industrial Electronic Engineers Inc, 7740 Lemona Av, Van Nuys CA 91405. Series 1800 includes high brightness, dual element models and also single element models. The dual element LEDs consist of two chips of light emitting material which are electrically interconnected in series and act functionally as single segments. Both types of red LEDs have wide angle and long distance viewing with a high contrast ratio. Common anode and common cathode versions are available with right-hand and left-hand decimal points and ±11 overflow. Series 1800 LEDs are directly interchangeable with Litronix. At the 500 piece level, prices range from $1.65 each for single element to $1.88 each for dual element.

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**Ink Blotter**

- The 2656 system memory interface (SMI) can be combined with the Signetics 2650 processor to form a 2 chip microcomputer that provides system flexibility and additional memory and IO port expansion capabilities. The unit is useful for applications where both reduced chip count and system flexibility are necessary.

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- **Circle 612 on Inquiry card.**
- **Circle 613 on Inquiry card.**

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**Addresses**

- **Signetics**
  - Address: 74 Hollywood Blvd, Hollywood CA 90046
  - Contact Signetics, POB 9052, 811 E Arques Av, Sunnyvale CA 94086

- **Comptronics Engineering**
  - Address: 7235 Hollywood Blvd, Hollywood CA 90046
  - Price: $3.95 in single quantities

- **TM Systems Inc**
  - Address: 25 Allen St, Bridgeport CT 06604
  - Model: Model 1013
  - Features: portable, compact, matrix coded output

- **Western Digital**
  - Address: 3128 Red Hill Av, POB 2180, Newport Beach CA 92663
  - Device: UC 1971 Astro-Chip Select
  - Features: biosynchronous, asynchronous, isochronous modes, double buffered receiver and transmitter data, convenient interface

- **IEEE-Hercules Series 1800**
  - Address: 7740 Lemona Av, Van Nuys CA 91405
  - Features: high brightness, dual element, single element, right-hand, left-hand decimal points, ±11 overflow

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**Further Information**

- Contact Western Digital for further information and price.

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**Ink Blotter**

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- **Circle 612 on Inquiry card.**
- **Circle 613 on Inquiry card.**
**THE 100 BUS DIAGNOSTIC BOARD CENTURION IV**

A LEGION OF DIAGNOSTIC TOOLS ON ONE BOARD!

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<thead>
<tr>
<th>EXTENDER BOARD</th>
<th>PULSE DETECTOR</th>
<th>LOGIC PROBE</th>
<th>CURRENT SHUNT</th>
</tr>
</thead>
<tbody>
<tr>
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WITH THIS BOARD YOU CAN BEGIN WITH JUST 8K OR MEMORY AND ADD ON AS MANY 32K'S AS INSURING THERE MEMORY CHIPS CAN耐P

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- POWERED IN 2 VOLTAGE LEVELS EACH ON A SEPARATE POWER SUPPLY
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BYTE September 1978 207
### Inquiry No. Page No.

<table>
<thead>
<tr>
<th>Inquiry No.</th>
<th>Page No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AAA Chicago Computer Center 146</td>
</tr>
<tr>
<td>2</td>
<td>Administrative Systems 125</td>
</tr>
<tr>
<td>3</td>
<td>Advanced Interactive Systems 176</td>
</tr>
<tr>
<td>4</td>
<td>AJA Software 150</td>
</tr>
<tr>
<td>5</td>
<td>Anderson Jackson 31</td>
</tr>
<tr>
<td>6</td>
<td>Apparat Inc 176</td>
</tr>
<tr>
<td>7</td>
<td>Apple Computer 14</td>
</tr>
<tr>
<td>8</td>
<td>Apple Computer 15</td>
</tr>
<tr>
<td>9</td>
<td>Atlas Electronics 128</td>
</tr>
<tr>
<td>10</td>
<td>ATV Research 169</td>
</tr>
<tr>
<td>11</td>
<td>Atwood Enterprises 199</td>
</tr>
<tr>
<td>12</td>
<td>AVR Electronics 197</td>
</tr>
<tr>
<td>13</td>
<td>Basic Computer Shop 176</td>
</tr>
<tr>
<td>14</td>
<td>Bazzy Electronics 176</td>
</tr>
<tr>
<td>15</td>
<td>Beckian Enterprises 192</td>
</tr>
<tr>
<td>16</td>
<td>Beta Business 197</td>
</tr>
<tr>
<td>17</td>
<td>BITS 95</td>
</tr>
<tr>
<td>18</td>
<td>BITS 109</td>
</tr>
<tr>
<td>19</td>
<td>BITS 111</td>
</tr>
<tr>
<td>20</td>
<td>BITS 196</td>
</tr>
<tr>
<td>21</td>
<td>Biz Comp '78 144</td>
</tr>
<tr>
<td>22</td>
<td>Buss 88</td>
</tr>
<tr>
<td>23</td>
<td>* BYTE Books 77-80</td>
</tr>
<tr>
<td>24</td>
<td>* BYTE Wats Line 175</td>
</tr>
<tr>
<td>25</td>
<td>California Digital 185</td>
</tr>
<tr>
<td>26</td>
<td>Canada Systems 139</td>
</tr>
<tr>
<td>27</td>
<td>Central Data 51</td>
</tr>
<tr>
<td>28</td>
<td>Computalk 49</td>
</tr>
<tr>
<td>29</td>
<td>Computer Age 176</td>
</tr>
<tr>
<td>30</td>
<td>Computer Corner 169</td>
</tr>
<tr>
<td>31</td>
<td>Computer Enterprises 127</td>
</tr>
<tr>
<td>32</td>
<td>Computer Factory 151</td>
</tr>
<tr>
<td>33</td>
<td>Computer Hardware Store 169</td>
</tr>
<tr>
<td>34</td>
<td>Computerland 5</td>
</tr>
<tr>
<td>35</td>
<td>Computer Pantry 169</td>
</tr>
<tr>
<td>36</td>
<td>Computer Resources 137</td>
</tr>
<tr>
<td>37</td>
<td>Contemporary Marketing 55</td>
</tr>
<tr>
<td>38</td>
<td>Cromemco 1, 2</td>
</tr>
<tr>
<td>39</td>
<td>Digital Pathways 143</td>
</tr>
<tr>
<td>40</td>
<td>Digital Research (CA) 91</td>
</tr>
<tr>
<td>41</td>
<td>Digital Research (TX) 187</td>
</tr>
<tr>
<td>42</td>
<td>Digital Research &amp; Eng 165</td>
</tr>
<tr>
<td>43</td>
<td>Disc 3 169</td>
</tr>
<tr>
<td>44</td>
<td>Dynabyte 89</td>
</tr>
<tr>
<td>45</td>
<td>Electrolobe 180</td>
</tr>
<tr>
<td>46</td>
<td>Electronic Control Technology 140</td>
</tr>
<tr>
<td>47</td>
<td>Electronic Systems 189</td>
</tr>
<tr>
<td>48</td>
<td>Electronic Warehouse 191</td>
</tr>
<tr>
<td>49</td>
<td>Emerge Systems 197</td>
</tr>
<tr>
<td>50</td>
<td>EMM/CMP 130</td>
</tr>
<tr>
<td>51</td>
<td>Essex Publishing 144</td>
</tr>
<tr>
<td>52</td>
<td>Forthought Products 119</td>
</tr>
</tbody>
</table>

### Inquiry No. Page No.

<table>
<thead>
<tr>
<th>Inquiry No.</th>
<th>Page No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>142</td>
<td>Functional Automation 136</td>
</tr>
<tr>
<td>143</td>
<td>Godbout Electronics 61, 81</td>
</tr>
<tr>
<td>144</td>
<td>GRT 134, 135</td>
</tr>
<tr>
<td>145</td>
<td>H &amp; K Computer Corp 163</td>
</tr>
<tr>
<td>146</td>
<td>Hamilton Logic Systems 169</td>
</tr>
<tr>
<td>147</td>
<td>DC Hayes 162</td>
</tr>
<tr>
<td>148</td>
<td>Hobby World 179</td>
</tr>
<tr>
<td>149</td>
<td>IMSAI 6, 11</td>
</tr>
<tr>
<td>150</td>
<td>Info 2000 97</td>
</tr>
<tr>
<td>151</td>
<td>Information Terminals 99</td>
</tr>
<tr>
<td>152</td>
<td>Integrated Circuits Unlimited 193</td>
</tr>
<tr>
<td>153</td>
<td>Integrated Technology 176</td>
</tr>
<tr>
<td>154</td>
<td>International Data Sciences 145</td>
</tr>
<tr>
<td>155</td>
<td>Ithaca Audio 183</td>
</tr>
<tr>
<td>156</td>
<td>Jade Company 181</td>
</tr>
<tr>
<td>157</td>
<td>Jameco 194, 195</td>
</tr>
<tr>
<td>158</td>
<td>Lifeboat Associates 119, 150</td>
</tr>
<tr>
<td>159</td>
<td>LMM Electronics 205</td>
</tr>
<tr>
<td>160</td>
<td>Logical Services 133</td>
</tr>
<tr>
<td>161</td>
<td>Manchester Equipment 67</td>
</tr>
<tr>
<td>162</td>
<td>The Math Box 197</td>
</tr>
<tr>
<td>163</td>
<td>Maxi-Switch 59</td>
</tr>
<tr>
<td>164</td>
<td>Micro Madness 197</td>
</tr>
<tr>
<td>165</td>
<td>Micro Mail 124</td>
</tr>
<tr>
<td>166</td>
<td>Micromation 66</td>
</tr>
<tr>
<td>167</td>
<td>Microelectronics 125</td>
</tr>
<tr>
<td>168</td>
<td>Microprocessor 121</td>
</tr>
<tr>
<td>169</td>
<td>Mikos 205</td>
</tr>
<tr>
<td>170</td>
<td>Morrow/Thinker Toys 25</td>
</tr>
<tr>
<td>171</td>
<td>Mountain Hardware 54</td>
</tr>
<tr>
<td>172</td>
<td>Mpi 161</td>
</tr>
<tr>
<td>173</td>
<td>Mullen Computer Boards 140</td>
</tr>
<tr>
<td>174</td>
<td>National Multiplex 83</td>
</tr>
<tr>
<td>175</td>
<td>Netronics 129</td>
</tr>
<tr>
<td>176</td>
<td>New England Electronics 142</td>
</tr>
<tr>
<td>177</td>
<td>New England Recruiters 176</td>
</tr>
<tr>
<td>178</td>
<td>North Star 7, 27</td>
</tr>
<tr>
<td>179</td>
<td>Northwest Microcomputer Sys 71</td>
</tr>
<tr>
<td>180</td>
<td>Ohio Scientific Instrument 18-21</td>
</tr>
<tr>
<td>181</td>
<td>OK Machine &amp; Tool 131</td>
</tr>
<tr>
<td>182</td>
<td>Oliver Advanced Engineering 165, 197</td>
</tr>
<tr>
<td>183</td>
<td>On-Line 163</td>
</tr>
<tr>
<td>184</td>
<td>Osborne &amp; Associates 107</td>
</tr>
<tr>
<td>185</td>
<td>Owens 141</td>
</tr>
<tr>
<td>186</td>
<td>Pacific Digital 158</td>
</tr>
<tr>
<td>187</td>
<td>Pacific Office Systems 180</td>
</tr>
<tr>
<td>188</td>
<td>Page Digital 188</td>
</tr>
<tr>
<td>189</td>
<td>PAIA Electronics 158</td>
</tr>
<tr>
<td>190</td>
<td>PanaVise 126</td>
</tr>
<tr>
<td>191</td>
<td>PCE Electronics 169</td>
</tr>
<tr>
<td>192</td>
<td>Per Com Data 32</td>
</tr>
<tr>
<td>193</td>
<td>Per &amp; Small Business Cmpt Show 101</td>
</tr>
</tbody>
</table>

### Article No. ARTICLE PAGE

<table>
<thead>
<tr>
<th>Article No.</th>
<th>ARTICLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Postdamar: The Mathematics of Computer Graphics</td>
<td>22</td>
</tr>
<tr>
<td>2</td>
<td>Kellerman: APL and Graphics</td>
<td>40</td>
</tr>
<tr>
<td>3</td>
<td>Chung-Yuen: A &quot;Tiny&quot; Pascal Compiler</td>
<td>58</td>
</tr>
<tr>
<td>4</td>
<td>Hearm: Some Words About Program Structure</td>
<td>68</td>
</tr>
<tr>
<td>5</td>
<td>Williams: Antique Mechanical Computers: Part 3</td>
<td>82</td>
</tr>
<tr>
<td>6</td>
<td>Ciarcia: Let Your Fingers Do the Talking: Part 2</td>
<td>94</td>
</tr>
<tr>
<td>7</td>
<td>Bondy: S2L: An Altair (S-100) to LSI-11 Bus Adapter</td>
<td>102</td>
</tr>
<tr>
<td>8</td>
<td>Boney: Math in the Real World</td>
<td>114</td>
</tr>
<tr>
<td>9</td>
<td>Hungerford: Graphic Manipulations Using Matrices</td>
<td>156</td>
</tr>
<tr>
<td>10</td>
<td>Keriasty: WADUZITDO: How To Write a Language</td>
<td>166</td>
</tr>
</tbody>
</table>

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Two "car" oriented articles were at the top of the June 1978 BOMB results. First prize of $100 goes to Steve Ciarcia for his article "Talk to Me: Add a Voice to Your Computer for $35," page 142. The $50 second prize goes to Bill Georgiou for "Give an Ear to Your Computer," page 56. The two articles placed 1.6 and 1.3 standard deviations above the mean, respectively.
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