Now SWTPC offers complete best-buy computer system with $995 dual minifloppy, $500 video terminal/monitor, $395 4K computer.

$995 MF-68 Dual Minifloppy
You need dual drives to get full benefits from a minifloppy. So we waited to offer a floppy until we could give you a dependable dual system at the right price.

The MF-68 is a complete top-quality minifloppy for your SWTPC Computer. The kit has controller, chassis, cover, power supply, cables, assembly instructions, two highly reliable Shugart drives, and a diskette with the Floppy Disk Operating System (FDOS) and disk BASIC. (A floppy is no better than its operating system, and the MF-68 has one of the best available.) An optional $850 MF-6X kit expands the system to four drives.

$500 Terminal/Monitor
The CT-64 terminal kit offers these premium features: 64-character lines, upper/lower case letters, switchable control character printing, word highlighting, full cursor control, 110-1200 Baud serial interface, and many others. Separately the CT-64 is $325, the 12 MHz CT-VM monitor $175.

$395 4K 6800 Computer
The SWTPC 6800 comes complete with 4K memory, serial interface, power supply, chassis, famous Motorola MIKBUG* mini-operating system in read-only memory (ROM), and the most complete documentation with any computer kit. Our growing software library includes 4K and 8K BASIC (cassettes $4.95 and $9.95, paper tape $10.00 and $20.00). Extra memory, $100/4K or $250/8K.

Other SWTPC peripherals include $250 PR-40 Alphanumeric Line Printer (40 characters/line, 5 x 7 dot matrix, 75 line/minute speed, compatible with our 6800 computer and MITS/MSAI); $79.50 AC-30 Cassette Interface System (writes/reads Kansas City standard tapes, controls two recorders, usable with other computers), and other peripherals now and to come.

Enclosed is:

1. $1,990 for the full system shown above
   - (MF-68 Minifloppy, CT-64 Terminal with CT-VM Monitor)
   - $995 for the Dual Minifloppy
   - $325 for the CT-64 Terminal
   - $175 for the CT-VM Monitor
   - $395 for the 4K 6800 Computer
2. $250 for the PR-40 Line Printer
3. $79.50 for AC-30 Cassette Interface
4. Additional 4K memory boards at $100
5. Additional 8K memory boards at $250
6. Or BAC # _______ Exp Date _______
7. Or MC # _______ Exp Date _______

Name __________________ Address __________
City __________ State __ Zip __________
You can now have the industry's finest microcomputer with that all-important disk drive

YOU CAN GET THAT ALL-IMPORTANT SOFTWARE, TOO

Loading your programs and files will take you only a few seconds with the new Cromemco Z-2D computer. You can load fast because the Z-2D comes equipped with a 5” floppy disk drive and controller. Each diskette will store up to 92 kilobytes. Diskettes will also store your programs inexpensively—much more so than with ROMs. And ever so much more conveniently than with cassettes or paper tape.

The Z-2D itself is our fast, rugged, professional-grade Z-2 computer equipped with disk drive and controller. You can get the Z-2D with either single or dual drives (dual shown in photo).

CROMEMCO HAS THE SOFTWARE

You can rely on this: Cromemco is committed to supplying quality software support.

For example, here’s what’s now available for our Z-2D users: CROMEMCO FORTRAN IV COMPILED: a well-developed and powerful FORTRAN that’s ideal for scientific use. Produces optimized, relocatable Z-80 object code.

CROMEMCO 16K DISK BASIC: a powerful pre-compiling interpreter with 14-digit precision and powerful I/O handling capabilities. Particularly suited to business applications.

CROMEMCO Z-80 ASSEMBLER: a macro-assembler that produces relocatable object code. Uses standard Z-80 mnemonics.

ADVANCED CONTROLLER CARD

The new Z-2D is a professional system that gives you professional performance.

In the Z-2D you get our well-known 4-MHz CPU card, the proven Z-2 chassis with 21-slot motherboard and 30-amp power supply that can handle 21 cards and dual floppy drives with ease.

Then there’s our new disk controller card with special features:
- Capability to handle up to 4 disk drives
- A disk bootstrap Monitor in a 1K 2708 PROM
- An RS-232 serial interface for interfacing your CRT terminal or teletype
- LSI disk controller circuitry

Z-2 USERS:

Your Z-2 was designed with the future in mind. It can be easily retrofitted with everything needed to convert to a Z-2D. Only $935 kit; or $1135 for assembled retrofit package.

Cromemco Incorporated
Specialists in computers and peripherals
2400 CHARLESTON RD., MOUNTAIN VIEW, CA 94043 • (415) 964-7400

Cromemco
We're able to put all of this including a UART for the CRT interface on just one card because we've taken the forward step of using LSI controller circuitry.

STORE/FACTORY

Contact your computer store or Cromemco factory now about the Z-2D. It's a real workhorse that you can put to professional or OEM use now.

Kit: Z-2D with 1 disk drive
   (Model Z2D-K) .................. $1495.

Assembled: Z-2D fully assembled and tested (Model Z2D-W) .... $2095.

Additional disk drive
   (Model Z2D-FDD) ............. $495.

SOFTWARE

(On standard IBM-format soft-sectored mini diskettes)
16K BASIC (Model FDB-5) ........ $95

FORTTRAN IV (Model FDF-5) .... $95

Z-80 Assembler (Model FDA-5) ... $95

Circle 40 on inquiry card.
Your computer's usefulness depends on the capability of its CPU, memories, and I/O interfaces, right?

So here's a broad line of truly useful computer products that lets you do interesting things with your Cromemco Z-1 and Z-2 computers. And with your S-100-compatible Altairs and IMSAls, too.

**CPU**
- **Z-80 MICROPROCESSOR CARD.** The most advanced µP card available. Forms the heart of our Z-1 and Z-2 systems. Also a direct replacement for Altair/IMSAI CPUs. Has 4-MHz clock rate and the power of the Z-80 µP chip. Kit (Model ZPU-K): $295. Assembled (Model ZPU-W): $395.
- **16K RAM.** The fastest available. Also has bank-select feature. Kit (Model 16KZ-K): $495. Assembled (Model 16KZ-W): $795.
- **THE BYTESAVER—** an 8K capacity PROM card with integral programmer. Uses high-speed 2708 erasable PROMs. A must for all computers. Will load 8K BASIC into RAM in less than a second. Kit (Model BSK-O): $145. Assembled (Model BSW-0): $245.
- **16K CAPACITY PROM CARD.** Capacity for up to 16K of high-speed 2708 erasable PROM. Kit (Model 16KPR-K): $145. Assembled (Model 16KPR-W): $245.

**I/O INTERFACES**
- **FAST 7-CHANNEL DIGITAL-ANALOG I/O.** Extremely useful board with 7 A/D channels and 7 D/A channels. Also one 8-bit parallel I/O channel. Kit (Model D + 7A-K): $145. Assembled (Model D + 7A-W): $245.
- **DIGITAL INTERFACE (OUR NEW TU-ART).** Interfaces with teletype, CRT terminals, line printers, etc. Has not one but two serial I/O ports and two 8-bit parallel I/O ports as well as 10 on-board interval timers. Kit (Model TRT-K): $195. Assembled (Model TRT-W): $295.
- **JOYSTICK.** A console that lets you input physical position data with above Model D + 7 A/D card. For games, process control, etc. Contains speaker for sound effects. Kit (Model JS-1-K): $65. Assembled (Model JS-1-W): $95.

**PROFESSIONAL QUALITY**
You get first-class quality with Cromemco.

Here are actual quotes from articles by independent experts: "The Cromemco boards are absolutely beautiful" . . . "The BYTESAVER is tremendous" . . . "Construction of Cromemco I/O and joystick are outstanding" . . . "Cromemco peripherals ran with no trouble whatsoever."

Everyone agrees. Cromemco is tops.

**STORES/MAIL**
So count on Cromemco. Look into these Cromemco products at your store. Or order by mail from the factory.

We wish you pleasure and success with your computer.
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Cover by Bruce Holloway
In this issue, author Steve Ciarcia begins what we expect to become a regular feature in BYTE: Ciarcia's Circuit Cellar. Steve, a senior engineering consultant to the aerospace industry by profession, is a rare combination of writer and tinkerer. The conceptual model he brings to his interactive column format is that of the late C. L. Stong's stewardship of "The Amateur Scientist" in *Scientific American*, but with an emphasis on hardware and software combinations to accomplish interesting applications of personal computing systems. Steve welcomes feedback from readers...CH

Games and models which employ moving objects require some attention to details of motion as simulated by a computer program. Beginning a series of articles on the subject of moving objects, Stephen P. Smith's *Simulation of Motion: An Improved Lunar Lander Algorithm* shows how a real time game can incorporate models of motion in more than one dimension.

Donald T. Piele shows that a computer fair doesn't have to be big to be good. *A Mini-computer Fair: Tiny and Personal* describes the University of Wisconsin's efforts to produce their own micro extravaganza, which drew over 700 attendees. Readers may get some ideas about putting on shows of their own based on Professor Piele's experiences.

What might not be appreciated by the neophyte is the fact that an interrupt driven clock suggests other uses besides keeping time. In M. F. Smith's article on *Using Interrupts for Real Time Clocks* you'll find a simple timekeeping algorithm, and a sketch of how it can be extended to share processor time between two different processes.

Do you occasionally find incorrect data in your computer when you know you entered the correct information and processed it with a reliable program? Does your computer do strange things every time the washing machine or furnace turns on? Perhaps your problem is voltage transients. John McCain writes about *Spikes: Pesky Voltage Transients and How to Minimize Their Effects*.

If you want to post a calendar of events in your computer's memory with a resolution of 1 second, a mere three integrated circuits added to an existing LSI digital clock can turn it into a source of time information for your computer. Use Robert Grappel's article in this issue to find an answer to the metaphorical question: "Does Anybody Know What Time It Is?"

Any regular source of interrupts can be used as the key element in a simple real time clock for the typical personal computer. James R. Sneed shows how to create such an interrupt source, then program a 6502 to generate internal variables for hours, minutes, seconds and 1/15th seconds of the day in his article on *Adding an Interrupt Driven Real Time Clock*.

If you do a lot of mathematical calculations on your microcomputer, you'll enjoy reading *Floating Point Arithmetic* by Burt Hashizume. Find out how to add an economical floating point package to your system and improve your number crunching facilities.

An excellent way to learn about computers is to build one yourself. Hilary D. Jones shows that this is not such a terrifying task. *Read Building a Computer From Scratch* and find out how to construct a working (albeit limited) computer for under $70 (plus the price of a power supply).

Occasionally readers ask for detail plans of computer systems. David Brader, a BYTE reader from Electric City, WA, has implemented an excellent piece of homebrew craftsmanship in his Kompuutar system based on the MOS Technology 6502 processor. In this issue, we provide David's complete design for the central processor, control panel interface, and serial terminal interface of a general purpose computer.

Frequency counters are useful tools for a variety of applications. Perry Lynne shows you how to add one to your microcomputer in *Implementing an LSI Frequency Counter*. His design takes advantage of the Intel 8253 programmable interval timer (as well as the power of the microprocessor) to produce a design that is both accurate and economical.

How do you make an 8 bit machine emulate a more comprehensive design? In his article, *SWEET16: The 6502 Dream Machine*, Stephen Wozniak details the design and functions of a low level interpreter for 16 bit operations which extend the functions of the more limited 8 bit 6502 processor.

Continuing the theme of real time and how to keep track of it, G. A. R. Trollope provides an example of the interrupt driven approach, implemented through the IRQ interrupt line of a 6800 processor with a PIA port. *Do You Need Real Time? If so, turn to this article.*

The game of NIM is well-known in the annals of computer lore, but many people have had no contact with it. Irwin Doliner presents us with a version of the game and supplies us with the design theory behind it in his article, *NIMBLE: The Ultimate NIM*.
You want to record your message verbatim—word for word—whether it's bits, bytes or "Dear Folks" translated into word processor language.

Our objective in manufacturing recording media for the electronics industry—digital tape cassettes, floppy disks, mag cards, computer cartridges—is to give you the finest, the best, the most dependable, the most cost-effective.

That means rugged, long-lived, abrasion-resistant recording media with superior magnetic qualities. If we made tires, they'd be steel-belted radials.

We delivered our first digital grade certified tape cassettes back in the beginning, 1969. We made the first commercial 3740-compatible floppy disks that didn't bear IBM's name. And the first Flippy® reversible flexible disks with anyone's name on them. The first mini data cassette is ours. And we've got the newest miniature flexible disk, the MD 525.

Now, Verbatim media. It's a new formulation of ferric oxides, an advanced macromolecular binder system to adhere it to the tough polyester film, and a process control system that demands over 200 separate quality checks before the material is cut, packaged, and certified to be 100% error-free.

The final quality check? "Make it pretty!" Our production people tell us that magnetic recording media is one of the rare instances in manufacturing where aesthetic appearance translates directly into final product quality. It has to look beautiful to work beautifully.

We have the formulas, the machines, the technology to make high quality recording media. But it takes the best people in the industry to deliver Verbatim disks, cards, cartridges and cassettes. You'll find them at your favorite retail computer store.
On August 16 1977 I received one of those refreshing and intoxicating articles (or rather group of articles) which makes the combined intellectual and emotional joys of creating a magazine once a month rise to new heights. This group of articles is a basic background tutorial on biological inputs to the field of robotics and artificial intelligence, written for the personal computing experimenter by Ernest W Kent, a professor in the department of psychology of the University of Illinois at Chicago Circle. It is one of those articles, like Ralph Hollis' article on NEWT in the June 1977 BYTE, which gets instant high priority due to the subject matter and style of presentation. (Readers should see the beginning of the series in early 1978.)

I call the twin subjects of robotics and artificial intelligence "hot" ideas for BYTE based on reader interest as expressed in the BOMB poll's responses to Ralph Hollis' article on NEWT and Mike Wimble's articles (among others) on various artificial intelligence concepts. Inspired by receipt of Dr Kent's articles, the theme of this editorial is the concept of smart machines and related robotic mechanisms as a fertile field for experimentation with design and implementation. What are the categories and classes of experimentation which are relevant to artificial intelligence and robot design? Why are we (experimenters all) so fascinated by the simulation of life? What are the topics of study needed to become "the complete robotics experimenter?" What will we see over the course of the next decade or so, as personal computers become the refined personal software development systems needed to support private robotics research?

It often helps to draw inspiration from fiction, an element of our culture which has been present from its beginnings in the allegorical tales of primitive religions to the sophisticated and future oriented technological fiction tales of contemporary film, television and printed media. Fictional representations of plots, scenarios and tales are a sort of logical game practiced by creators, logical games with very real emotional and value orientations which stimulate thought about real problems while providing an interesting and enjoyable diversion for users of the art. Technological fiction, of which science fiction is a proper subset, is the appropriate contemporary place to turn for inspiration regarding the very contemporary possibility of ingenious and useful automations guided by artificial intelligence.

A particular science fiction tale which has been one of my greatest emotional inputs regarding the positive values of technology in human culture is a tale entitled Door Into Summer, by Robert Heinlein. First published in the 1950s, this now outdated tale of the near future (1970 is the year when the action commences with flashbacks to the fictional 1960s) is perhaps the one science fiction story which maps most closely to the current technological milieu of the smart machines made possible by microprocessor technology. Anyone who is seriously interested in practical use of robotic technology and smart machines should read this book as a source of background information and ideas about what is or might be possible. (The actual plot is a well constructed romantic tale in spite of its use of that logical trap which is the time travel deus ex machina.)

The inspiration to be drawn from the story of Door Into Summer is that of an exciting time when technology has advanced to the threshold of intelligent robotic mechanisms mass-produced for use in mundane tasks. It is the era of Drafting Dan (automated intelligent drafting machine), Hired Girl (automated housekeeping robot), and numerous similar specialized devices. Some of these fictional concepts have already been implemented in practice, especially in the area of automated aids to the production of capital goods. The idea of Drafting Dan, the intelligent drafting device, is actually in use on a small scale today but with a far higher degree of refinement and intelligence. I refer to the various computer aided design techniques utilizing graphic displays and computational support in fields as diverse as airplane design, computer design, and architecture. Others among the concepts in Robert Heinlein's story have yet to be implemented with any degree of perfection or widespread use.

The parallels between Door Into Summer and the current era are many. In the fictional account, technology has developed
The complete $655 line printer.

It's ready to plug in, has an 80-column format, a remarkable MTBF and is 14 times faster than a teletype!

Breaking the hardcopy barrier
It's finally happened! The Axiom EX-800 provides full performance hardcopy at a price compatible with today's low cost micros. This little 80-column machine zips along at 160 characters per second (14 times faster than a teletype)—at a breakthrough single quantity price of $655 for a complete printer.

When we say complete we mean it
The EX-800 is a stand-alone unit with case, power supply, 96 character ASCII generator and interface, paper roll holder, infra-red low paper detector, bell, and multi-line asynchronous input buffer. You won't find these standard features on any other printer, regardless of price!

Our only option
Our printer is so complete, that we offer only one option. A serial interface (RS 232C or current loop) good for 16 baud rates from 50 to 19,200 and thoughtfully provided with a switch for either Centronics or Tally compatibility. Might we call it a Tally-whacker? At $85.00 it certainly should be!

Built-in LSI microprocessor
The heart of the EX-800 is a printed circuit card, containing a custom LSI chip made by Intel to Axiom specifications, which controls all printer functions. Microprocessor power means flexibility. Such as the built-in self test routine and variable character size. It also means reliability. Several industry surveys have shown LSI to be many times more reliable than equivalent conventional circuitry.

The advantages of electrosensitive printing
The EX-800 can print 80, 40, or 20 characters across the five inch wide electrosensitive paper. Under software control, single characters or words may be printed larger for emphasis. The permanence of the hardcopy is archival, because once the aluminum coating has been removed, there is no way to put it back. It's unaffected by sunlight, moisture or heat. Although the printer doesn't provide multiple copies, excellent quality photocopies can be made from the high contrast printout. Also, the paper is inexpensive and readily available, costing about 1¢ for an 8½ x 11” equivalent.

Light, small, quiet, reliable, and versatile
Our EX-800 weighs in at 12 pounds, is just 9½ inches wide, 4 inches high, and 11 inches deep, and is delightfully quiet which makes it ideal for office and other low noise environments. The simple print mechanism is virtually maintenance free. In fact, tests show an incredible MTBF; many times greater than impact printers. This versatile printer is the ideal mate for micros, minis, CRTs, instruments and systems.

Just unbox and plug it in
That's all you have to do to the Axiom EX-800—apart from pay for it, and at $655 that's almost a pleasure.

AXIOM CORPORATION
5932 San Fernando Rd., Glendale, CA 91202 • (213) 245-9244 • TWX 910-497-2283

Circle 8 on inquiry card.
Check out TI's new 4K static RAMs. They've got everything you ever liked about the 2102. And more.

<table>
<thead>
<tr>
<th>SIMPLE TO USE</th>
<th>2102 1K Static RAM</th>
<th>TI's New 4K Static RAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>✔</td>
<td>✔</td>
<td>Like the popular 2102, TI's new 4K static RAMs are easy to use. Minimize system overhead; no refresh; simple addressing. It's easy!</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NO CLOCKS. NO TIMING STROBES.</th>
<th>2102 1K Static RAM</th>
<th>TI's New 4K Static RAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>✔</td>
<td>✔</td>
<td>No clocking needed for TI's fully static 4K RAMs. No edges. Just present an address to the selected device and data can be read at access time. That's it.</td>
</tr>
</tbody>
</table>
FULLY STATIC. ACCESS TIME = CYCLE TIME.

- Fully static RAMs are totally asynchronous. Require no precharge or recovery time. Access and cycle times are always the same.

DATA VALID—NO TIME LIMIT.

- Fully static RAMs offer output data that are valid as long as the address is valid. Makes designing straightforward. No limit on output valid time. No extra circuitry.

SINGLE +5 V SUPPLY. FULLY TTL COMPATIBLE.

- Just one +5 V supply needed. Full TTL compatibility on all inputs and outputs with full 400 mV guaranteed dc noise immunity.

+10% TOLERANCE SUPPLY.

- Improved power supply tolerance means less stringent regulation. Less cost.

HIGH SPEED.

- TI's new 4K statics take up where the 2102 left off. Offering a wide choice of speeds from 150 ns to 450 ns maximum access/minimum cycle. Plenty of performance to match today's and tomorrow's CPUs.

<table>
<thead>
<tr>
<th>Access/Cycle Time (ns)</th>
<th>4K x 1</th>
<th>1K x 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>150 ns</td>
<td>TMS 4044-15</td>
<td>TMS 4045-15</td>
</tr>
<tr>
<td>200 ns</td>
<td>TMS 4044-20</td>
<td>TMS 4045-20</td>
</tr>
<tr>
<td>250 ns</td>
<td>TMS 4044-25</td>
<td>TMS 4045-25</td>
</tr>
<tr>
<td>300 ns</td>
<td>TMS 4044-30</td>
<td>TMS 4045-30</td>
</tr>
<tr>
<td>450 ns</td>
<td>TMS 4044-45</td>
<td>TMS 4045-45</td>
</tr>
</tbody>
</table>

LOW POWER.

- Compare the power savings of the new 4K statics to the low power 21L02. For equivalent speed, the new TMS 4044 uses 63% less power.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Four Low Power 1K Static RAMs (2102AL-2)</th>
<th>One TI 4K Static RAM (TMS 4044-25)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Access</td>
<td>250 ns</td>
<td>250 ns</td>
</tr>
<tr>
<td>Min Cycle Operating Power (Max)</td>
<td>1358 mW</td>
<td>500 mW</td>
</tr>
<tr>
<td>4 x 16 pin Package(s) Board Area Ratio</td>
<td>3.7</td>
<td>1.0</td>
</tr>
</tbody>
</table>

HIGH DENSITY 18-PIN PACKAGE.

- The new 4K statics come in industry-standard, 18-pin packages, plastic or ceramic. A density improvement of almost four-to-one over 2102s.

FOR DATA SHEETS, application reports, price and delivery, call your nearest authorized TI distributor or TI field sales office.
I don't want to get into a fight over which microprocessor chip is better. They all have their favorable and unfavorable features. But, if you look a little closer, you may find that some of these extra features can be added with very little expense.

I was speaking with a fellow computer nut recently, and he was arguing about the merits of the 6800 versus the 8080. I really didn't care to continue the conversation nor to justify why I had an 8080 and Z-80. But, when he said that one reason was that the 6800 had memory mapped IO and the 8080 didn't, I knew he didn't know what it was.

This of course made me curious, and I approached a number of 8080 users to ask if they knew what memory mapped IO was. They assured me that they did, and that it was in fact one of the main features of the 6800. But such a feature is hardly exclusive to the 6800!

First of all, memory mapped IO means simply that a portion of memory address space has been reserved for interfacing with external devices. A byte of data is stored into a memory location, as always, but this storage unit, rather than being made up of 1024 bit programmable memory chips, is an

---

**Power Wiring Table**

<table>
<thead>
<tr>
<th>Number</th>
<th>Type</th>
<th>+5 VDC Pin</th>
<th>Gnd Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>7420</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC2</td>
<td>74154</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td>IC3</td>
<td>7407</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC4</td>
<td>7407</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC5</td>
<td>74100</td>
<td>24</td>
<td>7</td>
</tr>
</tbody>
</table>

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**Figure 1:** A schematic diagram for a direct addressed output port decoding circuit. The port assignments as diagrammed are from octal codes 360 to 377. The bus pin assignments are for the Digital Group bus system, but the Altair (S-100) bus is logically equivalent.
Intel delivers SDK-85. It's the quickest way to sink your teeth into 8085 design.

Intel wants you to prove to yourself why the 8085 has become the new industry standard microcomputer. To make it easy for you to do that, our System Design Kit for the 8085 is available now for only $250.

SDK-85 is the best way we know for you to evaluate MCS-85™ and develop prototypes of 8085-based designs, because it gives you a hands-on look at this important new microcomputer's capabilities.

And to simplify your evaluation, we've designed SDK-85 as a stand-alone kit. It comes complete with an integral keyboard for system control and data/program entry, and LED display output. To simplify programming, debugging and operation we've incorporated an onboard, ROM-resident software monitor.

The 8085 family of components provides you with unprecedented design flexibility. The basic three-chip, high level integration MCS-85 system is included in SDK-85. It includes the 8085 CPU, 8155 256-byte RAM with I/O and timer and 8355 2K-byte ROM with I/O. And there's an on-board single-chip keyboard/display interface, the 8279. Sockets are provided for easy RAM and ROM/EPROM expansion. And there's ample free space laid out for easy wire wrap expansion using Intel's complete family of programmable peripheral controllers and your own prototype logic and special circuitry.

SDK-85 makes an excellent teaching aid for both microprocessor design and programming courses, for microcomputer design seminars and as a project for the progressive hobbyist. Because the 8085 is the most advanced microcomputer, SDK-85 is the key to state-of-the-art knowledge.

SDK-85 can be assembled in just a few hours with a soldering iron and a few basic tools. Hook it up to your 5V power supply and it's operational the same day you receive it. You can get your SDK-85 from any of Intel's distributors for $250 in single unit quantities.


Or, for more information, use the reader service card or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone: (408) 246-7501.
8 bit storage register such as a 74100. This type of procedure provides access to the data byte through the “back door,” or output lines of the 74100. If you have followed me to this point, you can see that the concept of memory mapped I/O is applicable to any microprocessor that directly addresses memory! I don’t know of too many processors which operate without this ability, so we’ll just have to conclude that any microprocessor can be wired to provide memory mapped I/O, including the 8080.

Look no further! It’s a bird, . . . it’s a plane, . . . no, it’s Superchip! It looks like an 8080, acts like an 8080 and, while not trying to steal Motorola’s thunder, has memory mapped I/O! The name of this new chip? Well, it’s the plain old 8080 with an intelligent user.

Why should I consider memory mapped I/O?

The 8080 directly addresses 64 K bytes of memory and 512 I/O ports (256 in and 256 out). The only way data can arrive at an output port is by being passed through the accumulator and routed to a particular port by a 2 byte output instruction. Similarly, a 2 byte instruction directs input data to the accumulator. Additional programming is necessary to store this input byte in memory.
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Obviously, if the data path went to a memory location instead of an output port, a broader range of instructions would be available. The 8080 (like most computers) has some very powerful instructions when it comes to memory operations. For the 8080 these include MOV, MVI, STAX and STA instructions which, by definition, are added to the output data manipulation repertoire with memory mapped IO.

Often the best way to approach a new subject is to analyze the present method. Figure 1 illustrates the basic design of an 8080 output “port.” To emphasize simplicity I’ve used 74100 latches for this example rather than the more complex ports such as the Motorola 6820 peripheral interface adapter. This configuration provides 16 output strobes, starting with the octal output port address 360 and ending with octal 377. Integrated circuits 1 and 2 decode the address bus and, when provided with an output strobe during an output instruction, load the present contents of the data bus into an 8 bit storage register (IC5). ICs 3 and 4 provide buffering and allow more 74100s to be attached to the buffered output bus lines for multiple ports. The pin designations are for the Digital Group bus system, but the Altair (S-100) bus is logically equivalent.

Converting an output system to memory mapped IO (illustrated in figure 2) requires the addition of two more integrated circuits, ICs 6 and 7, to decode the additional eight lines associated with memory addressing. With the decoding arrangement illustrated in figure 2, the 16 output (memory) loca-

![Power Wiring Table](image)

<table>
<thead>
<tr>
<th>Number</th>
<th>Type</th>
<th>+5 VDC</th>
<th>Gnd</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>7420</td>
<td>14</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>IC2</td>
<td>74154</td>
<td>24</td>
<td></td>
<td>12</td>
</tr>
<tr>
<td>IC3</td>
<td>7407</td>
<td>14</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>IC4</td>
<td>7407</td>
<td>14</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>IC5</td>
<td>74100</td>
<td>24</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>IC6</td>
<td>7402</td>
<td>14</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>IC7</td>
<td>7420</td>
<td>14</td>
<td></td>
<td>7</td>
</tr>
</tbody>
</table>

Figure 2: A schematic diagram for a memory addressed output port decoding circuit. The port assignments in this case are from split field octal memory addresses 377/360 to 377/377. Here again, the bus pin assignments are for the Digital Group bus.
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Example 1: Output the contents of the B register to port r.

- **8080 Direct I/O**
  
  - MOV B, A ; Move the contents of the B register to the accumulator
  - OUT r ; Output the accumulator to port #r
  - Total bytes: 3
  - Total states: 15

- **Memory Mapped I/O**
  
  - LXI HL ; Set memory pointer HL
  - MOV M, B ; Move B register to memory location HL
  - Total bytes: 4
  - Total states: 17

For simple data manipulations like this, the direct I/O technique, which is familiar to all 8080 users, occupies less memory space.

Example 2: With two 8 bit digital to analog convertors attached to output registers, generate two sawtooth waveforms 180° out of phase.

- **8080 Direct I/O**
  
  - LXI BC ; Load initial values into B and C (000, 200 octal)
  - CONTINUE INC B ; Increment the B value
  - MOV B, A ; Move the contents of the B register to the accumulator
  - OUT 1 ; Output the accumulator to port 1 (1st sawtooth)
  - INC C ; Increment the C value
  - MOV C, A ; Move the contents of the C register to the accumulator
  - OUT 2 ; Output the accumulator to port 2 (2nd sawtooth)
  - JMP CONTINUE
  - Total bytes: 14
  - Total states: 60 (one pass)

- **Memory Mapped I/O**
  
  - LXI HL ; Load initial values into H and L (000, 200 octal)
  - CONTINUE INC H ; Increment the H value
  - INC L ; Increment the L value
  - SHLD ADDR : Store H and L in two consecutive memory locations wired as output registers.
  - JMP CONTINUE
  - Total bytes: 11
  - Total states: 46 (one pass)

Now let's compare a couple of simple programs written using each method (see examples 1 and 2). It can be easily seen that the extra instructions which operate on memory can greatly improve the output speed of the 8080. This extra speed, though not necessary when driving a 110 bps Teletype, can be a saving grace in a computer music or graphics application. In fact, many video display drivers utilize this technique.

Summary

There are certain advantages to converting 8080 peripherals to mapped versus direct I/O. Among the major points to consider are the following:

- More IO ports are available. The full 64K bytes of addressable memory space can be set up for IO. It is not inconceivable that a video graphics display will use 8 K bytes of memory. This, of course, means that the 8 K bytes are decoded to provide 8192 IO port assignments.

- Once the H and L registers have been loaded and provide a memory pointer, memory output is by 1 byte instructions (such as MOV and STAX).

- By not always having to pass through the accumulator, outputs are faster.

- 16 bit IO capability through the use of the LHLD and SHLD instructions.

Now, should you consider changing your 8080 system to memory I/O? Frankly, if you are the type of person who will never write an assembly language program and is content to stick with high level languages such as extended BASIC, don't even consider it. If the software packages supplied by the computer manufacturers have worked consistently for you to this point, don't tempt fate. The majority of the systems sold, including Altair, IMSAI, DGS and so on, use 8080 I/O instructions to all their peripherals. But many video systems bought as plug-in boards for the Altair (S-100) bus have memory mapped I/O designs.

Delving into memory mapped I/O should be reserved for people willing to use assembly language and prepared to modify standard software if required. In future editions I intend to investigate computer music applications where fast memory mapped 8080 (Z-80) I/O will become a necessity. But, for the meantime, you should at least know what it is.

Author's Note

I hope you've enjoyed the first installment of Ciorcla's Circuit Cellar. I'd like to have your comments and criticisms as well as any ideas you may have for future editions of this feature. I'm always interested in hearing from readers who have such brainstorms. Send all correspondence to Steve Ciorcla, POB 582, Glastonbury CT 06033 and please enclose a stamped, self-addressed envelope.
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Simulation of Motion:

Part 1: An Improved Lunar Lander Algorithm

About the Author

Stephen P Smith's pet project as an amateur is a PASCAL compiler for a personal computer. Professionally, he leads the Computer Sciences Corporation support team attached to the range safety office at NASA Wallops Flight Center, where he and his team of analysts develop analytical methods and construct digital simulations of flight paths, flow fields and structural responses of rockets and aircraft. The BASIC programs which are part of this article and the remaining parts to come in several installments were developed and run on a Tektronix 4051, which uses a 6800 microprocessor and includes a BASIC interpreter.

One of the most delightful applications for personal computers is games, not just playing them, but creating them. If you are like most enthusiasts, you will have begun with random number games like blackjack, but sooner or later you will want to work with games involving moving objects. To describe that motion using a microcomputer you will need to use a form of simulation. The simulation could involve detailed mathematical models solved with elegant numerical techniques.

More likely, the novice will begin by following the pattern of the simple lunar lander games which have appeared often in BYTE (see "Kim Goes to the Moon," by Butterfield in April 1977 BYTE, or "Controlling Small DC Motors with Analog Signals" by Dwyer, Critchfield and Sweer in September 1977 BYTE). The truly advanced simulations are best left to professionals with mainframe computer power, but the home user can progress well beyond the simple lunar lander game. By picking up the basic physics and simple numerical methods presented in this article and the following ones, you will learn to simulate a wide variety of motion. Whether you use these simulations to create games, like the real time LEM simulator presented here, or to develop new applications for your personal computer system, you will acquire some valuable additions to your applications software toolbox.

For any application involving motion, your simulation will be required to predict the speed and position of an object at some time in the future. The predictions can be made using a microcomputer if you first limit the type of motions considered at any point in the program. In the lunar lander game, for example, the excursion module (LEM) is only allowed to move up and down. The simulation is said to have one degree of freedom. Other degrees are possible, but the separation into different degrees of freedom is an important first step.

Let's see how a one degree of freedom simulation is performed. Thanks to Sir Isaac Newton and his apple (that was a fruit, not a computer), we know that an object will continue to move in any degree of freedom without changing speed until a force acts on it. To predict how the LEM will move, we need only to examine the forces which might be present and determine how they effect the up and down motion.

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Gravity is provided for them. On some other heavenly bodies. The above table of accelerations due to gravity is provided for them.

Note that the gravitational accelerations shown in this table are surface accelerations, valid during the final stages of a landing when a spacecraft is relatively near the heavenly body. A more complicated simulation is required if movement far away from the heavenly body is contemplated.

Table 1: This article was written using the metric system of units. As the front runners in an exciting new technical hobby, we should be more ready than most to accept the coming metric conversion in this country, but if you haven't been converted yet, the above table will be useful.

Table 2: Players who grow adept at lunar landings may wish to try landing on some other heavenly bodies. The above table of accelerations due to gravity is provided for them.
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Photo 1: A scene from the “lunar lander” program which is the Digital Equipment Corporation’s graphics equipment demonstration program. This simulation is a real time model of a lunar landing in which a light pen is used to input control information and displays track the landing. The object of the game is to land near (but not on) the only MacDonalds’ hamburger stand on the moon. This simulation, like the one discussed in the article, has two degrees of freedom; superficially it differs from the program of this article largely in its incorporation of real time graphic display light pen control inputs and a model of the lunar terrain.

position. We have shown that if the LEM is moving downward at 100 meters per second now, \((\text{speed}=-100)\) then in 2 seconds the speed will be \(-100+2.0\times(\text{THrust}/\text{MASS} -1.62)\). Similarly, if the LEM is 10000 meters above the moon now, in 2 seconds it will be \(10000.0+2.0\times(\text{speed})\) meters up. Just as we multiply the forces by time and add the product to the speed, we multiply the speed by time, and add the product to the position.

What we have just done is to predict the speed and position at a “step” of 2 seconds into the future. In the jargon of simulation, 2 seconds is the step size. The step size can take any value you choose. Returning to the 1000 kg LEM, let the step size be 0.1 seconds. For a present speed of -100 meters per second, the speed predicted for 0.1 seconds in the future is \(-100.0+0.1\times(10000.0/1000.0-1.62)\) or -99.16 meters per second. If the position now is 10000 meters, then the position predicted for 0.1 seconds in the future is \(10000.0+0.1\times(-99.16)\) or 9990.08 meters above the moon.

Using these values of speed and position we can find new values for the forces and mass. We can then step the simulation into the future once again. The process can continue indefinitely, but usually one or more variables is tested for an end condition at each step. The test might be on position (Are you still above the moon?), on mass (Is there fuel remaining?), or on some other variable. Should any of the tests fail, the program will branch and end the simulation.

Adding a New Degree of Freedom

You now know the basic procedure for simulating motion in one degree of freedom. The LEM simulation has been in one degree because we have only predicted the up and down movements. These are called vertical motions. Suppose that we also predict the way the LEM moves horizontally, in other words, from side to side. The pilot must not only reach the surface of the moon successfully, but also land close to his target. While the pilot’s task has become more complicated, our simulation fortunately has not. Just as we are able to calculate the effects of each force separately, we are able to make calculations for speed and position separately in each degree of freedom.

To make those calculations for the second degree of freedom, first determine what forces are acting. Gravity, by definition, acts only up and down. It does not enter into the horizontal calculations. So far, thrust has also been limited to vertical action, but we can easily add a second thrust acting to the side. Positive horizontal thrust should cause the LEM to move left, while negative thrust moves it right.

Since there are no other forces to consider, the change in horizontal velocity (in meters per second) will be exactly equal to the horizontal thrust (in newtons) divided by the mass (in kilograms). This is, of course, the same equation used in the first or vertical degree of freedom. Similarly, the same equations used to calculate vertical speed and position will be used to calculate horizontal speed and position.

Return to the example used earlier, but also consider the horizontal motion. Let the LEM start 100 meters to the left of its target moving at 10 meters per second to the right. Generally motion to the left will be considered positive and to the right negative, so the horizontal speed is -10 meters per second. We found that during a step of 0.1 seconds the vertical speed changed from -100 to -99.16, and the position changed from 10000 to 9990.08. Quite apart from those calculations, we may set a horizontal thrust, say 5000 newtons, and find that during the same step the horizontal speed will become \(10+0.1\times(5000/1000)\) or -9.5 meters per second. The horizontal position will become \(100.0+0.1\times(-9.5)=99.05\) meters. After making these calculations, the simulation

Continued on page 216
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See it at your local computer store or contact us at 460 Ward Dr., Santa Barbara, CA 93111, (805) 967-0468.
Photo 2: Third graders Esther Mariani (left) and Lisa Hanson from Southport and Roosevelt schools in Kenosha WI deep in thought as they program one of the computers at the Wisconsin Computer Fair.

(120 miles). Many manufacturers who were contacted but could not come helped out by encouraging the stores in our area to attend and display their products.

Other sources of hardware were hobbyists and computer clubs within driving range. Two Chicago area clubs and the Wisconsin Computer Society (an amateur computer club) were invited, and they responded with a number of excellent displays. Two $25 cash prizes were donated by BYTE magazine for the best "homecooking."

The support we received from the computer stores, clubs and a few local manufacturers made the hardware component of our fair very successful.

Manufacturers who could not come usually sent the all-important free brochures that everyone enjoys collecting at a fair whether they ever read them or not. A few generous manufacturers such as Vector, OK Tool and Hexadaisy included samples of their products which we could use as valuable door prizes.

Speakers

Another important component of every fair is the speakers. Throughout the day, a number of "small talks" (one half hour in length) were given by members of the Center for the Application of Computers, faculty members from other schools, hobbyists and students. Topics ranged from an introduction to personal computing, cryptography, microcomputers in the laboratory, and computer graphics, to optical character recognition and speech conversion. The featured speaker for the day was Ted Nelson, the writer, showman and computer guru who came armed with his talk, "The End of the Dinosaurs."

Programming Contest

The final component of our fair (and the one that made it very special) was the First Annual Interactive Computer Problem Solving Contest. The glitter of computer hardware with all its razzlers and dazzlers soon fades without an understanding of how one controls them through programming. Despite the fact that kids will sit for hours at a terminal playing a canned computer game, nothing can compare with the excitement that radiates from their faces when they successfully write their own programs to solve a problem.

The programming contest was divided into four categories: 1st thru 6th grade, 7th thru 10th grade, 11th thru 12th grade, and college. The contestants entered as teams of up to three members each and were assigned one terminal per team. Five problems of varying difficulty were handed out with a 2 hour time limit for solution. The 11th thru 12th category proved to be the most popular, and one 2 hour session with 19 teams was devoted exclusively to this category. After two hours each team turned in their solutions which consisted of a listing of the program and a sample run. The programs were quickly graded using the criterion of accuracy first and cleverness second.

The winners in the 11th thru 12th class were three seniors from Eau Claire WI (Tim Sirianni, Ellery Chan and Jeff Teeters) who traveled 300 miles that day to enter the contest. They did an outstanding job writing successful programs for all five problems within the 2 hour time limit—an exceptional performance surpassing even the college division that took the same exam. Prizes for first, second and third were awarded in all divisions, including trophies, books and complimentary subscriptions to publications.

Finally, the kids in the 1st thru 6th grade category deserve special attention. Earlier in the year, the special education class of K thru 4th graders from Kenosha Unified

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schools, taught by Iris Helman and Sally Greenwood, had visited the computer center and played games on the terminals. This of course only whetted their appetites for more computer time, and arrangements were later made to return for four 1 hour lessons on programming in the BASIC language. Besides the mechanics of coding a computer, the elementary ideas of programming logic were emphasized through flowcharting. These ideas were discussed every day without a computer. The class enjoyed transforming its own scenario into a flowchart format using simple statements and branching conditions. We were pleasantly surprised at how entertaining and creative a flowchart can be when written by young children. The results were posted on a bulletin board at the fair and they proved to be a very popular attraction.

Future Plans

By starting earlier next year we hope to make the 2nd Annual UW-Parkside Computer Fair even more exciting. But quality, not quantity, will remain our long suit. About 700 attended the first fair and 1000 is our upper limit for a comfortable fair. Hardware exhibits will again be sought from local stores and vendors, but they will not play the dominant role that they do at larger fairs; talks and workshops exploring the expanding list of minicomputer applications will be just as important.

The 2nd Annual Interactive Computer Problem Solving Contest will be expanded and announced much earlier so that junior high and high schools throughout Wisconsin and Northern Illinois will have time to get ready. This year's exams will be freely handed out to schools along with instructions on how to run a computer problem solving contest locally. Through these contests we hope to lend encouragement to the growing number of teachers and young students who are eager to learn more about problem solving with the computer. In the process, we will be learning a great deal about this subject ourselves.

Finally, colleges and universities should take the lead in introducing the community they serve to the coming revolution of cheap computer power. They already have the physical resources to do the job with a minimum of cost. The return in public relations alone is worth much more than the investment. The local newspapers and Racine and Milwaukee television stations carried stories about the fair. Our fair represents one way of bringing computer awareness to the general public, and we highly recommend it.
SPACe WAR DEFINITIONS

I have seen repeated mention, both in BYTE and in other sources, of the original computer game of Space War developed at MIT. What I have failed to see is any type of description or explanation pertaining to this classic king of computer games. What exactly does the original Space War entail in the way of display and participation? I am deeply interested in computer games, and I wonder just what was offered by this "oldie-goldie" to have rated such continued interest.

Again, in reference to MIT's Space War, are there currently any manufacturers' software or hardware products which are comparable? With thrillers like MiniTerm's Deluxe Space War and ECD's Animated Spacewar, I wonder if the current state of the art in computer games doesn't exceed that of the original MIT game.

Rick Craig
2609 E Woodlyn Way
Greensboro NC 27407

See the article by Dave Kruglinski on page 85 of the October 1977 BYTE for the answer to your question about what a classic Space War game does, illustrated by a practical example, which will probably not be the last such example seen in BYTE.

SAMPLING BIAS?

After reading your editorial in May 1977 BYTE I still find it hard to believe that only 1% of your readers are female. Did you by any chance look at marital status in the questionnaire? I would guess that in many cases both husband and wife are computer hobbyists. In most cases I would guess that married women interested in computers would share that interest with their husbands.

The reverse however would not be as common. If my husband and I received your questionnaire he would most likely fill it out, thus skewing the results toward the 99% male figure. I'll bet what your survey really shows is the very small number of single women interested in computers and married women who are more interested than their husbands.

Next survey how about asking how many other people - other than the subscriber - read the magazine, and their age, relationship, level of interest, education, etc.

Looking at that 1% figure makes me feel very lonely. I'm sure there must be more women like myself who are interested in computers. I would enjoy hearing from other women hobbyists. Write and let me know who you are and what your interests are. I'll pass the information back to BYTE. It won't be an official survey, but I'll bet I'll get swamped with letters and postcards.

Come on girls, let's show them that we exist!

Leah R O'Connor
6315 W Raven St
Chicago IL 60646

AN INVITATION TO ALL 1802 USERS: THE 1802 EXCHANGE

Very little software for the RCA CDP1802 is currently in the public domain. To remedy this situation I am going to publish a 10 page booklet listing available software. If you desire to sell or even give away your software please send me a listing for my review. My booklet will provide a complete description and cost information with a reference number corresponding to a number on an ordering coupon.

I plan to charge $1 for the booklet. This amount will also cover the costs associated with processing the coupons. The use of the coupon will reduce the costs to the person ordering from more than one source.

The publication date is set for early December 1977. Advance orders may be made at $1 per copy. Send all orders, software listings, and other correspondence to:

Ross Wirth
1636 S 108 East Av
Tulsa OK 74128

SELF-PROPAGATION MONSTERS

I discovered a real "bug" in the Z-80. If the registers are set up correctly, and the user has 64 K of programmable memory, a "living" creature can be created, similar to the interrupt driven monsters that pop up unexpectedly. Its only purpose in "life" is to procreate and eat food, namely time. If you object to my use of the term "life," go back and reread the definition. The "crea-
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*MOTOROLA EVALUATION KIT
ARTICLES NEEDED

As an owner and user of an MEK-6800D2 kit from Motorola, I would like to see some software especially for this system with its J-BUG monitor. A somewhat similar but older system, the KIM-1, has a devoted following and many articles concerning this system have appeared in past BYTES. I believe the D2 system, with a little encouragement, could also become popular. I know you are a 6800 fan, CH, so how about encouraging someone to write about this Motorola kit?

David Beach
POB 360
Frankford Ontario
CANADA K0K 2C0

PS: The MEK6800D2 appears fairly well thought out. Mine went together without any problems (I used sockets for all the chips, however) and ran perfectly on the first power up.

MORE ON COMMERCIAL RADIO AUTOMATION

Joe Alvin's request in the February 1977 BYTE for information on microprocessor based radio automation systems is easily answered. McCurdy Radio of 108 Carnforth Rd, Toronto CANADA, has an 8080 based system that will do just what he wants. Data input is via keyboard or standard audio cartridges or cassettes for compatibility with other radio station equipment. Logging may be on Teletype, or the data may be recirculated in memory and used again for another day's programs. Data is displayed on a CRT.

And now perhaps one of your readers can help me. I am looking for a "Universal Alarm Annunciator." If any one of, say, 100 terminals is grounded, I want to display a one line alarm message on a CRT, eg: ""$5: XMT OFF AIR." The messages must be previously entered from a keyboard and must of course be protected against power failure. An additional "HELP" routine could be used to call up (off disk) a whole page of previously entered text describing what to do to solve the $54 alarm problem. As you will appreciate, the difficulty lies in solving the sorting problem economically. Including the CRT, keyboard and microprocessor, the whole thing should come in at less than $15,000. Has anyone such an item up their sleeve?

M Barlow
5052 Chestnut Av
Pierrefonds
Montreal CANADA

LORAN-C CLARIFIED

In the July 1977 BYTE, there was a letter from Ian McNicol in which he occurred a sort of throw-away line: "... why use OMEGA when there are satellite systems like LORAN-C?" Well, perhaps this is a pertinent question, but it displays a little misinformation. LORAN-C is not a satellite system. LORAN-C is a system consisting of a master station and two to four slave stations which broadcast a series of pulses which modulate a 100 kHz carrier. The master sends a signal which is received by the slave stations and the navigation receiver. The slave stations delay the master signal and rebroadcast it to the navigator. The LORAN-C receiver measures the time difference between arrival of the master and slave

Continued on page 145

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John Montagna, computer engineer (above left), lead this successful network team in generating election results speedily, efficiently and reliably using predominantly TDL hardware and software. Montagna created three programs to get the job done. The text for a SWAPPER program was written and assembled using the TDL TEXT EDITOR and Z80 RELOCATING MACRO ASSEMBLER. The SWAPPER text and all debugging was run through TDL’s ZAPPLE MONITOR. The relocatable object code was punched onto paper tape. A MAIN USERS program updated votes and controlled air display. An ALTERNATE USERS program got hard copy out and votes in. The latter two programs were written in BASIC. Montagna modified the ZAPPLE BASIC to permit time-sharing between the two USERS programs.

Four screens were incorporated, two terminals entered votes as they came in and were used to call back votes to check accuracy. Montagna called on the power and flexibility offered by TDL’s ZPU board and three Z-16 Memory boards.

Montagna’s setup worked constantly for over four hours updating and displaying state-wide and county-wide results without flaw.

“I chose TDL because they have all the software to support their hardware, and it’s good; it has the flexibility to do the job.”

John Montagna

We salute John Montagna and NEW JERSEY PUBLIC BROADCASTING for spearheading the micro-computer revolution.

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Introducing Apple II.
You've just run out of excuses for not owning a personal computer.

Clear the kitchen table. Bring in the color TV. Plug in your new Apple II, and connect any standard cassette recorder/player. Now you're ready for an evening of discovery in the new world of personal computers. Only Apple II makes it that easy. It's a complete, ready to use computer, not a kit. At $1298, it includes video graphics in 15 colors. It includes 8K bytes ROM and 4K bytes RAM—easily expandable to 48K bytes using 16K RAMs (see box). But you don't even need to know a RAM from a ROM to use and enjoy Apple II. For example, it's the first personal computer with a fast version of BASIC permanently stored in ROM. That means you can begin writing your own programs the first evening, even if you've had no previous computer experience.

The familiar typewriter-style keyboard makes it easy to enter your instructions. And your programs can be stored on—and retrieved from—a cassette interface, so you can swap with other Apple II users.

But Apple II is more than an advanced, infinitely flexible game machine. Use it to teach your children arithmetic, or spelling for instance. Apple II makes learning fun. Apple II can also manage household finances, chart the stock market or index recipes, record collections, even control your home environment.

Right now, we're finalizing a peripheral board that will slide into one of the eight available motherboard slots and enable you to compose music electronically. And there will be other peripherals announced soon to allow your Apple II to talk with another Apple II, or to interface to a printer or teletype.

Apple II is designed to grow with you as your skill and experience with computers grows. It is the state of the art in personal computing today, and compatible upgrades and peripherals will keep Apple II in the forefront for years to come.

Write us today for our detailed brochure and order form. Or call us for the name and address of the Apple II dealer nearest you. (408) 996-1010. Apple Computer Inc., 20863 Stevens Creek Boulevard, Bldg. B3-C, Cupertino, California 95014.

SPECIFICATIONS
- Microprocessor: 6502 (1 MHz).
- Video Display: Memory mapped, 5 modes—all Software-selectable:
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Apple II is also available in board-only form for the do-it-yourself hobbyist. Has all of the features of the Apple II system, but does not include case, keyboard, power supply or game paddles. $598.

PONG is a trademark of Atari Inc.

*Apple II plugs into any standard TV using an inexpensive modulator (not supplied).
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Some Comments on "An APL Interpreter for Microcomputers, Part 1"

The following letter from Fred J Dickey contains corrections to "An APL Interpreter for Microcomputers, Part 1" by Mike Wimble, which appeared on page 50 of the August 1977 BYTE. We thank Fred for his efforts.

I received my August 1977 BYTE yesterday, and was quite impressed by Mr Wimble's APL implementation article and the fact that he is giving a hardware independent description of a significant software system. This article is of value regardless of what type of microprocessor one uses. Furthermore, one would expect the article to be of value as long as there is interest in APL, which will probably be long after the current crop of microprocessors become historical curiosities.

Despite my enthusiasm, I regret to inform you that I found the following errors by doing a hand simulation of the program on page 55.

1. Some arrays are dimensioned starting at 0, others at 1. In particular TVAL starts at 0, and all others seem to start at 1. This is not explained anywhere.

2. FUNC, NOMBRE, OTHERS, NILAD, MONAD, DYAD, EOL, CARRET are called subroutines, but they are in fact extensions of the main routine given on page 56.

3. The labels IP, IPGET, IP_GET, and IP_INIT are nowhere defined. Apparently IP = IPGET = IP_GET and the flowchart on page 56 should appear as shown in figure 1.

4. Why is DA initialized to 3? Also, the scanner initialization box on page 56 should appear as in figure 1.

5. "No" and "yes" on page 56 should also appear as in figure 1.

6. The call to IDEN on page 56 should say CALL IDEN (Q, B). Otherwise Q and B are undefined.

7. The flowchart on page 62 should appear as in figure 2.

8. On page 64, it should be made clear that F and Q are local parameters of subroutine FN_VAR_ADD. F and Q have different meanings external to this routine.

9. On page 64, "routine" carret references STMT. STMT must be in ROM. What is its value?

10. The flowcharts do a good job of trapping errors. How do you recover?

11. Let " _ " mean blank. On the example of page 55, you state that you are going to scan 37_25, but apparently 3_7_25 is scanned instead.

12. On page 55, SP(19). C = 6. I don't see how this can be. Also, SP(9). C = 4 not 6, and SP(2). P = 0.

13. Make the following change on page 64:

Fred J Dickey
3420 Granville Rd
Westerville OH 43081

Mike Wimble replies:

Mr Dickey is correct on most points; however, I would like to clarify the following:

Point 3: IPINIT is of course the beginning of the statement interpreter as defined in part 2 of the article published in September.

Point 4: I inadvertently included DA in this portion of the article. It is used in a later version of the interpreter to handle threaded lists.

Point 9: STMT, again, is part of the later version of my interpreter, and should be ignored.

Point 10: This version of the interpreter has no provisions for error recovery.

Point 12: SP(19).C was incorrectly set equal to 6; it should equal 8. SP(2).P is correct as it stands. Although I did not state it explicitly, the case for SP(1).C=1 is used in the later version of my interpreter. It indicates that P is not to be used at that time (This

Continued on page 164
BOMB Lands on APL

Readers of the August 1977 BYTE voted for APL all the way. The BOMB first prize of $100 goes to Mike Wimble for his article, An APL Interpreter for Microcomputers, Part 1, on page 50. The $50 second prize goes to Dr Kenneth Iverson for Understanding APL, page 36. The distribution of points for August's articles was relatively even in the voting (The standard deviation was only 10% of the mean of all article votes.), indicating a diversity of interests on the part of BYTE readers. Mike Wimble's article was 1.7 standard deviations above the mean, and Dr Iverson's article was 1.3 standard deviations above the mean. Readers are encouraged to express their opinions about this month's articles by filling out and sending in the BOMB card between page 256 and the inside back cover.

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If you're just getting into personal computing and are buying your first machine, you're probably confused by the myriad of companies and products available.

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Ohio Scientific has always maintained upward expandability from old models to new models, which is nice to know considering the rate at which technology is constantly improving. For example, Ohio Scientific’s original 400 series products can be plugged right into the new Challenger II P. And Ohio Scientific has 2 years of experience in building personal computers, so we’re not new to this business unlike some of our competitors.

Complete with a full computer keyboard Challenger II P comes fully assembled for $598 from Ohio Scientific.

Check the chart below and compare Challenger II P with other BASIC in ROM computers. Unlike other personal computers, Challenger II P has a much greater capacity for expansion and the capability to perform big computer functions with all of its big computer features.

<table>
<thead>
<tr>
<th>Processor</th>
<th>Ohio Scientific</th>
<th>Other BASIC in ROM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Challenger II P</td>
<td>6502A</td>
<td>6502 or Z-80</td>
</tr>
<tr>
<td>Clock</td>
<td>1 or 2 MHz</td>
<td>slower</td>
</tr>
<tr>
<td>Display (Lines/Characters)</td>
<td>32/64</td>
<td>25/40 or 16/64</td>
</tr>
<tr>
<td>Keyboard</td>
<td>Full Computer</td>
<td>4 Function</td>
</tr>
<tr>
<td></td>
<td>(Capacitive Contact)</td>
<td>Calculator Type or Full Computer</td>
</tr>
<tr>
<td>Display Characters</td>
<td>256</td>
<td>(Mechanical Contact)</td>
</tr>
<tr>
<td>Lower Case</td>
<td>Yes</td>
<td>128 or 64</td>
</tr>
<tr>
<td>Plotting</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Audio Cassette Interface</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>BASIC</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>String Functions PEEK, POKE, User</td>
<td>Yes</td>
<td>some have only 4K BASIC</td>
</tr>
<tr>
<td>Machine Language Accessible</td>
<td>Yes</td>
<td>Not Always</td>
</tr>
<tr>
<td>Optional Assembler/Editor</td>
<td>Yes</td>
<td>Not Always</td>
</tr>
<tr>
<td>Disk Option Available Now</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>In Case Memory Expansion Ability</td>
<td>36K</td>
<td>Less</td>
</tr>
<tr>
<td>Expansion Boards Available Now</td>
<td>15</td>
<td>None</td>
</tr>
</tbody>
</table>

BYTE November 1977 41
Any serious application of a computer demands a Floppy disk or hard disk because a disk allows the computer to access programs and data almost instantly instead of the seconds or minutes required with cassette systems. In real-world application of computers, such as small business accounting, a cassette based computer simply takes too long to do the job.

Ohio Scientific offers a full line of disk based computers utilizing full size floppy disks with 250,000 bytes of formatted user work space per disk. That's 3 to 4 times the work space of mini-floppies.

**Challenger II**

Challenger II is available with a single or dual floppy disk and a minimum of 16K of RAM instead of ROM BASIC. The disk BASIC is automatically loaded into the computer so there is no need for ROMs.

Ohio Scientific's powerful disk operating systems allow the computer to function like a big system with features like random access, sequential, and index sequential files in BASIC and I/O distributors which support multiple terminals and industry-standard line printers.

Challenger II's with disks can have the following optional features:
- 16 to 192K of RAM memory
- Single or dual drive floppys
- Serial and/or video I/O ports
- Up to 4 independent users simultaneously
- Two standard line printer options
- Optional 74 Megabyte Hard disk
- Much more

Challenger II disk systems are very economical. For example a 16K Challenger II computer with serial interface, single drive floppy disk, BASIC and DOS costs only $1964.00 fully assembled.
Ohio Scientific proudly announces the ultimate in small computer systems, the Challenger III. This computer has a 3 processor cpu board equipped with a 6502A, 6800, and Z-80.

This system allows you to run virtually all software published in the small computer magazines!

The Challenger III is fully software and hardware compatible with Ohio Scientific products and can run virtually all software for the 6800, 8080 and Z-80 including Mikbug® dependent 6800 programs!

Incredible as this is, Challenger III costs only about 10% more than conventional single processor microcomputers. For example a 32K Challenger III with a serial interface and a dual drive floppy disk (500,000 bytes of storage) costs only $3481.00. Fully Assembled, complete with software. Terminal not included.

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This is our unbelievable triple processor board! Complete with the 6502A, 6800, and Z-80 processors, this board allows you to run virtually all programs published for small computers. Available in the Challenger III, the 510 board is ideal for industrial development and research applications. There isn't another triple processor board like the 510 anywhere, except at Ohio Scientific!

560Z CPU Expander Board
The 560Z board is our multiprocessing board with a Z-80 and 6100 chip. This board allows you to run several processors simultaneously and the 6100 chip lets you run powerful PDP8 software with the 560Z. The 560Z board is the only multiprocessing board available for small computers, and Ohio Scientific makes it!

These three state-of-the-art CPUs are only a small part of the picture. Ohio Scientific's advanced technology offers you other unique features such as Multiport Memories, Distributed Processing, Big Disks with up to 300 megabytes on line, and Advanced Software.
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The 74 megabyte disk from Ohio Scientific

C-D74 from Ohio Scientific is the ultimate storage device for small computers. The C-D74 is the first Winchester technology disk for small computers making big system technology affordable and reliable for the small system not under maintenance contract.

The disk uses a non-removable sealed chamber drive with a unique rotary positioner to provide the highest performance disk available today.

The Ohion scientific C-D74 can store all the records of a medium size company for instant access. And the Winchester technology of the C-D74 means that the drive can run 24 hours a day without worry of disk wear.

There are other important C-D74 applications in business computing and research in computing itself. The disk makes small computers practical for much larger jobs than formerly thought feasible, particularly since most business computing is disk bound and not computer bound.

C-D74 provides an unbelievable 35 millisecond average access time to any of 74 million bytes of information. With a 10 millisecond single track seek, the drive has an incredible data transfer rate of 7.3 megabits per second.

Recommended minimum hardware for the C-D74 is a Challenger with 32K RAM and at least 8K on a Dual Port 525 board, and a single or dual-drive floppy disk.

The drive, cable, interface for an Ohio Scientific Challenger and OS-74 operating system software is $6,000 FOB Hiram, OH. Equipment rack shown not included.

The state of the art in small computers.
To order direct call 1-216-569-3241
Announced in August, the new Radio Shack TRS-80 is a major entry into the personal computer market. The $599 single board Z-80 based unit comes complete with a full ASCII character set keyboard, cassette recorder and video display monitor. Also included for the price is 4 K bytes of programmable memory and 4 K bytes of read only memory; the latter features a built-in BASIC package. An additional 12 K bytes of programmable memory can be added for $289.

The computer is being marketed in selected Radio Shack stores across the country; peripherals planned for release in December include a disk drive, printer and memory expansion hardware. An interesting feature of the TRS-80 is the convenient hinged door on back for easy access to the 40 pin printed circuit card IO connector.

Software will be available in a variety of packages, including a blackjack program (which comes free with the computer); a payroll program for up to 15 people, priced at $19.95; a kitchen menu program for $4.95; and so on.

The unit is priced competitively with some other computers on the market, and it will be interesting to see what develops in this low priced appliance computer market.
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B. PCS-80 with CRT, dual floppy disk & Intelligent Keyboard options
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D. Processor, Memory & Interface boards—standard MINS & 16K RAM, and floppy disk, line printer and serial I/O.
E. PCS-80 System—sample component configurations.
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Features and specifications subject to change without notice.
Using Interrupts for Real Time Clocks

We have developed several software time-keeping routines for oceanographic data systems which may be of more general interest. These routines are based upon the Motorola M6800 and have been tested on SwTPC 6800, MITS 680b and Motorola MEK-6800D1 evaluation kit systems. The routines require little memory or hardware and do not slow program execution appreciably. Features of the routines are:

- packed BCD storage of time values: days, hours, minutes and seconds.
- little interference with user routines through use of interrupts.
- usable with a wide range of clock frequencies.
- minimal hardware complexity.
- possibility of event scheduling.

Hardware

The routines are driven by direct non-maskable interrupts of the processor by a clock pulse source as shown by figure 1. Use of the NMI in this fashion precludes use for other functions but minimizes hardware. Also, such use of interrupts can cause problems when timing loop software is interrupted: constants which are valid without interrupts can be incorrect when interrupts are in operation. With these caveats in mind, however, use of interrupts proves quite convenient.

The clock source may be in the range 1 to 99 Hz (10 Hz is used here) and drives a monostable (74121, 9601, etc). The Motorola literature describing the 6800's non-maskable interrupt function is just a trifle confusing. Using the information in the M6800 Microprocessor Applications Manual, one could conclude that the NMI line requires a low level input to initiate an interrupt. This conclusion results from the terse description of NMI and reference to the fact that NMI is supposed to work similar to IRQ. However, the hardware specification sheets for the processor explicitly state that NMI is sensitive to the negative going edge of the digital signal on its input. This detail is easily confirmed by experiment. [It is also the only sensible way to handle this interrupt, in view of the fact that it cannot be masked in the processor to inhibit further interrupt while the interrupt routine is in operation. . . CH] The oneshot in figure 1 should be interpreted as a way of transforming an arbitrary signal into a well-defined TTL pulse of a minimum 2 microseconds in length, or slightly greater, which provides the required negative edge.

Unless the time routine is stored in ROM with “hard” NMI vectors, means of disabling NMI pulses must also be provided until the interrupt routine and vector are estab-
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Pricing, specifications, availability subject to change without notice.

Circle 124 on inquiry card.
Entered following NMI interrupt pulse.

Update clock variables (i.e., count interrupts modulo E4:60:60:N where N = number of interrupts per second).

Location of "return from interrupt" in simple clock routines of listings 1, 2 and 3.

Note: \( T_0 \) = time of next background task event.

"Old process state" is content of top seven levels of stack.

Manipulations of process state can be accomplished by maintaining two stacks and switching stack pointers.

\[ T_0 \cdot T_0 + \Delta T_B \]

\[ T_0 \cdot T_0 + \Delta T_F \]

Figure 2: A suggested algorithm for implementing two simultaneous tasks using the interrupt input to keep track of times \( \Delta T_B \) and \( \Delta T_F \) allocated to each process. It is assumed here that the "foreground" task is the principle task, and that the presence or absence of a hidden "background" task is governed by a flag.
lished in programmable memory. We use a mechanical switch (S1), but more elegant methods are possible with increased hardware complexity.

Software

A minimal timekeeping routine called RAMTIME is shown as listing 1. This routine performs the function of a real time clock when it responds to the interrupts from NMI. It has two counters. A counter 1 byte long called WATCH continually cycles with a binary integer count. A second 5 byte count field provides the usual day, hour, minutes and seconds counts using the "overflow" constants 99, 99, 24, 60, 60 and the number of interrupts per second to determine when a carry has occurred. All the counting in this field is done in BCD. If at any time it is desired to output the BCD numbers in the various count fields, the MIKBUG subroutines OUT2HS and OUT4HS can be used to convert to external ASCII decimal values on a terminal.

The program includes a binary "stopwatch" function. The location WATCH is incremented with every NMI pulse, thus providing a convenient means of timing short events. This function can be eliminated with a small saving of memory, if desired.

Clock rates different from the 10 Hz rate are accommodated by changing the RATE variable (RAMTIME) to the packed BCD value of the clock rate, eg: the present rate of hexadecimal 10 (BCD for 10 Hz) is changed to hexadecimal 60 for a 60 Hz clock source.

Scheduling

The nature of the NMI-driven clocks make them ideal for the inclusion of task scheduling routines. Scheduling, using these routines as vehicles, is transparent to the user program, i.e: scheduling is performed without "knowledge" of the program that scheduling is going on. Timetables are accurate because the schedule is checked every NMI. A very simple scheduler is suggested in the flowchart of figure 2. This algorithm implements a timing diagram (like that in the figure) which switches between two tasks arbitrarily called "foreground" and "background." This is the simplest form of "timesharing" or "multi-programming."

Operation

Startup of the routines is not automatic if routines and vectors are held in programmable memory. The source of NMI pulses must be disabled until the routine and vector are loaded. Once they have been installed, enable the NMI source and the routine begins working. Time can be set using memory alter functions or with special setting routines. Once the timekeeper is running, normal operation may proceed as usual, subject again to the caveat of checking the effects of interrupts on any timing loops in other programs.

Listing 1: RAMTIME. This routine is a minimum "clock" and "stopwatch" function to be used at interrupt service of an NMI (nominally 10 Hz rate). The "stopwatch" maintained at hexadecimal location A051 is incremented as a binary number every interrupt for short term timing by counts. After incrementing stopwatch, the routine treats the bytes at locations A04A to A052 as a 2 digit BCD field with subfields for days (2 bytes), hours (1 byte), minutes (1 byte) and seconds (1 byte) and parts of a second (1 byte). The overflow values for each field are coded as BCD numbers stored at locations A052 to A057.

The overflow values for each field are coded as BCD numbers stored at locations A052 to A057.
Figure 1: Typical shape of a voltage transient waveform. The voltage transient is superimposed on the normal voltage in a circuit, and is characterized by an exponentially damped envelope around an oscillatory waveform.

Spikes: Pesky Voltage Transients and How to Minimize Their Effects

You're sitting at your computer playing a game of Super Universe War, about to defeat King Computer, when suddenly, instead of his spaceship disappearing from the display, you see smoke rings drifting from the top of your mainframe. While you curse the expert technician that built the system (you), you dissect the power supply and find a shorted rectifier diode or a bad regulator integrated circuit. Although the uninformed would blame the component manufacturer, you know that it was Spike that did you in; possibly the voltage spike your brother made when he started the washing machine. The roughest environment you can put that fragile MOS circuit in is probably the one you find most comfortable, your house. The way voltage transients run around the power wiring in your home, you'd think they made the mortgage payment. Let's look at just what these beasts are, where they come from, what they do, and how to protect your microcomputer from them.

The beast I'm talking about is the voltage impulse that enters your computer through the wall plug and tries to eat power supply components and fragile chips. These spikes originate everywhere. You can't turn on the television or turn off the coffee pot without making one. Many are small enough to pass by unnoticed, but often they dump their energy where you least want it. Voltage spikes of 1700 V have been recorded on the 120 V wiring in common houses. Multiple spikes of over 1200 V can be expected in 2 to 4% of all houses. These are usually due to changes in an electrical circuit, i.e., opening or closing a switch. Remember, the wiring in your house obeys the same laws of nature that govern other circuits with resistance, inductance and capacitance. If you try to rapidly change the current through an inductor, for example, opening or closing a switch, the voltage across it rises rapidly. Guess what? Most power wiring just happens to be predominately inductive. Researchers have shown that residential areas often exhibit more transients, and more severe transients, than commercial and even some industrial areas. What does the spike look like on an oscilloscope? It is usually a damped sine wave such as the one in figure 1. It has extremely sharp rise characteristics (steep leading edge) and it normally dies out after 5 or 10 cycles. It may be only 5 µs long, but may last for 50 µs or longer. A typical wave shape is shown in figure 1. Another source of surges that I will quickly mention is lightning. Although we can't prevent it, we can divert it. I have a lightning arrester at the power entrance to my house. If you don't, I strongly suggest that you look into getting one. It's a good insurance policy for about $10. I've never seen an electric utility that didn't install lightning arresters like they were going out of style, and those people know what they are doing.

Now, let's look at what a well-placed spike can do. It might find a low impedance...
The Dumb Terminal lets you put it all together.

With the new, lower-priced Dumb Terminal™ Kit, that is. Pick one up and escape, once and for all, the headaches of scavenged teletypes and jury-rigged TV sets. With just a little time and aptitude, you can have a live and working Dumb Terminal right in your own home, garage, or business. One that lets you get it all out of your system—or into it.

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All you need, besides the Kit, is some initiative, and a few basic tools—a good soldering iron, wire cutters, needle-nose pliers, and one or two trusty screwdrivers. The Dumb Terminal Kit provides you with everything else. Including an attractive cabinet, CRT screen, keyboard, PC board, and all essential electronic components. Naturally, you also get illustrated, step-by-step assembly instructions, not to mention an easy-to-understand operator's manual.

So, if you'd like more input on the Dumb Terminal Kit, just fill out the coupon and we'll send you complete, free information.

Oh, and by the way, just by sending in the coupon, you will be made a charter member of the Dumb Terminal Fan Club. A select organization that will send you your own nifty Dumb Terminal Fan Club Kit, containing: an official certificate of membership, an autographed photo of the Dumb Terminal himself, and a bona fide membership card to prove irrefutably you're "One of Us." (Sorry, limit one kit per person.)

And, if you include a trifling $6.00, you can have your very own Dumb Terminal T-shirt. (No limit at all on these.)

Simply mail the coupon and get the whole assortment. And find out why members of the Dumb Terminal Fan Club are some of the smartest people around.

Figure 2: The combined isolation and shunting method is the best way to protect your system from voltage transients. The varistor shunts large transients in the AC source of power. Small high frequency “despiking” capacitors provide a low impedance path for any components of the external spike which make it through the transformer and rectifier. (The inductance of the regular filter capacitor tends to limit its usefulness at high frequencies.)

path to ground and pass by unnoticed. But more than likely it will enter some dandy appliance, or your computer, and do all the damage it can. Remember that I that mysteriously appeared in memory shortly after you wrote a 0? Have you ever wondered how that bad data got into your system? It could have been put there by your next door neighbor turning on a vacuum cleaner. You have seen rectifier diodes fail when they were carrying only a tenth of their rated current, voltage regulator integrated circuits die when they weren’t even running warm, and transistors stop working when the hermetic seal broke, letting out the smoke. (I’ve always wondered how they work with all that smoke in there.) If you have mysterious errors in your system, transient and random, chances are a spike might have been involved.

Now let’s get to the good part: how to get rid of the little monsters. There are two basic techniques available. First, you can attempt to isolate the equipment from the source of the spikes by running it on batteries or an uninterruptible power supply. Isolation transformers show up at the surplus dealers occasionally, but are usually expensive. The second method is usually cheaper, but is somewhat less effective. Use the voltage divider principle and shunt the spike to ground through a low impedance at the power supply. A common example of this principle is the 0.01 µF capacitor placed between the power buses and ground of a digital circuit, to suppress the low level switching transients of digital integrated circuits. Since we are talking about transients that come in over AC lines, we need to put the low impedance on either the AC line or the power supply bus. On the DC side, hefty filter capacitors do this for the spikes with low frequency characteristics, but they often exhibit stray inductance which looks like a high impedance to a fast pulse. Putting a 0.01 µF capacitor in parallel with the filter capacitor will take care of many of these. Nonlinear devices such as spark gaps and varistors may be placed on the AC line. The last part of the shunt method is the most important. Put a good ground on the machine! If your house doesn’t have three wire outlets, tie the case ground to a water pipe; if you have to, drive a ground rod. Be aware of the grounding system in all your electronic equipment. Poor grounding practice can cause shocks, ground loops, and erratic operation. (When I took my system away from its usual solid grounding arrangements for a demonstration at the ACGN meeting May 20 of this year, the lack of a good ground became painfully obvious: programs which have never before committed suicide became quite distressed and recalcitrant . . . CH/

We can expect to adequately protect the hardware without much trouble (or cash). The best procedure is to use a combination of the above methods as shown in figure 2.

I’ve tried to explain a little about voltage transients without getting into the physics of semiconductor failure or transient generation analysis. If you want to become better versed in this field, read several of the references. They all offer good background material and references 2 and 3 give detailed information. Hopefully, you are among the many who haven’t had any problem with spikes. The best time to prepare for them is before they give you trouble.

REFERENCES

the Processor Terminal. A logical forward step in Microcomputer design

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Circle 141 on inquiry card.
Here is a program I wrote using Tom Pittman's Tiny BASIC. It originally appeared in KIM-1 User's Notes. This program allows my two children to play with the computer and also learn math. The output of the program looks like this:

```
THIS IS A MATH TEST
12
X 6
?
```

If the correct answer is input, the computer replies with YOU'RE RIGHT and a new problem is set up. For a wrong answer the reply is ??WRONG??, TRY AGAIN and the same problem is repeated. If you answer incorrectly three times THE RIGHT ANSWER IS 72 appears and a new example is set up.

The actual problems are randomly chosen. The number limits for multiplication are set at line 200 for the multiplicand and 205 for the multiplier. Lines 305 and 355 define the two addends for addition.

```
10 PR "THIS IS A MATH TEST"
15 PR
20 LET V=0
30 LET I=0
35 LET Z=0
40 PR "TYPE 1 FOR MULTIPLICATION"
50 PR
60 PR "TYPE 2 FOR ADDITION"
70 PR
80 INPUT I
90 PR
100 IF I=1 GOTO 200
110 IF I=2 GOTO 350
120 IF D=Q GOTO 500
130 GOTO 600
190 END
200 LET X=(RND (12)+1)
205 LET Y=(RND (12)+1)
210 IF X <=10 GOTO 230
220 GOTO 240
230 PR " " ,X
235 GOTO 260
240 PR " " ,X
260 IF Y<=10 GOTO 280
270 GOTO 290
280 PR " X " ,Y
285 GOTO 300
290 PR "X " ,Y
300 PR " ---- "
310 LET Q=X*Y
320 INPUT D
330 GOTO 120
350 LET X=(RND (50)+1)
355 LET Y=(RND (50)+1)
360 IF X<=10 GOTO 380
370 GOTO 390
380 PR " " ,X
385 GOTO 410
390 PR " " ,X
410 IF Y<=10 GO TO 430
420 GOTO 440
430 PR " + " ,Y
435 GOTO 450
440 PR " + " ,Y
450 PR " ---- "
460 LET Q=X+Y
470 INPUT D
480 GOTO 120
500 PR "YOU'RE RIGHT"
505 PR
508 LET Z=Z+1
509 IF Z<3 GOTO 512
510 GOTO 10
512 IF I=1 GOTO 200
514 IF I=2 GOTO 350
600 PR " WRONG , TRY AGAIN"
610 PR
620 LET V=V+1
630 IF V=5 GOTO 650
640 IF I=1 GOTO 210
645 IF I=2 GOTO 360
650 PR "THE RIGHT ANSWER IS ",
655 PR Q
660 PR
670 GOTO 10
```
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My Experiences with the 2650

A Report from Our 14 Year Old Correspondent

When I saw an ad in Electronics magazine for the Signetics 2650, I had a "sixth sense" that this was the processor I wanted. After contacting Signetics Corporation I received the 2650 manual. I had only started to learn about computers two months before, so I did not understand everything in the manual. I had no one to ask; my mom and dad are not familiar with computer technology. I began to write to Signetics, asking about various things, and they wrote back expressing much enthusiasm about my being interested in computers at such a young age. (I was 13 years old).

Signetics made available to me a 3 day seminar about the 2650 and about microcomputers in general. Needless to say, I was ecstatic. Even my parents were excited! When I arrived at the sales office where the seminar was to be held, I found I was the only person under 20 years of age. There was one person from a well-known megacomputer company, three men from a well-known amusement device company, two instructors, and myself. These adults were surprised that a "kid" would be learning about computers, and they asked me many questions.

The first day of the seminar went well, considering that my specialty is hardware, and I actually began to understand software. I had many chances to discuss certain aspects of personal computers with the man from the megacomputer company, and over lunch we discussed many problems of systems going berserk, dropping bits, breaking down, etc.

The second day we studied the problem of programming I/O ports, and tested our programs on a timeshare computer service provided by the seminar. My program (the first I had written) had one bug in it. The problem was to read in data from a certain port into a specified register and output it to
a certain port containing an LED for each data line. The program was to do this continually, but when I loaded the data in from the port I forgot to clear it first.

I wanted to keep the program to an absolute minimum because the Teletype I was using kept losing contact with the timeshare computer. After fighting a battle of trying to write and save programs before the modem "crashed," the final score was: modem 4, me 1. I finally finished it. At this point the instructor said I could use another Teletype. No way!

Now came my turn to load my program into the demonstration computer. The 2650 must have liked me because it worked right after I loaded the program and pressed reset.

The third and last day at the seminar we learned about hardware usage and interfaces. I was sad to be leaving when it came time to bid everyone goodbye. I had become good friends with all the people and they had all helped me in one way or another.

The seminar was in March, and until late May I programmed on paper since I had no computer, nor access to one. I decided to purchase an AMT-2650 from Applied Microtechnology so I could learn more about it before I designed and built my own processor board. It was two months and five days from the date of my order that my computer was delivered. It arrived the day before school reopened. This was a great disappointment because I was planning to work on it during summer vacation.

After programming the diagnostics to check out the computer, I discovered that bit 0 in output port C remained lit when the computer was in the run state, and when a true bit was in position 0 in output port C, the bit in the data load byte would come on, making things more confusing.

Despite all the bugs, I developed many short programs on this computer including one that rotates left one bit in output port C until it gets to bit 7, while another bit in output port D rotates right at the same speed; then both would repeat. One row of LEDs is on top of another, so that, when this program is run, the lights seem to chase each other in circles. There is one catch: the lights go very fast at first and get slower and slower until they come to a full stop and the machine halts. Upon reset, the whole process is started again.

I'm still listing features I want for my processor board and front panel. If anyone is interested in the 2650 please contact me, since no one I know uses this processor, and I would like to possibly start a users' group.
Does Anybody Know What Time It Is?

One of the earliest products of LSI technology that filtered down to the hobbyist was the "clock chip." This little "beauty" divided the 60 Hz line signal down to seconds, minutes and hours...and displayed the results on 7 segment LED or other displays. Today these "clocks" come in a great variety of types, sizes and functions. They come tiny for watches. Some have extra timers and alarm capabilities. They are inexpensive, and require little in the way of external circuitry. For long term timing applications, they form an ideal solution for computer experimenters.

For many personal computer applications, it would be useful for the computer to have a knowledge of the time. The computer can certainly count interrupts from a crystal time standard, but why not use external hardware optimized for the timekeeping function, i.e.: a "clock chip?" This article describes an approach to such a linking of computer and clock. The clock I used had a National Semiconductor MM5314, but other clock chips using multiplexed 7 segment displays will also work.

The circuit attaches to the display lines, does not disable the clock functions or the display, and is easily added inside the clock's case. It simply lets the computer read the clock digits (with the appropriate software) at the same time that the ordinary electronic display is produced.

The hardware interface is shown in figure 1. It consists of three integrated circuits at a total cost of less than $5. Two CD4010 buffers are used to convert the MOS voltage levels of the clock to TTL levels. These buffers are CMOS, so they form almost no load on the clock circuits. The pins labelled $V_{DD}$ are tied to the clock supply. The pins labelled $V_{CC}$ are tied to the computer TTL power supply of 5 V. The common ground line for clock and interface and computer is $V_{SS}$. The only criteria assumed here are that $V_{SS}$ GND $< V_{CC} + 5$ V $< V_{DD}$.

The clock uses a multiplexed 7 segment display format. This means that each digit is formed from seven data bits, and the digits are sequenced one at a time. The lower buffer works on the segment signals. Although seven bits are used for the display, only five are needed to uniquely decode digits. This circuit sends the a, b, c, d and e signals to the computer. These five bits are used in a software table lookup to convert to the digit code. The buffer IC2 handles the digit signals. The six digits are scanned right to left, from seconds digit to tens of hours digit. These six signals are converted to a 3 bit binary number by a 74147 priority encoder. Since both the clock and the 74147 utilize inverted logic, the connections have been manipulated to provide a normal logic output. (Seconds digit is 1, tens of seconds is 2, etc). Thus each digit is converted to eight data bits: three which describe its place in the display and five when uniquely map to its value.

The subroutine of listing 1 illustrates how to read the clock interface. It is written for a Motorola 6800, but should be readily convertible to other processors. The location CLKIO is the interface input (which is assumed to be previously initialized if it is a PIA data location). The subroutine reads the digits from right to left and stores the ASCII code for each digit in a 6 byte storage area. This area is pointed to by the X register contents when the subroutine is called.

The code between WAITD and CLK2 continuously samples the interface waiting for the low order 3 bit digit code pointed to by the B register. When data for that digit is presented, its segment data is separated from the input value and those five bits (shifted right three positions) are used in a table lookup in SEGTAB. This returns the ASCII digit. If no digit corresponds to the bit pattern (hardware error), the letter E is returned. This ASCII character is stored in the storage area. The routine loops through all 6 digit locations and then returns.

Figure 1: Schematic of the clock interface, and a partial schematic of the clock chip and display circuitry. The interface circuitry is intended to convert the signals from an existing electronic clock using MOS integrated circuits and LED displays (left) into TTL compatible levels usable by the microprocessor port at right. Some analysis of the particular clock used is required to attach the interface wires to the appropriate digit and segment output lines. Since the CMOS DC4010 level shifting buffers employed have high impedance inputs, the loading of the clock chip's output lines will not affect operation of the clock itself when the computer is attached.
LED DISPLAY

CUSTOM WIRED OR PART OF EXISTING CLOCK UNIT

INTERFACE TO COMPUTER

+5V

POWER WIRING TABLE

<table>
<thead>
<tr>
<th>NUMBER</th>
<th>TYPE</th>
<th>(VCC)</th>
<th>(VSS)</th>
<th>(VDD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>74147</td>
<td>16</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>IC2</td>
<td>CD4010</td>
<td>1</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>IC3</td>
<td>CD4010</td>
<td>1</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>IC4</td>
<td>CLOCK*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
</tbody>
</table>

NOTES:
VDD IS TAKEN FROM EXISTING CLOCK SUPPLY, AND MUST BE GREATER THAN VCC+5V

*PINOUTS DEPEND ON PARTICULAR CLOCK CHIP
LISTING 1: A program written for the 6800 which will translate the outputs of the clock chip at the input port CLK10 into a 6 byte string of ASCII digits. Due to the typical scanning times of clock displays, the execution of this routine will complete in 6 to 11 milliseconds, so use in time-dependent portions of a program may require careful thinking.

The table lookup is done with the trick of instruction modification at INDEX. If this offends your sense of “proper programming practice,” then try the code used in the MORSER article (BYTE, October 1976, page 34).

The clock steps through digits at a roughly 1 kHz rate. Since the clock and the computer are not synchronized, it might take up to 11 digit times for the program to run to completion. The subroutine thus executes in between 6 and 11 ms. It requires about 80 bytes of memory.

Now there is no excuse for your computer not to know the time unless its clock stops.

---

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70 BYTE November 1977
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Circle 127 on inquiry card.
Figure 1: A simple circuit which processes a 6.3 VAC reference signal derived from the power companies' 60 Hz grid to produce a digital logic level square wave at 15 Hz which can drive an interrupt line of a typical processor. The disable switch is optional and can be left out if the interrupt handlers are permanently loaded in ROM; otherwise, interrupts must be manually disabled while the system's software is bootstrapped into volatile memory.

Adding an Interrupt Driven Real Time Clock

Whenever a computer is interacting with the real world, either through sensors or actuators, a real time clock can be valuable. Using a real time clock, the computer can run programs at specified times or intervals, or the computer may record the times at which events are sensed.

There are two basic types of real time clocks used in computing systems: the external (hardware) clock and the internal (software) clock. An external clock uses hardware to keep track of time, and periodically or on command transmits the time to the computer. An internal software clock has hardware which interrupts the computer at regular intervals, and software which keeps track of time by incrementing a register whenever the computer receives a timing interrupt.

The hardware clock imposes a small software burden on the computer, and being separate from the computer, it need not be reset whenever the computer is shut off. The software clock imposes a larger software burden on the computer, and the clock must be initialized if the computer has been completely halted or had its power shut off. In applications where the computer operates continuously, the advantages of the software clock due to hardware simplicity outweigh its disadvantages due to increased software burden, and the software clock is the logical choice for a real time clock.

There are two key considerations involved in selecting the interrupt rate for the software clock. First, where the interrupt clock is derived by dividing a higher frequency clock, such as a 1 MHz computer clock, hardware simplicity favors as high an interrupt rate as possible, but the computational overhead of interrupt response increases with increasing interrupt rate. Second, a low interrupt rate produces a low computational burden but decreases time-keeping resolution and programming flexibility. Since my system requires no routines to be performed more often than 15 times per second, I decided that a 15 Hz interrupt derived by dividing the 60 Hz power line frequency by 4 would be an adequate interrupt rate. This gives a minimum event to event resolution of 67 ms.
Listing 1: Interrupt handler. This routine contains the overhead needed to field an NMI interrupt on a 6502 processor, save the state of the processor, call an interrupt processing subroutine, restore the state of the processor, and return from the interrupt event. If the jump at location 206 is replaced by NOP operations, this program will spin its wheels 15 times a second, doing nothing in response to the 15 Hz signal produced by the circuit of figure 1. With the exception of the JSR at location 206, this routine is independent of the location in memory of the software discussed in this article.

<table>
<thead>
<tr>
<th>Hexadecimal Address</th>
<th>Hexadecimal Code</th>
<th>Op</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>0200</td>
<td>48</td>
<td>PHA</td>
<td>Push accumulator onto stack</td>
</tr>
<tr>
<td>0201</td>
<td>8A</td>
<td>TXA</td>
<td>Transfer X register to accumulator</td>
</tr>
<tr>
<td>0202</td>
<td>48</td>
<td>PHA</td>
<td>Push X register onto stack</td>
</tr>
<tr>
<td>0203</td>
<td>98</td>
<td>TYA</td>
<td>Transfer Y register to accumulator</td>
</tr>
<tr>
<td>0204</td>
<td>48</td>
<td>PHA</td>
<td>Push Y register onto stack</td>
</tr>
<tr>
<td>0206</td>
<td>20 00 00</td>
<td>JSR</td>
<td>Call CLOCK</td>
</tr>
<tr>
<td>0209</td>
<td>66</td>
<td>PLA</td>
<td>Pull Y register from stack</td>
</tr>
<tr>
<td>020A</td>
<td>A8</td>
<td>TAY</td>
<td>Transfer accumulator to Y register</td>
</tr>
<tr>
<td>020B</td>
<td>68</td>
<td>PLA</td>
<td>Pull X register from stack</td>
</tr>
<tr>
<td>020C</td>
<td>AA</td>
<td>TAX</td>
<td>Transfer accumulator to X register</td>
</tr>
<tr>
<td>020D</td>
<td>68</td>
<td>PLA</td>
<td>Pull accumulator from stack</td>
</tr>
<tr>
<td>020E</td>
<td>40</td>
<td>RTI</td>
<td>Return from interrupt</td>
</tr>
<tr>
<td>FFFA</td>
<td>00 02</td>
<td></td>
<td>Interrupt address vector</td>
</tr>
</tbody>
</table>

The circuit in figure 1 produces the 15 Hz interrupts. The 60 Hz signal is taken from the secondary of a 6.3 V filament type transformer. (The term is a hangover from vacuum tube days when many tubes had 6.3 V filaments somewhat like incandescent light bulbs). The input to IC1A, a CMOS buffer, is clamped between 5 V and ground by diodes D1 and D2, which can be any silicon small signal diodes at hand. Resistor R2 provides positive feedback to produce about a half a volt of hysteresis in the switching of the buffer. This hysteresis reduces false interrupts due to line voltage fluctuations and transients. The two D type flip flops in IC2 are used as cascaded divide-by-two circuits. The 15 Hz output from IC2 is buffered to drive TTL loads by IC1B. To prevent runaway power consumption and the resulting chip destruction, the unused inputs of the CMOS integrated circuits are grounded.

The nonmaskable interrupt of the 6502 is edge triggered; that is, the processor receives an interrupt whenever the voltage on the nonmaskable interrupt line goes from high (>2.4 V) to low (<2.4 V). The nonmaskable interrupt line can then stay low without generating another interrupt. When the processor receives a nonmaskable interrupt it jumps to the memory address stored at FF FA and FFFB, and pushes the address from which it was interrupted and the processor status onto the stack so that it can return to the preinterrupt computation as soon as it has processed the interrupt. A switch is shown between the 15 Hz interrupt and the NMI line so that interrupts can be disabled after power is applied until the interrupt handler for NMI has been loaded in volatile memory. If the interrupt handler is in read only memory, this switch can be omitted.

The contents of the accumulator and the X and Y registers should be saved by software when the interrupt is received and control switches to the interrupt handler program. This is done by pushing them onto the stack using appropriate instructions. Once the preinterrupt state has been safely preserved, the processing done as a result of the interrupt is performed. After the interrupt program has been completed, the preinterrupt contents of the Y and X registers and the accumulator are restored by pulling them off the stack. The processor then pulls the preinterrupt processor status and program address from the stack and returns to the previous computation. Listing 1 is a sample interrupt handler.

Listing 2 is a 24 hour clock generated in software by accumulating 15 Hz interrupts. This program contains only relative jumps and so is easily relocatable, either in volatile memory, EROM or PROM.

The operation of the program real time
Listing 2: Time of day clock. If the jump at line 206 in the interrupt handler of listing 1 references the CLOCK routine, locations C4 to C7 in memory address space are continuously updated with hours, minutes, seconds and 1/15 seconds respectively as the 15 Hz interrupts invoke its action. The 6502 code of this routine has been constructed to use relative branches only, so that it can be relocated anywhere in memory address space at the convenience of its user without modification of the object code.

CLOCK (Real Time Clock)

<table>
<thead>
<tr>
<th>Hexadecimal Address</th>
<th>Hexadecimal Code</th>
<th>Label</th>
<th>Op</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>F8</td>
<td>CLOCK</td>
<td>SED</td>
<td></td>
<td>Set decimal mode</td>
</tr>
<tr>
<td>0001</td>
<td>18</td>
<td></td>
<td>CLC</td>
<td></td>
<td>Clear carry</td>
</tr>
<tr>
<td>0002</td>
<td>A5 C7</td>
<td></td>
<td>LDA</td>
<td>FSEC</td>
<td>Load seconds fraction</td>
</tr>
<tr>
<td>0004</td>
<td>E9 01</td>
<td></td>
<td>ADC</td>
<td>1</td>
<td>Incr seconds fraction</td>
</tr>
<tr>
<td>0006</td>
<td>85 C7</td>
<td>STA</td>
<td>FSEC</td>
<td></td>
<td>Store seconds fraction</td>
</tr>
<tr>
<td>0008</td>
<td>38</td>
<td>SEC</td>
<td></td>
<td></td>
<td>Set carry</td>
</tr>
<tr>
<td>0009</td>
<td>E9 15</td>
<td>SBC</td>
<td>15</td>
<td></td>
<td>Subtract 15</td>
</tr>
<tr>
<td>000B</td>
<td>D0 C2</td>
<td>BNE</td>
<td>END</td>
<td></td>
<td>If not 15, go to end</td>
</tr>
<tr>
<td>000D</td>
<td>85 C7</td>
<td>STA</td>
<td>FSEC</td>
<td></td>
<td>Reset seconds fraction</td>
</tr>
<tr>
<td>000F</td>
<td>A5 C6</td>
<td>LDA</td>
<td>SEC</td>
<td></td>
<td>Load seconds</td>
</tr>
<tr>
<td>0011</td>
<td>18</td>
<td>CLC</td>
<td></td>
<td></td>
<td>Clear carry</td>
</tr>
<tr>
<td>0012</td>
<td>E9 01</td>
<td>SEC</td>
<td></td>
<td></td>
<td>Set carry</td>
</tr>
<tr>
<td>0014</td>
<td>85 C6</td>
<td>SBC</td>
<td>60</td>
<td></td>
<td>Subtract 60</td>
</tr>
<tr>
<td>0016</td>
<td>38</td>
<td>BNE</td>
<td>END</td>
<td></td>
<td>If not 60, go to end</td>
</tr>
<tr>
<td>0018</td>
<td>E9 60</td>
<td>STA</td>
<td>CEC</td>
<td></td>
<td>Reset seconds</td>
</tr>
<tr>
<td>001A</td>
<td>18</td>
<td>LDA</td>
<td>MIN</td>
<td></td>
<td>Load minutes</td>
</tr>
<tr>
<td>001C</td>
<td>18</td>
<td>CLC</td>
<td></td>
<td></td>
<td>Clear carry</td>
</tr>
<tr>
<td>0020</td>
<td>E9 01</td>
<td>SEC</td>
<td></td>
<td></td>
<td>Set carry</td>
</tr>
<tr>
<td>0022</td>
<td>85 C5</td>
<td>SBC</td>
<td>60</td>
<td></td>
<td>Subtract 60</td>
</tr>
<tr>
<td>0024</td>
<td>38</td>
<td>BNE</td>
<td>END</td>
<td></td>
<td>If not 60, go to end</td>
</tr>
<tr>
<td>0026</td>
<td>E9 60</td>
<td>STA</td>
<td>MIN</td>
<td></td>
<td>Reset minutes</td>
</tr>
<tr>
<td>0028</td>
<td>85 C5</td>
<td>LDA</td>
<td>HOURS</td>
<td></td>
<td>Load hours</td>
</tr>
<tr>
<td>002A</td>
<td>18</td>
<td>CLC</td>
<td></td>
<td></td>
<td>Clear carry</td>
</tr>
<tr>
<td>002C</td>
<td>E9 01</td>
<td>SEC</td>
<td></td>
<td></td>
<td>Set carry</td>
</tr>
<tr>
<td>0030</td>
<td>85 C4</td>
<td>SBC</td>
<td>24</td>
<td></td>
<td>Subtract 24</td>
</tr>
<tr>
<td>0032</td>
<td>38</td>
<td>BNE</td>
<td>END</td>
<td></td>
<td>If not 24, go to end</td>
</tr>
<tr>
<td>0034</td>
<td>E9 24</td>
<td>STA</td>
<td>HOURS</td>
<td></td>
<td>Reset hours</td>
</tr>
<tr>
<td>0036</td>
<td>D0 02</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0037</td>
<td>85 C4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0039</td>
<td>D8</td>
<td>END</td>
<td></td>
<td></td>
<td>Clear decimal mode</td>
</tr>
<tr>
<td>003A</td>
<td>60</td>
<td>RTS</td>
<td></td>
<td></td>
<td>Return</td>
</tr>
<tr>
<td>003C</td>
<td></td>
<td>HOURS</td>
<td></td>
<td></td>
<td>Storage for hours</td>
</tr>
<tr>
<td>0035</td>
<td></td>
<td>MIN</td>
<td></td>
<td></td>
<td>Storage for minutes</td>
</tr>
<tr>
<td>0036</td>
<td></td>
<td>SEC</td>
<td></td>
<td></td>
<td>Storage for seconds</td>
</tr>
<tr>
<td>0037</td>
<td></td>
<td>FSEC</td>
<td></td>
<td></td>
<td>Storage for seconds/15</td>
</tr>
</tbody>
</table>

CLOCK is straightforward. Time is stored in BCD in the first page of memory: hours in 00C4, minutes in 00C5, seconds in 00C6, and 1/15 seconds in 00C7. When an interrupt is received and the preinterrupt state saved, the interrupt handler will call the real time CLOCK at 0000 (location 0206 in listing 1). The second's fraction is incremented and compared to 15. If it is less than 15 the processor will jump to the end of the clock program for return, but if it equals 15 the second's fraction is reset to zero and the seconds are incremented. Seconds, minutes and hours are handled similarly, counting modulo 60, 60 and 24 respectively. At the end of the program the processor returns to the interrupt handler. The clock can be set simply by loading the desired time into the time memory locations.

By comparing desired program times with the time of the real time CLOCK program, the processor may perform programs at any desired interval, up to one day, which is expressable as a multiple of 1/15 second. As an example, a program to be performed once per second would be executed only at those times when CLOCK has counted the second's fraction equal to zero.

It is important that the real time CLOCK should not impose an unreasonable computational burden on the computer. Using a 15 Hz interrupt and the program shown here, this criterion is satisfied. When run in a computer using a 6502 processor with a 1 MHz clock, the interrupt service requires about 1100 µs per second. This 0.1% cannot be called an excessive burden on the computer.
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Floating Point Arithmetic

Many computer hobbyists are finding 8 bit integer arithmetic inadequate for a variety of mathematical applications. 16 and even 32 bit fixed point calculations are being used with increasing frequency because of their greater accuracy. However, these techniques are still inherently inadequate for calculations performed over a wide range of numbers.

Using a 16 bit integer format, only numbers from 0 to 65,535 can be represented. Larger or smaller numbers can be represented by moving the implicit radix point, but the range of discrete values still remains constant. The fractional part of the quotient in a division of one large number by another could be lost.

If one could dynamically slide the radix point, the number range would be dramatically increased. Using the same format, very small fractions and very large integers can be represented as floating point numbers. This is made possible by keeping track of the radix point's position separately with an exponent.

Floating Point Formats

There are many ways to represent floating point numbers, but there are only three basic formats, the others are variations. Two of these (the dominant ones in the traditional computer industry) use different binary representations. The third format, the one with the most variations, uses a binary coded decimal (BCD) representation, and is widely used in the electronic calculator and home computer industry.

The first format, shown in figure 1, is used in American National Standards Institute (ANSI) FORTRAN. It consists of a 24 bit mantissa, a 7 bit exponent and a sign bit.

The mantissa represents a fraction with the radix point assumed to be to the left of the most significant digit. The exponent is in excess-64 notation, which is a 7 bit two's complement notation with the sign bit inverted, eg: a zero exponent (160) is 100 0000, the minimum exponent (16-64) is 000 0000, and the maximum exponent (16-63) is 111 1111. The algebraic sign bit of the value is associated with the mantissa, and the exponent's sign is inherent in its format: a one sign bit indicates the number is negative, and a zero sign bit indicates a positive number.

This is the data storage format of floating point numbers. All such data is assumed to be normalized (ie: the most significant digit in the mantissa is nonzero unless the number itself is zero, in which case all 32 bits are zero). Before a calculation, the numbers are assumed normalized; after a calculation they are normalized in the floating point accumulator before being stored.

The actual calculations take place in the floating point accumulator and other floating point registers. These registers can be in the hardware or in memory (software). Hardware floating point registers (expensive, but much faster than software) are used by large computers and many minicomputers, whereas most small computers implement floating point in software to keep costs down.
With the ANSI format a "guard byte" is used in the floating point registers to maintain accuracy in performing the calculations. The guard byte (see figure 2) is an 8 bit extension to the least significant end of the 24 bit mantissa, temporarily creating a 32 bit mantissa during calculations. By keeping track of 32 bits of accuracy throughout the operation, significance will not be lost when storing numbers because the 32 bits can be rounded off to 24 bits. If a guard byte is not used, no rounding off is possible, and the effect would be the same as truncation (which can result in loss of accuracy very quickly, as will be shown later).

Numbers from $1.00 \times 16^{65}$ to $1.FFFF \times 16^{+62}$ can be represented by this format, resulting in an approximate range of from $10^{-79}$ to $10^{+76}$ with an accuracy of six or seven decimal digits. Table 1 lists several decimal numbers along with their hexadecimal ANSI FORTRAN format equivalents.

The next format, shown in figure 3, is also a binary format and is implemented by Digital Equipment Corporation (DEC) and Hewlett-Packard in their BASIC interpreters. It consists of a 23 bit mantissa plus a "hidden" bit, an 8 bit exponent and a sign bit. The format assumes that the number to be represented is always normalized: the most significant bit of the number is always understood to be 1 unless the entire number is equal to 0. This assumed "1" bit is the so-called "hidden" bit.

### Table 1: Several decimal numbers along with their ANSI FORTRAN floating point hexadecimal format equivalents (see figures 1 and 2).

<table>
<thead>
<tr>
<th>Decimal Number</th>
<th>Hexadecimal Floating Point Number (Hexadecimal Digits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>41 100000</td>
</tr>
<tr>
<td>6.00</td>
<td>41 600000</td>
</tr>
<tr>
<td>-1.00</td>
<td>C1 100000</td>
</tr>
<tr>
<td>0.50</td>
<td>40 800000</td>
</tr>
<tr>
<td>-0.50</td>
<td>C0 800000</td>
</tr>
<tr>
<td>100</td>
<td>42 640000</td>
</tr>
<tr>
<td>$2^{16} (-65,536)$</td>
<td>45 100000</td>
</tr>
<tr>
<td>2 - 16</td>
<td>3D 100000</td>
</tr>
<tr>
<td>-2 - 32</td>
<td>B9 100000</td>
</tr>
<tr>
<td>0</td>
<td>00 000000</td>
</tr>
<tr>
<td>16 - 65</td>
<td>00 100000</td>
</tr>
<tr>
<td>16^62</td>
<td>7F 100000</td>
</tr>
</tbody>
</table>

### Table 2: Examples of decimal numbers and their equivalents as encoded in the binary floating point format used in several BASIC interpreters (see figure 3).

<table>
<thead>
<tr>
<th>Decimal Number</th>
<th>Binary Floating Point Number (Hexadecimal Digits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>40 800000</td>
</tr>
<tr>
<td>6.00</td>
<td>41 C00000</td>
</tr>
<tr>
<td>-1.00</td>
<td>C0 800000</td>
</tr>
<tr>
<td>0.50</td>
<td>40 000000</td>
</tr>
<tr>
<td>-0.50</td>
<td>C0 000000</td>
</tr>
<tr>
<td>100</td>
<td>43 C80000</td>
</tr>
<tr>
<td>$2^{16} (-65,536)$</td>
<td>48 800000</td>
</tr>
<tr>
<td>2 - 16</td>
<td>3B 800000</td>
</tr>
<tr>
<td>-2 - 32</td>
<td>B0 800000</td>
</tr>
<tr>
<td>0</td>
<td>00 000000</td>
</tr>
<tr>
<td>2 - 128</td>
<td>00 800000</td>
</tr>
<tr>
<td>2^126</td>
<td>7F 800000</td>
</tr>
</tbody>
</table>

![Figure 2](image1.png) **Figure 2:** The ANSI FORTRAN floating point format showing the location of the "guard byte." The guard byte is an extra field which holds portions of intermediate calculations so that the final calculated value can be rounded off rather than truncated prior to further use.

![Figure 3](image2.png) **Figure 3:** A binary floating point format used by Digital Equipment Corporation and Hewlett-Packard in their BASIC interpreters. It consists of a 23 bit mantissa with a "hidden" bit, an 8 bit exponent and a sign bit. The format assumes that the number to be represented is always normalized: the most significant bit of the number is always understood to be 1 unless the entire number is equal to 0. This assumed "1" bit is the so-called "hidden" bit.
into six bytes: one byte for the sign, one byte for the exponent, and four bytes for the mantissa (including the guard byte). As a result there is a fair amount of processing necessary to load and store the floating point registers.

This format has a range of from $2^{+126}$ to $2^{128}$ or from approximately $10^{+38}$ to $10^{+128}$ with a 7 decimal digit accuracy (several examples are represented in table 2).

There are numerous BCD floating point formats currently in use. Mantissas range from as few as four digits to as many as 16 digits of accuracy, and exponents can typically range from $10^{+59}$ to $10^{+99}$, or even $10^{+127}$ to $10^{+127}$. The most popular format (see figure 4) has an 8 digit mantissa (four bytes of two digits per byte) with the decimal point assumed to be to the left of the most significant digit.

The mantissa sign is typically represented by a whole byte: 00 for positive and 011 for negative. A variety of formats use one byte to represent the exponent.

One of the more frequently used formats is binary in the form of excess 128 notation. The exponent format itself is identical to the Digital Equipment Corporation format discussed earlier, but represents a power of ten instead of a power of two. Thus, an exponent of 84 base 16, using DEC's format, signifies two to the fourth power, and using the BCD format, ten to the fourth. The exponent represents the same power in both cases, but of different bases.

Eight digits are packed into four bytes in what is known as packed BCD (four bits represent one BCD digit).

The same format is usually used for both storage of data and actual calculations. This means neither a guard byte nor round off is used. The need for a guard byte is circumvented by using more significant digits than are actually necessary, e.g.: calculating to eight digits for 6 digit results, or calculating to nine digits for 8 digit results. This of course makes it necessary to use more memory per number for storage.

Some examples of numbers in this format are found in table 3.

Table 3: Several decimal numbers along with their equivalent floating point representations as encoded in BCD hexadecimal digits.

<table>
<thead>
<tr>
<th>Decimal Number</th>
<th>BCD Representation (Hexadecimal Digits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>00 81 10000000</td>
</tr>
<tr>
<td>6.00</td>
<td>00 81 60000000</td>
</tr>
<tr>
<td>1.00</td>
<td>FF 81 10000000</td>
</tr>
<tr>
<td>0.50</td>
<td>00 80 50000000</td>
</tr>
<tr>
<td>0.90</td>
<td>FF 80 90000000</td>
</tr>
<tr>
<td>100</td>
<td>00 83 10000000</td>
</tr>
<tr>
<td>216, 65, 536</td>
<td>00 85 65536000</td>
</tr>
<tr>
<td>2.16</td>
<td>00 7C 15294739</td>
</tr>
<tr>
<td>2.32</td>
<td>FF 37 23282064</td>
</tr>
<tr>
<td>10−126</td>
<td>00 00 00000000</td>
</tr>
<tr>
<td>10−128</td>
<td>00 01 10000000</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 4: A BCD floating point format consisting of an 8 bit sign, an 8 bit exponent and a 32 bit (8 digit) mantissa.

Continued on page 180
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Photo 1: The author's computer, seen from the component side, was assembled using two sections of perforated board (0.1 inch grid) and sockets for all integrated circuits. The arithmetic unit is in the lower right hand section in this photograph, the eight memory circuits are in the lower left hand region, and the control section is implemented by the parts on the board at the top of this photograph.

Building a Computer from Scratch

With so many excellent microprocessors available today, the experimenter needs a good reason to design and build a personal computer from scratch. That reason will certainly not be one of economy. The best available microprocessors offer so much capability at such a low price that one cannot hope to save money by building a computer from scratch. For many, the reason will simply be the challenge of doing it. For others, the reason will be more practical (perhaps to gain some capability not readily available from an off-the-shelf microprocessor). And for still others, the reason will be to learn more about the techniques of computer design.

While any of these reasons is certainly valid, the design of a computer from the ground plane up is still generally regarded as an art that only the foolhardy would undertake. In reality, though, the job is not nearly as mysterious as it seems. For proof I offer the fact that when I began this project I had no design experience with TTL (or experience with any form of electronics design for that matter). Indeed, I chose this project to learn how to use TTL parts, on the assumption that the microprocessor I planned to buy would eventually become bored talking to my TV set.

Because of my inexperience with TTL circuitry, I chose to simplify the design as much as possible at every step. As a result, the major strengths of this computer are its low cost and its simplicity. With judicious shopping, it should be possible to construct the computer for around $65, including everything but the power supply. With only four instructions, the computer offers an instruction set that is guaranteed not to overwhelm the novice. At the same time, the signals that drive the various modules of the computer are readily accessible so that the electronics can be seen to work “as advertised.”

Despite the simplicity of the computer, its microprogrammed bus oriented architecture conforms to the design principles in the most modern of minicomputers.

This article gives the groundwork from which a serious student or hacker can design and build his/her own personal computer.
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Table 1: The instruction set for the computer. N is any 6 bit integer. The bits of N are denoted by mmmnnn.

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Object Code</th>
<th>Operation Performed</th>
</tr>
</thead>
<tbody>
<tr>
<td>WIO N</td>
<td>00nnnnnn</td>
<td>Wait for input to location N. Display current contents of Location N while waiting.</td>
</tr>
<tr>
<td>ADD N</td>
<td>01nnnnnn</td>
<td>Add data in location N to accumulator.</td>
</tr>
<tr>
<td>STN N</td>
<td>10nnnnnn</td>
<td>Store negative of accumulator in location N.</td>
</tr>
<tr>
<td>JGE N</td>
<td>11nnnnnn</td>
<td>Jump to location N if accumulator is greater than or equal to zero.</td>
</tr>
</tbody>
</table>

At the same time it also describes a very simple computer, one that can be built by a student as a science project, by a teacher for a laboratory demonstration, or by a novice hacker who just wants to learn about computers without a large investment.

The Instruction Set

The most important task facing the computer designer is choosing the instruction set. In the case of this computer, every effort was made to choose the simplest possible instruction set. Therefore, multiple word instructions, stacks, register files, interrupts and elaborate I/O facilities were not permitted. An 8 bit word length was chosen because it is the smallest size that can be reasonably expected to use one word per instruction. This constrained me to an instruction set of four op codes and a directly addressed memory space of 64 bytes. The instruction set is summarized in table 1.

The ADD instruction is included for obvious reasons. The STN instruction was chosen to store the negative value of the accumulator's contents so that both subtraction and addition could be done. (In particular, by executing STN N and ADD N in sequence, the accumulator can be cleared.)

The JGE instruction is an all purpose test or branch instruction. By clearing the accumulator before executing a JGE, an unconditional branch results. Alternatively, by placing a number in the accumulator, the JGE tests whether the number is positive or negative.

The WIO instruction provides the only means for loading and examining memory. There are no front panel switches for this function, so everything must be done under the control of a suitable program (including the loading of that program itself). Therefore, the WIO instruction requires special attention. When executed, WIO N brings the computer to a halt with the contents of location N displayed in the LED display. At this point, the user will enter data into a switch register. When the continue button is pressed, the data will be written into memory location N, thus destroying the data just displayed. In effect, the instruction combines the wait, input and output instructions of the conventional computer.

A particularly useful application of this instruction occurs when the instruction at location N is a WIO N+1 instruction. At that point the data entered by the user becomes the next instruction to be executed!

The most important program for this computer is the bootstrap program. Other programs are left to the reader to devise. The bootstrap program, which provides the simplest practical way to load data into the computer, is loaded as follows. When the reset button is pressed, the computer will wait to accept data into location 0. The data will be stored, then executed when the continue button is pressed. Needless to say, the data loaded must be chosen carefully if the user is to be able to keep control of the computer. The data that permits this is the WIO 1 instruction. When this instruction is loaded into location 0 and executed, the computer will halt, ready to accept data into location 1. When the continue button is again pressed, the new data is stored. The computer resumes execution with the next instruction in memory, namely, the instruction just entered into location 1. Again, that instruction must be carefully chosen: a WIO 2 is a good choice. The computer will again halt, at which time a JGE 0 should be entered. After JGE 0 is loaded into location 2 and executed, we will have completed entering the bootstrap program. The JGE 0 will unconditionally jump to the start of the bootstrap program (location 0) because the accumulator is cleared at restart time.

To use the bootstrap program, enter pairs of bytes as follows: a 6 bit address followed by eight bits of data to be placed at that address. For example, if, in response to the first two halts in the bootstrap program, we enter an octal 003 followed by an octal 010, then the value 10 will be placed in location 3. In this case, the bootstrap program returns to location zero, where it is ready to accept another pair of bytes. Once a program is loaded, we can execute it by entering the appropriate JGE instruction in response to the next halt instead of the address data pairs.

Hardware for the Computational Unit

The computer is shown in block diagram form in figure 1. The control unit, to be discussed later, interprets the instruction
set and generates the control signals which tell the computational unit how to execute instructions. This is a true microprogrammed computer with a 32 word by 16 bit control store. (For control store contents see table 2.) The system is organized around an 8 bit bidirectional bus. Because of this, each module that uses the bus may be built as an independent unit without regard to how the other modules work, an obvious advantage.

When two modules need to exchange data, one will put the data on the bus while the other will read it from the bus. The arrows in figure 1 show the directions in which such data transfers can be made. The only restriction is that no two modules are permitted to put data on the bus at the same time. The use of the bus system allowed me to build the entire computational unit before giving detailed thought to how the control unit would be implemented (the algorithm for successful computer design being “divide and conquer”).

The arithmetic logic unit buffer register deserves comment. During an ADD operation, data from memory is placed on the bus. The arithmetic logic unit reads the data from the bus and adds it to the accumulator. The output of the arithmetic logic unit must eventually find its way back to the accumulator. This is done by putting the data on the bus, an action permitted only after the memory is no longer using the bus. The arithmetic logic unit buffer is provided to give a temporary holding place for the sum until the memory can release the bus.

Note that there is no instruction register or memory data register. This represents a departure from conventional computer design made possible by the simplicity of the instruction set. The conventional memory address register and program counter are present, however, and serve their usual purpose.

For even this simple computer, there are some 30-odd signals between the control and computational units. Therefore, I found it essential to establish a system for naming the signals. Names are best chosen to suggest what the signal does as well as the voltage
Figure 2: The memory address register and the memory. Data is addressed by six bits of the 74174 memory address register and stored in the 7489 memories, each of which has 16 4-bit registers. A total of eight 7489s are required to make up the 64-byte memory.

required to achieve the effect. For example, AC-CLR-L is a signal that, when brought low, clears the accumulator. Conversely, when PC-INCR-H is brought high, the program counter is incremented. The eight bus lines are named BUS0 thru BUS7 (in order of arithmetic significance). The master clock is named MCLK; its complement is called CCLK.

The memory and memory address register are shown in figure 2. I chose to base my system around the 7489 64-bit memory integrated circuit largely because I happened to have them. In a redesign, a 2101-based memory might be a slightly better choice, but the present design does have the advantage of showing how multiple chip memories are controlled. Each 7489 contains sixteen 4-bit registers; eight 7489s are required for a 64-byte memory. Data is addressed by a 6-bit memory address register (a 74174).

The memory address register is loaded with data on the bus by MAR-CLK. Alternatively, it can be cleared by MAR-CLR-L (eg: when the reset button is pressed). The two high bits of the memory address register are decoded together with MEM-ENAB-L by a 74155 decoder. If MEM-ENAB-L is low, the high two bits select one of four pairs of 7489s, and the low four bits select one of the 16 registers in the selected pair. (If MEM-ENAB-L is high, the memory is disabled.) In this way, a byte of memory is addressed. Now, if WRITE-MEM-L is low, that byte will be written using data from the bus. But when WRITE-MEM-L is high, the complement of the data at the addressed byte will be placed on the bus. The fact that the 7489 complements data stored in it is used to advantage by the STN instruction, as we will see later.

The accumulator (AC), arithmetic logic unit, and arithmetic logic unit buffer are shown in figure 3. The accumulator is constructed from a pair of 74175 integrated circuits. It is cleared by AC-CLR-L (eg: at reset time), and it is loaded by AC-CLK. The sign bit of the accumulator is sent (as AC-GE-L) to the control hardware, where it is used for the JGE instruction. The arithmetic logic unit, in the form of a pair of 74181s, is used in two ways. When executing an ADD instruction, ALU-ADD-L will be brought low, so that the arithmetic logic unit computes AC plus memory. This sum is then latched into the arithmetic logic unit buffer (a pair of 74173s). Once memory is no longer using the bus, BUS-BUFL can be brought low to place the sum on the bus. The sum can then be latched back into the accumulator to complete the add cycle. Alternatively, to execute the STN instruction, ALU-ADD-L will be brought high. Now the 74181 will compute “accumulator minus one,” which is latched into the buffer and eventually written into memory. The convenience of a complementing memory can now be appreciated, since in two's
complement arithmetic, the complement of AC-1 is AC. (With a 2101-based memory, the inversion would have to be done with extra hardware.)

The last part of the computational unit, shown in figure 4, consists of a program counter, LED display, and switch register. The program counter consists of two 74LS161 counters and two three-state buffers. (The 74161 is not an acceptable substitute for the 74LS161 because of differences in the way their clocks behave, a fact I learned the hard way.) The program counter is cleared by PC-CLR-L. It can be loaded (incremented) on the next clock transition after PC-LOAD-L (PC-INCR-H) becomes low (high). The output of the program counter is enabled onto the bus by PC-BUS-L.

The LEDs are driven by ordinary inverters. The inverters assure that the LEDs are lighted for the high bus lines rather than the low ones. The switch register (a DIP switch) is wired so that a closed switch drives the associated bus line low. This is because the memory complements data. The switch outputs are enabled onto the bus by a pair of 74125 three state buffers under the control of BUS-SWI-L.

Hardware for the Control Unit

The control unit, shown in figure 5, is responsible for providing the various signals in the proper sequence to drive the computational unit. To simplify the design, a microprogrammed architecture was chosen. In this design, the control logic is held in a pair of 74288 programmable read only memories in the form of a 12 word (16 bits per word) microprogram. When one or another word is selected from the programmable read only memory, the individual bits of the selected word are delivered more or less directly to the computational unit as individual signals. For example, the PC-INCR-H bit of the microprogram directly drives the PC-INCR-H line to the program counter. Similarly, the BUF-LOAD-L bit directly drives the BUF-LOAD-L line to the arithmetic logic unit buffer.

Several other lines can be readily identified that are directly driven by the programmable read only memory. From this it is clear that the problem of designing a control unit reduces to deciding which
Figure 4: Program counter circuitry.

Signals are to be high or low at what time, programming a programmable read only memory to contain this information, and devising a way to select the proper word from the programmable read only memory at the proper time so that the appropriate signals can be generated.

Occasionally, microprogram bits do not drive signal lines directly but must first undergo some transformation. For example, in figure 5 we see that the AC-LOAD-L bit of the microprogram is gated with CCLK to create the clock that loads the accumulator. (It would not be permissible to drive the accumulator directly from AC-LOAD-L, because the signal has to be delayed by a half clock cycle.) Similarly, MAR-CLK is derived by gating MAR-LOAD-L together with CCLK, and PC-LOAD-L is created by gating together AC-TEST-L and AC-GE-L, so that the program counter is loaded only when the microprogram allows it and the accumulator is not negative.

The BUSDAT0 and BUSDAT1 lines are another case in which a transformation is required. In this case the two lines are decoded by a 74155 decoder to select one of four possible sources of data for the bus, namely, the switch register, program counter, ALU-BUFFER and memory. These are selected by BUSDAT1, BUSDAT0 values of (L, L), (L, H), (H, L) and (H, H), respectively. This arrangement saves bits in the microprogram as well as insuring that only one device can put data on the bus at any one time. Note that the open collector memory used is logically connected to the bus by enabling an appropriate memory chip. (The memory chips must also be enabled before writing memory.)

In order for the microprogram to deliver its control signals to the computational unit in the appropriate order, some means must be provided for sequencing thru the words in the programmable read only memory. In this computer, we have allocated six bits (BASE0 thru BASE4, and OPJMP-H) to accomplish this. First, assume that OPJMP-H is low. "BASE" then determines a microprogram address (the base address) which is fed forward directly to the 74174 microprogram address register. When CCLK goes high, the
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Figure 5: The microprogrammed control unit of this computer.
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Figure 6: A finite state graph representation of the microcode shown in table 2. The five digit binary numbers shown in each state are the control memory addresses when the computer is in that state. Note that a 4-way branch occurs at state 00010 (left side of the graph), indicating the four different op codes implemented for this computer. The resulting initial states for the four op codes are shown in contrasting color.

Base address becomes the new microprogram address, thus defining the next microprogram word to supply control signals. Continued clocking of the 74174 thus causes the microprogram to sequence through whatever steps it has chosen for itself, and at the same time, to deliver control signals to the computational unit.

To this next address scheme we must add some means of varying the microprogram flow based on the op codes encountered. This is the reason for having the OPJMP-H bit. When it is high, the base address is no longer the next address. The latter is formed by performing a logical OR of the base address with the op code (assuming that the bus holds the instruction to be executed). Ordinarily OPJMP-H will be set high in a microinstruction that has the two lowest bits in BASE set to zero. In that case, each op code will produce a different next address.

To see the next address scheme in action, consider table 2 and figure 6 in which the microcode for the computer is shown. If we start at microcode address 00000, which is the case when the start button is pressed, then we find that OPJMP-H is low, so the next address will be at BASE=01000. Subsequent addresses are 01001, 00001, and finally 00010. At this point, OPJMP-H goes high. Let us assume for sake of example that an ADD instruction has been placed on the bus (op code = 01). Then the next address will be 00100 or 01 = 00101. The subsequent addresses are then 01010, 01011, 00001,
and so on. Note that address 00001 marks the beginning of an infinite microprogram loop that fetches, interprets and executes the instruction set.

One more microprogram bit (WAIT-L) remains to be described. It provides a way to halt our computer at the WIO instruction. As long as this bit remains high, the rather involved network of NAND gates conspires to pass clock pulses so that the microprogram executes freely. But when the WAIT-L bit goes low, a flip flop changes state and permits the clock synchronization network to turn off the clock at the end of the current clock cycle. This stops the computer, but it can still be single stepped by hand so that we can study the microprogram. Clock pulses will remain disabled until the continue button is pressed; then the flip flop reverts to its original state, enabling the clock synchronization network to pass pulses at the start of the next clock cycle. This restarts the microprogram, and hence the computer. The edge trigger on the continue button prevents the computer from continuing right thru several WIO instructions. (A properly debounced continue button is essential here for the same reason.)

The restart button shown in figure 5 allows us to prime the computer or to abort a malfunctioning program. Pressing it causes the accumulator, program counter, memory address register and microprogram address register to be cleared and paves the way for the bootstrap program to be reloaded.

In table 2 I have listed the version of microcode that implements the instruction set laid out earlier. The various fields are identified at the top of the table, with additional explanatory notes at the bottom. Figure 6 uses the information in table 2 to show a complete state diagram of the instruction set. Each state (a colored circle) is one address in the control memory represented by one line in table 2.

One point worth keeping in mind concerns timing. At the beginning of each cycle,
Table 3: Power wiring table for the circuits in figures 2 thru 5.

<table>
<thead>
<tr>
<th>Number</th>
<th>Type</th>
<th>+5 VDC</th>
<th>Gnd</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>74174</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC2</td>
<td>74155</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC3</td>
<td>7489</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC4</td>
<td>7489</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC5</td>
<td>7489</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC6</td>
<td>7489</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC7</td>
<td>7489</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC8</td>
<td>7489</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC9</td>
<td>7489</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC10</td>
<td>7489</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC11</td>
<td>74175</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC12</td>
<td>74175</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC13</td>
<td>74181</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td>IC14</td>
<td>74181</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td>IC15</td>
<td>74173</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC16</td>
<td>74173</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC17</td>
<td>74LS181</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC18</td>
<td>74LS181</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC19</td>
<td>74125</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC20</td>
<td>74125</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC21</td>
<td>7404</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC22</td>
<td>7404</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC23</td>
<td>74125</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC24</td>
<td>74125</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC25</td>
<td>74288</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC26</td>
<td>74288</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC27</td>
<td>74174</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC28</td>
<td>74155</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>IC29</td>
<td>555</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>IC30</td>
<td>7400</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC31</td>
<td>7400</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC32</td>
<td>7402</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC33</td>
<td>7432</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC34</td>
<td>7408</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>IC35</td>
<td>7410</td>
<td>14</td>
<td>7</td>
</tr>
</tbody>
</table>

as CCLK goes high, a new microinstruction will appear at the output of the programmable read only memories. This might cause data to be placed on the bus, or a sum to be formed by the arithmetic logic unit, etc. In any case, by the middle of the clock cycle, when CCLK goes low, it is assumed that all such data has settled. Therefore it will be safe to latch the data set up during the first half of the cycle into some appropriate device. By the end of the cycle, the latched data will also be stable, so that a new microinstruction can be safely executed. In this way we have avoided timing problems without going to a two phase clock. I estimate that the cycle time of the computer could approach 300 ns, although I have not pushed the computer to its limit.

Summing Up

The design of this simple computer will certainly not appeal to everybody. Expanding the design to a 12 bit word length would permit much more flexibility in the instruction set, perhaps enough to even make the computer practical. For example, indirect addressing might be thrown in, or a subroutine calling mechanism. The WIO instruction could be broken down into separate wait, input and output instructions, allowing the computer to do things like flash its lights. (The present design comes to a grinding halt with each flash.) A more elaborate bus structure, and some sort of flexible IO facility are other obvious improvements that one could try. Alternatively, a 12 bit word length could be used to increase the address space. Each of these changes would add to the cost and complexity of the design, but could lead to a more useful computer.

Although the requirements of the bootstrap loader do impose some severe constraints on the instruction sets that can be implemented with this architecture, you will probably want to try a few variations. It might be possible to implement two instruction sets: one defined by the lower 16 words of the programmable read only memory for loading programs, and the other in the upper 16 words for experimentation. A switch would be used to select between the instruction sets.

Once you have mastered the ideas behind the design of this computer, you'll be well on your way to building a serious computer. All you need to do is sit down and write out an instruction set that best fits your personal needs and then implement it in hardware. Bit slice microprocessors such as the AM2900 series offer a very attractive way of doing this.
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- Write protection in 16K blocks; and
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CIRCLE 58 ON INQUIRY CARD.
A 6502 Personal System Design:

Documenting Komputer -- A Guide to the Details

The design information included with this article, together with the excellent documentation provided by MOS Technology on the 6502 design, should be complete enough to enable the advanced experimenter to build a similar Komputer. The details provided here cover a basic processor, but do not include a detail design of a programmable memory board which is a necessary part of a usable system. David Brader is currently working on an 8 K dynamic memory board, with invisible refresh, to be used in Komputer. The details of the wiring and construction of Komputer are shown in the several figures, tables and photographs, as well as listing 1. As a short guide to these materials here is a detailed table of contents to the article.

Front Panel Assembly: This is the circuit with various displays and switches which is mounted on the front panel, and talks to the front panel interface module via a multi-conductor cable from P2 to J1.

Front Panel Interface Module: This is the logical interface between the processor's backplane bus and the front panel. It is the home of address decoding and the read only memory with the front panel service programs.

Central Processing Module: This is the heart of the Komputer system, a board which contains the 6502 processor, and associated buffering and clocking circuits which define the backplane bus structure of the system.

TIM Interface Module: This card is provided so that the MOS Technology "Terminal Interface Monitor," or TIM program, can be used with Komputer.

Miscellaneous Items:

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Table 5: Shows a master list of all integrated circuits, where they appear by figure, wiring, map locations for the physical layout shown, and power wiring connections.

Table 1: Shows the allocations of memory for Komputer, as implemented here.

Listing 1: Shows the front panel control program which can be used to manipulate Komputer without any other monitor program.

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Kavcat Kompuutar

It is with some trepidation that we present the details of the Kompuutar design. The design is complete and comprehensive, but Murphy is addicted to complete and comprehensive designs. Thus we’d like readers to be aware that there is a non-zero probability that errors exist in this magazine representation of author David Bruder’s design. We suggest that serious homebrewers of Kompuutar treat these pages as a detailed design guide, to be used with the standard design documentation of the chips involved. But us with any road map, do not be afraid to question and verify what you see with your own knowledge and experience.

David Bruder reports that a local friend of his has built a second Kompuutar from the same set of blueprints which were the source of the circuit in this article. The experiences of the second builder were reflected in his corrections and changes to the drawings which are part of the normal “author proof” cycle applied to articles. Based on our own experiences with microprocessors, this report from David, and a tremendous amount of “desk debugging” of the article, we believe the information presented here is complete and buildable. However we highly recommend that readers who attempt to duplicate the design have sufficient experience with digital hardware and logic so that detailed understanding of its operation is possible. This is not a novice’s project.

It all started at WESCON 1975, in San Francisco. It was there that I discovered what a “hospitality suite” is. In a hotel not far from the convention site, MOS Technology Inc had set up their WESCON hospitality suite. A hospitality suite is a bit like Las Vegas: some refreshments, a couple of elegantly decorative ladies, flashing lights and shiny gizmos, and the age old desire to persuade you and your money to part company.

I decided to stop and at least get a free drink. A man by the bar said, “Help yourself,” so, being afraid of a one drink limit, I poured a double. As I left the bar area, I spotted a friend. We struck up a conversation about common friends and assignments, which lasted through half my drink and all of my clearheadedness. As our conversation ended, I noted some blinking LEDs and shiny new printed circuit boards. These boards were surrounded by several professional looking guests, giving the hardware an illusion of significance. So I went over to investigate.

I listened, wide eyed, to the saga of the MCS6502 as I slowly finished my drink. After the story ended, everyone seemed to be forming a line in a different part of the suite. Feeling part of the group now, I moved to the line. A little bit later, I remember being at the head of the line and the last thing I recall was handing two 20 dollar bills to a very pretty lady.

That evening, after sobering up, I discovered what I had done. There on my bed, stark naked, was a bright new MOS Technology Inc MCS6502 microprocessor chip and its manuals. Well, now the only
thing to do was to build a computer with the chip. After several days reading, I realized that building a computer was not going to be all that easy. I also realized that the initial $36.75 investment was but a drop in the proverbial bucket of costs.

**Designing the Kompuutar System**

Since my $36.75 investment was going to need considerable financial and design support, it was clear that making a project out of the computer would require planning. The first thing I had to accomplish was a specification of the features I wanted in my machine. I had had a good deal of experience with the Data General NOVA 1200 minicomputer, which led me to favor its functional front panel switch setup. With this input, I decided that the new machine would have the front panel functions of master reset, halt, program run, single instruction step, memory examine, examine the next memory location, deposit, deposit to the next memory location, load processor register, and enter data or address information from switches. I also knew that I wanted to be able to display the information on the data lines and address lines. I decided to use hexadecimal LED displays for the address bus information, but not for the data bus. My reasoning was that the address bus is always considered to be a numerical value, whereas the data bus is sometimes considered to be numeric data, but is sometimes viewed as a combination of individual bits. (If the data bus was showing hexadecimal E6 and you wanted to know if bit 5 was on or off, you would probably have to think for a while to make sure.) Another argument in favor of discrete LED indicators for each bit is the fact that hexadecimal displays are a bit more expensive.

After reading more about the MCS6502, a trait common to the other single chip processors revealed itself. The status register, accumulator, index register X, index register Y and stack pointer register do not come out of the chip on their own sets of pins. All that information was going to be hidden from the operator (me) sitting in front of the machine. I knew I would have to design digital logic to get that information out of the chip and displayed upon some sort of front panel. I even decided to go one step further and build in the capability to set or reset the status flags from the front panel. Being able to throw a switch and set the carry flag, for example, is a very handy capability when debugging a conditional branch in some program.

I decided to use toggle switches for the 16 data inputs because the state of individual switches could then be tested in software and used to control options in a program. This complicates the entry of an address (which is displayed in hexadecimal) but gains an ability to write applications programs which can be modified by the state of these input switches.

With these considerations in mind, the front panel design was fixed up as a starting point for the processor. I then started to work on the detailed logic design of what came to be called Kompuutar in my lexicon. After a month's work, I realized that the

<table>
<thead>
<tr>
<th>Backplane (P1) Pin Designation</th>
<th>Logic Diagram Mnemonics</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>+5V</td>
<td>voltage supply</td>
</tr>
<tr>
<td>B</td>
<td>IRQ 1</td>
<td>interrupt 1</td>
</tr>
<tr>
<td>C</td>
<td>A0</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>A2</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>A4</td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>A6</td>
<td>address bus lines (even)</td>
</tr>
<tr>
<td>H</td>
<td>A8</td>
<td></td>
</tr>
<tr>
<td>J</td>
<td>A10</td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>A12</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>A14</td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>IRQ 2</td>
<td>interrupt 2</td>
</tr>
<tr>
<td>N</td>
<td>IRQ 3</td>
<td>interrupt 3</td>
</tr>
<tr>
<td>P</td>
<td>D0</td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>D2</td>
<td>data bus lines (even)</td>
</tr>
<tr>
<td>S</td>
<td>D4</td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>D6</td>
<td></td>
</tr>
<tr>
<td>U</td>
<td>SO</td>
<td>set overflow flag</td>
</tr>
<tr>
<td>V</td>
<td>PHICLK</td>
<td>φ1 clock</td>
</tr>
<tr>
<td>W</td>
<td>MASRST</td>
<td>master reset</td>
</tr>
<tr>
<td>X</td>
<td>RW</td>
<td>read and write</td>
</tr>
<tr>
<td>Y</td>
<td>IRQ 4</td>
<td>interrupt 4</td>
</tr>
<tr>
<td>Z</td>
<td>GND</td>
<td>ground</td>
</tr>
</tbody>
</table>

Table 1: Kompuutar bus list. This table gives the backplane socket pin identifications, mnemonics used in the logic diagrams, and a short description of the line's use. The pin designations are the standard ones printed on the Vector prototyping cards and embossed in the typical 44 pin sockets.
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front panel logic was going to contain nearly 220 TTL integrated circuits if I implemented it with a conventional logic design. After that false start, I thought about a simplification made possible by a read only memory program, or "firmware" as it is sometimes called. I could replace most of the front panel logic with a program burned into a single read only memory integrated circuit. With a PROM program and 16 bytes of volatile programmable memory, the 6502 processor itself would operate the front panel of the system. The integrated circuit count for the front panel including the programmable read only memory and 16 bytes of volatile solid state memory was now reduced to just over 50 packages.

**System Design Philosophy**

During the process of designing the front panel, I worked out a total system design philosophy which goes like this:

- There would be a central processing unit and peripherals. The peripherals would be interfaced to the processor with a minimum of hardware by using memory address interfaces wherever possible.
- The system would be modular. A common backplane would be defined. Each module would be connected to the other modules through this backplane. Each socket on the backplane would be wired pin by pin to every other socket on the backplane.
- An address allocation map for the system would be defined. This would define addresses for hardware (peripherals), firmware (read only memory programs) and main programmable memory use.

The front panel design I had already created follows the first point of this philosophy quite well. It has several separate peripherals. Some are input devices, some are output devices, and some are a combination of both functions. Each is interfaced as a memory address and operated by firmware with a minimum of supporting hardware. Details of front panel operation will be discussed a little later in this article.

The physical arrangement of the design implements the details of the second point in the philosophy. The front panel assembly is connected to the top of a Vector prototyping card which contains the programmable read only memory with the front panel servicing routines. This card in turn plugs into the backplane bus which is implemented with a Vector card cage and edge connectors. By pulling the front panel card out of the backplane, the Kompuutar system can be isolated from the front panel completely. Similarly, the rest of the Kompuutar system is fabricated on Vector 3662 cards. Each card module contains one complete section of the system. These modules include the central processing unit card with the 6502 and bus interfacing chips, and a terminal interface card. Eventually 8 K byte programmable (volatile) memory cards will be part of the system. The cage I used has room for eight memory cards for a total of 64 K bytes. Since the backplane is wired from pin to corresponding pin of each socket, the cards can be placed in any available socket in the card cage. Table 1 shows the definitions of all the bus pins. In developing the system, I used an extender card plugged into the backplane so that I could have access to the various modules with an oscilloscope probe.

The third part of the design philosophy

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Type of Hardware</th>
<th>Usage of Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 to 3FFF</td>
<td>Volatile programmable memory</td>
<td>This is the general programmable memory region for user applications programs. Locations 0000 to 01FF are dedicated to scratch pad and stack use by the architecture of the 6502 processor.</td>
</tr>
<tr>
<td>4000 to 6FFF</td>
<td>Unimplemented</td>
<td>This region is reserved for 12 K of general user memory expansion. When the TIM monitor interface card is in the system, this area is reserved.</td>
</tr>
<tr>
<td>7000 to 73FF</td>
<td>TIM read only memory</td>
<td></td>
</tr>
<tr>
<td>7400 to 7FFF</td>
<td>Unimplemented</td>
<td></td>
</tr>
<tr>
<td>8000</td>
<td>Scratch pad memory with external visibility</td>
<td>Current accumulator value maintained by front panel service program</td>
</tr>
<tr>
<td>8001</td>
<td>Scratch pad memory with external visibility</td>
<td>Current X register value</td>
</tr>
<tr>
<td>8002</td>
<td>Scratch pad memory with external visibility</td>
<td>Current Y register value</td>
</tr>
<tr>
<td>8003</td>
<td>Scratch pad memory with external visibility</td>
<td>Current processor flag values</td>
</tr>
<tr>
<td>8004</td>
<td>Scratch pad memory</td>
<td></td>
</tr>
<tr>
<td>8005</td>
<td>Scratch pad memory with external visibility</td>
<td>Current stack pointer value</td>
</tr>
<tr>
<td>8006</td>
<td>Scratch pad program begins here</td>
<td></td>
</tr>
<tr>
<td>8007 to 8008</td>
<td>Scratch pad</td>
<td>Current address register value, displayed through locations 8014 and 8015</td>
</tr>
<tr>
<td>8009 to 800C</td>
<td>Scratch pad program area</td>
<td></td>
</tr>
<tr>
<td>800D</td>
<td>Scratch pad memory with external visibility</td>
<td>Current data at memory location in address register locations 8007 to 8008</td>
</tr>
<tr>
<td>800E 800F</td>
<td>Scratch pad</td>
<td>Front panel request register (see table 3)</td>
</tr>
<tr>
<td>8010</td>
<td>Read only data input</td>
<td>Low order address and data switch register</td>
</tr>
<tr>
<td>8011</td>
<td>Read only data input</td>
<td>High order address switch register</td>
</tr>
<tr>
<td>8012</td>
<td>Read only data input</td>
<td>Flag data latch and binary display</td>
</tr>
<tr>
<td>8013</td>
<td>Write only display</td>
<td>Low order address latch</td>
</tr>
<tr>
<td>8014</td>
<td>Write only display</td>
<td>High order address display latch</td>
</tr>
<tr>
<td>8015</td>
<td>Write only display</td>
<td>High order address display latch</td>
</tr>
<tr>
<td>801F</td>
<td>Idle command address</td>
<td>References cause processor to idle</td>
</tr>
<tr>
<td>8020 to 80FF</td>
<td>Programmable memory</td>
<td>Unimplemented hardware device addresses</td>
</tr>
<tr>
<td>8100 to 81FF</td>
<td>Unimplemented</td>
<td></td>
</tr>
<tr>
<td>F000 to F0FF</td>
<td>Programmable read only memory allocations for systems programs</td>
<td>This area is expected to be used by interrupt service routines, utility subroutines and the like, programmed into read only memory parts.</td>
</tr>
<tr>
<td>FE00 to FFFF</td>
<td>Read only memory</td>
<td>This region is allocated to the firmware which controls the front panel. The 6502's interrupt vectors are programmed into the last portion (see listing 1).</td>
</tr>
</tbody>
</table>

*Table 2: A memory allocation map for Kompuutar. When interfacing both peripherals and programming to a single memory address space, it helps to make a memory map to keep track of allocations.*
Dynabyte builds the Great Memory

We cut up a Dynabyte 16k dynamic RAM board and constructed this pyramid to illustrate an important point: Dynabyte designs and builds memory boards with the same unshackled engineering ability and technical skill that went into Egypt's Great Pyramid.

One of the seven wonders of the ancient world, the Great Pyramid has been standing on the desert for an incredible 4,400 years. Although its enormous base covers 13 acres, it is perfectly square. Rising 450 feet, it is as tall as a 37 story building. Over 2.3 million blocks of stone were used, each averaging 2 1/2 tons. Some weigh 16 tons. Despite their size, they fit together with a tolerance that is less than half the width of a human hair.

Dynabyte builds its 16k dynamic RAM boards with the same exceptional precision and care. Their reliability is as solid as a rock.

Dynabyte's design meets rigid industrial grade standards. The design is so good, in fact, that one of the largest, most experienced electronics manufacturers has tried to imitate it. (We were flattered but not surprised; we know how good it is.)

More than 1400 microcomputer owners also know how good it is. Dynabyte's 16k dynamic is running in more systems than any other dynamic memory on the market.

We select the best components we can buy to build the 16k dynamic, because solid parts make a solid memory. Our memory-chips, for example, are factory prime from National Semiconductor.

Dynabyte was the first to deliver 16k dynamic RAM's assembled, tested and burned in. And at a price competitive with kits! Each board's complete function is confirmed by three stages of testing and a burn in cycle that runs 72 hours at 70°C (158°F).

When we build them that solid we can guarantee them for a full year.

If a Dynabyte board ever needs repair, we provide factory service with a 24 hour turnaround for both warranty and non-warranty work.

The Dynabyte 16k dynamic has the widest compatibility of any dynamic memory. So it will work in your system.

The Great Memory by Dynabyte is a solid buy. And an economical one. Effective October 1, the new Manufacturer's Suggested Price is reduced from $485 to $399.

Ask for the Great Memory by Dynabyte at your local computer store. If it isn't in stock, tell the owner that he missed another Dynabyte sale, and order direct. Telephone (415)494-7817. Cable DYNABYTE. Or mail to Dynabyte, Inc., 4020 Fabian, Palo Alto, CA 94303.

Specifications: 16,384 bytes, National Semiconductor MM5271 chips, S-100 compatible, 350 nsec. access time, 550 nsec. cycle time, transparent refresh, no wait states for 2 MHz 8080 processor, on board clock, 5 watts power consumption, 1 MHz direct memory access, 16k addressing, solder masked, assembled with sockets, tested, burned in, guaranteed one year.

Dynabyte
Builders of the Great Memory
was implemented by picking address allocations. (See table 2 for a detailed list of the allocations.) I decided early in the project that 16 K bytes of memory would be a good start for general programming uses. I had to allocate this volatile user oriented programmable memory, as well as all the addresses for peripheral hardware and "firmware" read only memory programs. The address range of the 6502 is from 0 to 65,535 (0000 to FFFF in hexadecimal). Since the architecture of the chip itself uses addresses 0000 to 01FF for dedicated functions which must be in programmable memory, I assigned the 16 K byte block of main memory to the lowest part of the addressing range, from hexadecimal 0000 to 3FFF. I was interested in the possibility of occasionally using the MOS Technology TIM monitor, so I reserved locations 7000 to 73FF for use by that program's read only memory. I allocated the control panel scratch memory and peripheral ports starting at address 8000 hexadecimal, with the addresses starting at 8020 reserved for general peripheral use as I expand the system. At the end of the address range, I reserved the 4096 bytes from addresses F000 to FFFF for read only memory containing various systems routines. The high end of this range is reserved for the control panel support program and the interrupt vectors of the MOS Technology 6502 design.

Backplane

The backplane of the card cage (see table 1) carries the address bus, the bidirectional data bus, six vectored interrupt lines, and other functional signals as detailed in table 1. All signals that pass through the backplane are interpreted to be logical 1 or "true" in a low voltage (TTL 0) state. A high voltage (TTL 1) state is interpreted as a logical 0 or "false" state. Each module which connects to the backplane uses TTL inverting buffer circuits for signals sent or received. The +5 V (VCC) and ground (GND) connections are arranged on the card edge connectors such that by plugging a module into the backplane upside down, polarity to the card will not be reversed. This simple arrangement eliminates the need for keying the cards; while it prevents physical destruction of the card due to inadvertent reversal of orientation, the system should not, of course, be expected to work with one or more cards reversed relative to the balance of the cards in the system.

The vectored interrupt lines of the backplane are defined by some logic implemented on the central processing unit card (see figures 3). This card contains logic necessary to cause hardware vectoring of interrupt levels to one of the six possible interrupt service routines. The vectoring

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flag Select Bits</td>
<td>Flag Control</td>
<td>Control Request Functions</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = CARRY flag</td>
<td>&quot;1:&quot; = set flag</td>
<td>0 = Null command (pass NMI)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = ZERO flag</td>
<td>&quot;0:&quot; = reset flag</td>
<td>1 = FLAG MODIFICATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 = IRQ DIS flag</td>
<td>2 = DEPOSIT NEXT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 = DECIMAL flag</td>
<td>3 = DEPOSIT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 = BRK CMD flag</td>
<td>4 = EXAMINE NEXT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 = Not used</td>
<td>5 = EXAMINE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 = OVRFLW flag</td>
<td>6 = STEP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 = NEG flag</td>
<td>7 = HALT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8 = REG LOAD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9 to 15 = Unused</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3: Control request word layout. The control request word, located at address 8010 in memory address space, is an input to the processor with this format. It is used by the front panel service program of listing 1 to govern the operation of the panel based on settings of various switches.
**4800 BAUD CASSETTE RECORDER**

An ASYNCHRONOUS NRZ type Recorder with remote motor start/stop. Error rate 10⁻⁸ at 4800 BAUD. Can be used from 110 to 4800 BAUD into a UART or "Bit Banger PIA" - no clocking required. This is not an audio recorder. It takes RS232 or TTL signals from the terminal or computer and gives back the same signals. No audio interface is used. Motor start/stop is manual or through TTL or RS232 signals.

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Recommended for DATA LOGGING, WORD PROCESSING, COMPUTER PROGRAM RELOADING and DATA STORAGE. Especially recommended for 6800 systems, 6502 systems, 1800 systems and beginners with the 8080 systems. Manual control except for motor start/stop. 6800 or 8080 software for file or record searching available on request with order. Used by major computer manufacturers, Bell Telephone and U.S. Government for program reloading and field servicing.

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Extra serial port is provided for your use with a second terminal or printer. (RS232, TTL or 20 ma)

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$190.00, Tested & Assmb. ($160.00, Kit)

PROVIDES MONITOR AND TAPE SOFTWARE in ROM TERMINAL and TAPE PORTS on SAME BOARD CONTROLS ONE or TWO TAPE UNITS (CC-8 or 3M3A)

This is a complete 8080, 8085, or Z80 system controller. It provides the terminal I/O (RS232, 20 mA, or TTL) and the data cartridge I/O, plus the motor controlling parallel I/O latches. Two kilobytes of on board ROM provide turn on and go control of your Altair or Imesi. NO MORE BOOTSTRAPPING. Loads and Dump's memory in hex on the terminal, formats tape cartridge files, has word processing and paper tape routines. Best of all, it has the search routines to locate files and records by means of six, five, and four letter strings. Just type in the file name and the recorder and software do the rest. Can be used in the BISync (IBM), Biphase (Phase encoded) or NRZ modes with suitable recorders and interfaces.

This is Revision 7 of this controller. This version features 2708 type EPROM's so that you can write your own software or relocate it as desired. 2708 preprogrammed is supplied with the board. A socket is available for the second ROM allowing up to a full 2K of monitor programs.

Fits all S100 bus computers using 8080 or 280 MPU's. Requires 2 MHz clock from bus. Cannot be used with audio cassettes without an interface. Cassette or 2510 cartridge inputs are RS232 level.

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$190.00 ($160.00 Kit)

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is accomplished by using the selected service routine address for the interrupt vector requested by the 6502 processor during its interrupt sequence. The service routines are assumed to reside in programmable read only memory chips located in a separate module elsewhere on the backplane bus. The processor hardware also incorporates a priority arrangement of these six interrupts. Thus when two interrupts occur simultaneously the system has no problem: the higher priority one is serviced first. This becomes important when several interrupt driven peripherals are used with the system. An automatic reset function initializes the system when power is turned on, a separate interrupt for the 6502 which is supported on the processor board.

As an alternative to the front panel logic, the memory map of table 2 shows allocations for the MOS Technology TIM integrated circuit, MCS6530-004. This “Terminal Interface Monitor” allows the user to use an ASCII serial device such as a Teletype or other terminal. In making a board to support TIM, I also included an 8 bit parallel interface to allow the possibility of using a high speed paper tape reader with Kompuuutar. Details of the TIM module are shown in figures 4.

Front Panel Logic

Getting into more of the details of the system, I’ll concentrate mainly on the place where I started my design, the front panel. The front panel logic is composed of input devices, output devices, 16 bytes of scratch pad memory, logic of the ready and nonmaskable interrupt timing, address decoders, switch debouncers, a data bus multiplexer, command encoder, line buffers and the control program in a programmable read only memory. The overall design of the front panel is found in figure 1, with details spread out in figures 1.1 thru 1.9. Photos 1 and 2 give further details.

There are four input sources of data in the front panel design. Each source is selected by the address decoding logic, which in turn allows the proper source to be input through the data bus multiplexer. The first source of input is the control request register. This source carries data from the command encoder, the flag selection switch, the flag modification switch and the register load switch. Table 3 shows the bit assignments of this source, which is located at hexadecimal address 8010 in memory address space.

The second source of input is the low

<table>
<thead>
<tr>
<th>Wire</th>
<th>Logic Diagram Mnemonic</th>
<th>Description</th>
<th>Wire</th>
<th>Logic Diagram Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 to 4</td>
<td>+5 V</td>
<td>voltage source</td>
<td>21</td>
<td>X800X</td>
<td>address selection</td>
</tr>
<tr>
<td>5</td>
<td>D0</td>
<td>data bus lines</td>
<td>22</td>
<td>X800F</td>
<td>lines</td>
</tr>
<tr>
<td>6</td>
<td>D1</td>
<td></td>
<td>23</td>
<td>X8013</td>
<td>multiplexer select</td>
</tr>
<tr>
<td>7</td>
<td>D2</td>
<td>phase 1 clock</td>
<td>24</td>
<td>X8014</td>
<td>lines</td>
</tr>
<tr>
<td>8</td>
<td>D3</td>
<td>phase 2 clock</td>
<td>25</td>
<td>SEL 1</td>
<td>multiplexer disable</td>
</tr>
<tr>
<td>9</td>
<td>H1 CK</td>
<td>any interrupt pending</td>
<td>26</td>
<td>SEL 2</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>H2 CK</td>
<td>address bus line</td>
<td>27</td>
<td>BSOUT</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>IRQX</td>
<td>data bus lines</td>
<td>28</td>
<td>-op</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>A3</td>
<td>address bus line</td>
<td>29</td>
<td>X8015</td>
<td>address selection</td>
</tr>
<tr>
<td>13</td>
<td>D4</td>
<td></td>
<td>30</td>
<td>XFEEA</td>
<td>lines</td>
</tr>
<tr>
<td>14</td>
<td>D5</td>
<td></td>
<td>31</td>
<td>X801F</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>D6</td>
<td></td>
<td>32</td>
<td>-op</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>D7</td>
<td></td>
<td>33</td>
<td>-op</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>A2</td>
<td></td>
<td>34</td>
<td>REST</td>
<td>front panel reset</td>
</tr>
<tr>
<td>18</td>
<td>A1</td>
<td></td>
<td>35</td>
<td>RDY</td>
<td>ready</td>
</tr>
<tr>
<td>19</td>
<td>A0</td>
<td></td>
<td>36</td>
<td>NMI</td>
<td>nonmaskable interrupt</td>
</tr>
<tr>
<td>20</td>
<td>R/W</td>
<td>read/write</td>
<td>37 to 40</td>
<td>GND</td>
<td>ground</td>
</tr>
</tbody>
</table>

Table 4: Wiring list for the J2-P2 cable. This cable runs from the front panel interface board in the card cage to the front panel assembly, as seen in photos 2 and 3. In the author’s version of Kompuuutar, the wiring was direct without use of a plug and jack; in order to simplify nomenclature in presenting the article, we’ve used a numerical identification of signal paths as if a 40 wire cable and connectors had been used...CH/
Specialization is the only way of doing a job well. S-100, Inc. is committed strictly to the needs of S-100 based minicomputer systems. We don’t sell books, Teletypes, video terminals, or products that do not directly plug into an S-100 bus.

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<thead>
<tr>
<th>Item Description</th>
<th>OUR PRICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMSAI 22-SLOT MOTHERBOARD, KIT</td>
<td>$ 589.95</td>
</tr>
<tr>
<td>Z-80 CPU BOARDS</td>
<td></td>
</tr>
<tr>
<td>Our Kit</td>
<td>144.95</td>
</tr>
<tr>
<td>Digital Innovations (Similar to TDL)</td>
<td>149.95</td>
</tr>
<tr>
<td>TDL ZPU</td>
<td>239.95</td>
</tr>
<tr>
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<td>1,495.00</td>
</tr>
<tr>
<td>4K S-100 MEMORY BOARD, low-power, 450ns</td>
<td>89.95</td>
</tr>
<tr>
<td>8K S-100 MEMORY BOARD, low-power 450ns</td>
<td>144.95</td>
</tr>
<tr>
<td>16K S-100 STATIC MEMORY BOARD</td>
<td>439.95</td>
</tr>
<tr>
<td>16K S-100 DYNAMIC MEMORY BOARD (assembled and tested)</td>
<td>299.95</td>
</tr>
<tr>
<td>CYBERCOM VIDEO BOARD VB1A</td>
<td>149.95</td>
</tr>
<tr>
<td>NORTH STAR MICRO DISK, Kit</td>
<td>594.95</td>
</tr>
</tbody>
</table>

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Figure 1. Block diagram of Komputer's front panel logic. The Komputer design uses a read-only memory program to manipulate the contents of memory interactively, using function switch inputs and front panel display outputs. This diagram serves as a functional road map to the various components of the display and its interface board.

KEY

- SYSTEM DATA BUS (BACKPLANE)
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A new high in S100 bus memory cost effectiveness. Fully assembled (with sockets), tested, burned-in and guaranteed. 4Kx1 dynamic memory chips (the same ones used by the ton in IBM compatible memory systems) combined with self contained control logic, yield a memory system with these features:

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- No waiting. In fact, XRDY is not even connected to the memory.
- Full DMA capability.
- Reliable, low level clock and control signals.
- Three full days testing at 70° C (185° F).

**SPECIFICATIONS**

**Capacity:** 16384 bytes
**Addressing:** 16K boundaries
**Bus structure:** S100 - Plug compatible with IMSAI 8080, POLY 88, ALTAIR 8800, BYTE-8, SOL
**Address and Data Buffering:** <200 uA, special high impedance buffers - less than one low power Schottky load
**Access time:** 350 nSec
**Memory chips:** MM 5271 (National Semiconductor and others) 4K dynamic

**Dynabyte Inc.**

4020 Fabian Way, Palo Alto Ca. 94303

for more information call or write to:

**R.H.S. MARKETING**
2233 El Camino Real
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Figure 1.1: Switch debouncing logic. This is a detail logic diagram suitable for construction of Kompuaar. As in all the logic of this design, all resistors are 1/4 W unless otherwise noted, and standard TTL integrated circuits are used for miscellaneous functions. Debouncing is done with set-reset flip flops contained in the 74279 part, which we have noted in the discrete logic form internal to dotted lines. The flip flops can be wired out of gates (7400, 7410) if desired, should the 74279 be unavailable in the builder's parts bin. Integrated circuit power wiring for the entire design is summarized by IC number in table 5.
Introducing:

**MSDD-100**

Floppy Disc System software:

The user is provided with two diskettes. One is dedicated solely for data and the other for programs. The system supports two disk drives and cassette I/O. In addition, the user can format and load programs on the disc. The Basic system is quite flexible, supporting three disk drives and cassette I/O. In addition, number matrices may be saved and loaded as named files (versions 4.0 and later only). The link also supports sector level 0/1 I/O.

The MSDD-100 Floppy Disc System represents a significant advancement in low cost, high density mass storage systems. Utilizing the industry standard Shugart SA400迷你floppy™ drive and a highly reliable LSI controller, the single card MSDD-100 Floppy Disc System represents a major cost/performance breakthrough for the hobbyist and businessman.

Many features not provided on the larger disc systems are standard on the MSDD-100 Disc system. The controller will support up to three drives. The controller provides all disc timing functions, therefore no software timing loops are required. The controller also supports three modes of programmed I/O (no DMA). First, there is simple command I/O. Second, there is a standard interrupt with all command completion and data request conditions interrupting to Restart 7. Third, the controller has the switch selectable facility to vector the processor to any of the Restart locations upon generation of an interrupt. This allows data requests and command completion interrupts to be vectored separately. This type of interrupt structure is ideal for multi-user / multi-tasking applications.

The controller design is totally synchronous, requiring no "one shots". Ease of maintenance is evidenced by the fact that there are no adjustments required for operation. The controller is a single board design, with very low power consumption.

**Introducing:**

**MSDV-100**

Video Display Systems:

The Video Display System is a high quality 80 character, 24 line video output device for the S-100 bus. Many advanced features have been incorporated which are normally not found on units costing many times the price.

The character set includes upper and lower case characters as well as full punctuation. Any character can be underlined, a feature useful in work processing. A character can also be made to blink at a user-selectable rate, often used for alarm or warning situations. Additionally, a character can be made to appear brighter than normal or to appear in a reverse field (black on white), useful in order entry or other applications to highlight text.

Also included in the MSDV-100 is the ability to generate high quality forms overlays. Margins can be either single or double wide with continuous intersections. Charts, graphs, or order entry forms are easy to produce on the video screen.

A third significant feature of the MSDV-100 Video Display System is the ability to display continuous grey scale elements in any of nine levels in any of 1920 positions on the screen. This is especially useful for bar graphs and for grey scale graphics or animations, as well as in forms applications.

Though these capabilities are standard and provided with every unit, MSD has the capability to generate and deliver MSDV-100 Video Systems with custom character sets as defined by the user. This could include mathematical symbols, APL characters, or Boolean logic symbols to name a few.

Internally, the MSDV-100 is a two board S-100 based system which occupies 2K of RAM address space and two Input/Output ports. A bus device, the microcomputer can write to the screen as fast as it can to any memory. For diagnostic purposes, a memory test can be performed on the screen.

Software support for the MSDV-100 is complete with both machine language code, including fully commented source listings, and a comprehensive Basic software package implementing all MSDV-100 features.

The assembly language drivers allow the sophisticated user to easily customize the system for specialized applications.

Programs are provided that permit the user to link the video system to high level programming languages such as Basic. A link program, provided in Basic, permits the user without knowledge of assembly language programming to immediately obtain video output from that software. The link fully implements the forms capability of the MSDV-100, provides direct cursor addressing, and is fully upwards compatible with the LSI ADM-3A video terminal.

---

**Introducing:**

**MSDD-100**

Floppy Disc System specifications:

- Drive: 89,600 byte maximum data capacity (formatted)
- 35 tracks
- Variable format: 128 - 1024 bytes / record
- User Definable format: 16 - 2560 bytes / record
- Track to track step time: 40 milliseconds
- Average access time: 600 milliseconds (Random read/write)
- Latency: 200 milliseconds
- Power requirement: +12 V regulated . 5A typ. 1.1A max. 1.8 A surge. +5V regulated . 5A typ.

**Controller commands:**

- Read/Write record, Seek, Step in/Step out, Read track, Write track (format), Read ID field, Force interrupt (conditional or immediate)
- Interfacing:
  - Controller to drive: 34 conductor ribbon cable (provided)
  - Interrupts: standard, internal vectors (switch selectable) or external vectors
  - I/O: Programmed byte Input and Output
  - Addressing: User selectable port definitions, occupies six contiguous ports addresses
  - Controller power requirements:
    - +8 Volts unregulated, 200 milliamperes maximum
    - +15 Volts unregulated, 20 milliamperes maximum
    - -15 Volts unregulated, 10 milliamperes maximum

**MSDV-100**

Video Display System specifications:

- Character Set: 80 characters, 24 lines
- Resolution: 80 characters x 24 lines
- Color: Monochrome
- Interface: S-100 bus
- Power: 12 V regulated
- Form Support: 24 lines x 80 characters
- Screen Size: 8x8

---

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- Video Display System .......... $999
- Additional Drivers .............. $850 ea.
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Figure 1.2: Flag selection switch. The control panel service program of Kompuutar uses the binary encoded 3 bit value on the output of this switch to determine which processor flag is to be set or reset using an appropriate function selection. This switch is a rotary switch which has three poles and eight positions.

![Diagram of flag selection switch]

Figure 7.2: Flag selection switch. The control panel service program of Kompuutar uses the binary encoded 3 bit value on the output of this switch to determine which processor flag is to be set or reset using an appropriate function selection. This switch is a rotary switch which has three poles and eight positions.

Figure 1.4: Display data selection switch. The control panel service program uses the binary encoded 4 bit value on the output of five possible words for default display from the control panel scratch pad located at addresses 8000 to 800F. The five addresses selected are for the accumulator (0), X index (1), Y index (2), stack register (5) or data register (D).

![Diagram of display data selection switch]

Figure 1.4: Display data selection switch. The control panel service program uses the binary encoded 4 bit value on the output of five possible words for default display from the control panel scratch pad located at addresses 8000 to 800F. The five addresses selected are for the accumulator (0), X index (1), Y index (2), stack register (5) or data register (D).

![Diagram of display data selection switch]

Figure 1.3: Front panel data entry switches. The entry of static data is accomplished by 16 toggle switches. These switches are connected to either logical 1 (+5 V through a 1 K resistor) or logical 0 (ground).

![Diagram of front panel data entry switches]
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Figure 1.5: Control logic for front panel functions. This logic generates the function request code (read from address 8010 bits 0 to 2), and controls the NM line of the 6502 to implement single step execution of the processor.

Figure 1.6: Data source multiplexer and bus interface. The sources of data read from the front panel logic are four: the two 8 bit data entry switch registers of figure 1.3, the 8 bit control request word from figure 1.5, and the output of the scratch pad programmable memory (lines labeled "RAM") from figure 1.7. These are selected by a 2 bit addressing code generated on the front panel interface board of figures 2.
Text continued from page 102

Order byte of the data entry switches. The eight toggle switches of this switch register are used to enter a byte into the data bus or into the least significant byte of the address register which is maintained by the control panel program in its scratch pad. These toggle switches are located at address 8011 in memory address space.

The third source of data for the control panel program is the set of toggle switches which define the most significant byte of an address. These eight switches are located at address 8012, and are only used for address inputs.

The last source of data is the output of the 16 byte scratch pad memory in the control panel. The scratch pad responds to addresses 8000 thru 800F.

The address decoding logic is found in figure 2.1. The outputs of this decoding logic include miscellaneous individual address selections, plus the selection signals which are used to control the data input multiplexer found in figure 1.6. The selection signals are generated by the priority encoder IC35, and are used to pick one of the four sources for routing to the bus interface gates IC73 and IC74. These gates connect to the backplane data bus from the front panel via P2's connecting cable between the front panel and the front panel interface board.

The front panel also includes several possible outputs for data. In addition to the input possible from the scratch pad, the processor can address and write data to the scratch pad in any one of the locations 8000 to 800F. The actual contents of the data in the scratch pad can be displayed for addresses 8000, 8001, 8002, 8003, and 800D by moving the rotary switch S24. This switch (see figure 1.4)

Text continued on page 116
Microtech, Incorporated continues to provide a number of sophisticated software packages for microcomputer users. Our software is created expressly for microprocessors, making it fast and memory-efficient. Our higher level language, MICROTECH BASIC, provides features never before offered for microcomputers, and our applications and documentation allow even first-time users to be up-and-running quickly and effortlessly.

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- Complete String Variable Package
- Table Driven Variable Storage — reduced memory overhead for variable storage.
- Mass Storage Data File Handling — allows data to be read or written to mass storage devices either sequentially or randomly.
- Mass Storage Program File Handling — a full directory based program file capability has been implemented. Commands available include PGRM (used to create a directory entry), SAVE, ERASE, LOAD, and RUN (load and go).
- Complete Program Overlay Capability — a powerful programming technique that allows an executing program to load and execute any other program currently in the directory with all variable values passed to the new program.

MICROTECH BASIC is currently available in audio cassette form for Digital Group Z-80 systems. We have hooked MICROTECH BASIC to our own Phi-Deck driver software to create TOS (Tape Operating System) BASIC. Up to four Phi-Decks may be used for mass data and program storage. All tape control is provided through BASIC commands. This package, with all audio, video, and mass storage drivers, requires roughly 9.5 K. A minimum 18 K system is recommended.

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TOS BASIC (for Digital Group Systems) — includes BASIC (with Floating Point), data tape formatting routine, and deck-to-deck copying routine — 28 page user’s manual and free updating service .................................................. $64.95
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Figure 1.8: Displays. The front panel displays are detailed here: (a) is the output latch used to drive LED indicators for the eight flag bits, located at hexadecimal address 8013. At (b) are the four digits of hexadecimal address lamp display, addressed at locations 8014 and 8015. These displays incorporate latching logic as well as the needed decoding of 4 bit hexadecimal patterns into an array of LED dots. And at (c) are two miscellaneous indicators for the front panel.
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defines an address value which is presented to the 7489 scratch pad memories IC61 and IC63 by 74157 multiplexer IC62 when the scratch pads are not being referenced by the processor. Since the control panel program references the scratch pad only occasionally, the normal state is an address selected by S24 determining which of the five scratch pad locations is seen in the display lamps for scratch pad data. Thus the scratch pad memory has several potentially visible bytes of memory address space and acts as an output device.

A second output device is an 8 bit data latch whose outputs activate eight discrete LED devices. This device, located at address 8013 in memory address space, is used to display the processor's status register bits. The front panel control program is responsible for maintaining current information in this display (as is the case with all the display outputs).

Address display information is latched into four digits of hexadecimal display provided by Hewlett-Packard HP5082-7340 parts, IC65, IC66, IC67 and IC68 in figure 1.8b. Each of these displays has a built-in 4 bit data latch which retains information defined by writing to the memory locations 8014 (low order) and 8015 (high order).

Two miscellaneous indicators are also included in the design. These single bit LED displays are connected to the processor's ready (RDY) and main interrupt (IRQ) lines. The RUN indicator lights

---

Figure 1.9: Front panel mechanical layout. This is a detail drawing to scale of the physical layout of the front panel as seen in the photographs, along with the front panel electronics board which is mounted on standoffs behind the panel.

NOTES:

1. All ICs except locations E1 and E2 are Texas Instruments SN74XXX series TTL logic. E1 and E2 are three-state bidirectional bus drivers made by National.
2. Switches S1 thru S6 are Alco model MTF-206SA.
3. Switches S8 thru S23 are Alco model MTF-106D.
4. Switch S7 is a Centralab model PA-2009 rotary.
5. Switch S24 is a Centralab model PA-2011 rotary.
6. RD, ID, DDO to 007 and SDO to SD7 are discrete LED displays. HP model 5082-488D.
7. X1-X4 are dot matrix hexadecimal LED displays. HP model 5082-7340.
8. All pull up resistors shown on schematics in conjunction with front panel switches are mounted on those switches.
FUNCTION: Assembles programs written in symbolic language for an 8080 CPU on an 8080 based system.

HARDWARE REQUIRED: 8080 computer with minimum of 4K memory (of which at least 1K should be RAM); a source listing input device; an object code output device.

OPTIONAL HARDWARE: A system console device such as a keyboard/CRT or keyboard/printer will allow convenient control of the program using executive commands; additional memory beyond 4K will allow expanded symbol table length, or capability to assemble directly into memory.

SOFTWARE REQUIRED: User provided I/O driver routines for whatever I/O devices will be utilized. Each I/O device is linked to the program by a single vector for ease in adapting the program to individual systems.

MEMORY UTILIZED: The assembled listing provided in the manual resides in pages 01 through 0A (hexadecimal 001 through 012 octal). Pages 00, part of 0A, all of 0B and 0C (hexadecimal 000, part of 012, 013 and 014 octal) are left available for user provided I/O routines. Pages 0D (hexadecimal 015 octal) are used for symbol table storage (or as direct assembly areas in systems with sufficient memory).

MNEMONICS UTILIZED: This program is written in, and accepts for assembly purposes, standard industry accepted mnemonics for the 8080 CPU (such as MOV A,B; INX H: CALL; etc.) [Note: SCELBI is discontinuing its use of special 8080 compatible mnemonics which have characterized its 8080 programs in the past.]

PUSEDO-OPERATORS: Accepts the ORG (originate), END (stop assembly), SET (define a name), DB (data byte), DS (data string) and DW (data word or double byte) pseudo-operators.

PROGRAM OPERATION: The program processes a source listing in two passes to produce assembled object code. An optional third pass allows an assembled listing to be obtained. Listings may be obtained in hexadecimal or octal format. The program will also display the contents of the symbol table at the operators request. The program can process source listings as single or multiple files. Program operation may be controlled from a console device using executive commands or through computer panel switches by jumping to appropriate locations within the program.

SOURCE FORMAT: Convenient, easy to use, variable length fields permitted. Labels may be 1 to 6 characters in length, accepts both hexadecimal and octal numbers with or without leading zeros, has "literal" capability (can accept ASCII characters directly as data), allows use of letters of numbers as CPU register operands.

DOCUMENTATION: Thorough in the SCELBI tradition! The program manual describes the operation of the assembler, presents detailed discussions of all major routines, and contains two completely assembled listings (one provided in hexadecimal and one in octal notation). Of course it includes operating instructions and even provides a routine that may be used for loading programs produced by the assembler.

SPECIAL FEATURES: Because the program has been carefully organized and written with all memory references assigned labels, it may be readily reassembled to reside in any general area in memory. It may even be reassembled to reside in ROM provided that some RAM area is available for scratch pad and symbol table use!

OPTIONS: A punched paper tape of the object code for this assembler (as described in the documentation) is available. The object code tape is provided in the widely accepted "hexadecimal format." Also, the complete, commented source listing of the program as presented in the documentation is available in straight ASCII format on punched paper tape. Fan-fold paper tapes are provided for ease in handling. Additionally, opaque paper tape is supplied to facilitate the use of low cost optical paper tape readers now in widespread use. NOTE: Paper tapes are sold only as optional supplements to the documentation.

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SCELB 8080 Standard Assembler: $19.95 Optional object code on punched paper tape; specify 8080SA-OPT: $10.00 Optional commented source listing on punched paper tape, specify 8080SA-SPT: $39.00.

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Note: X followed by a 4 digit hexadecimal number indicates an address selection line. Additional Xs indicate "don't care" hexadecimal digits. O followed by a 4 digit octal number (outputs of 74138s) with Xs for "don't care" indicates a low order 12 bit address decode.
up when the machine is in the run mode, and the interrupt indicator remains lit while an interrupt is pending. Interrupt control logic is contained in the devices requesting an interrupt, with the processor’s priority encoder defining the backplane signal IRQX (backplane pin 12) which indicates that some interrupt is pending (and also signals the processor through its IRQ input, pin 4.) Thus when interrupt driven IO is used, the interrupt indicator lamp will flicker if appreciable interrupt processing wait states occur as various devices request attention.

Other Front Panel Functions

The front panel logic includes logic of the ready (RDY) and nonmaskable interrupt (NMI) timing, shown in detail in figure 1.5. These lines are used to generate signals which affect the processor in a manner very similar to interrupts. The HALT and single STEP switch are used to generate signals for these lines. This timing logic causes the 6502 processor and its control program to implement fairly conventional single stepping and program half or restart functions. HALT or STEP switches are used to cause the processor to execute one more instruction. Any other switch activated on the front panel causes this logic to allow the processor to complete only its present instruction. The hardware protocol of this logic locks out all front panel functions when the processor is running, except for the HALT switch.

The front panel’s interface to human fingers are through various function switches. These switches are debounced using set-reset flip-flops which come four to a package in the 74279 part. The debouncing logic guarantees that only one pulse is received for each activation of a switch.

Getting Kompuutar Into Operation

The operation of the front panel’s control logic with respect to the actual processor

Figure 2.1: Front panel interface module address decode logic. This logic decodes the several addresses in the 8000 to 801F range which are used by the front panel design of Kompuutar. Since 3 bit decoders are used, octal intermediate terms are used to symbolize the outputs of the 74138s prior to logical sums performed by the 74260 OR gates. Outputs of the circuit are discrete select lines for several addresses, plus two source selection lines for the data bus input multiplexer of figure 1.6.

Figure 2.2: Buffering of processor control signals at the front panel interface module.
You Asked For It!

You asked for the Intel 8080A CPU .................................................. We gave you the VECTOR 1
You asked for a real-time clock .......................................................... We gave you the VECTOR 1
You asked for eight level vectored priority interrupts ......................... We gave you the VECTOR 1
You asked for a jump-on-reset and resident monitor ......................... We gave you the VECTOR 1
You asked for the S-100 bus ............................................................... We gave you the VECTOR 1
You asked for an 18 slot fully shielded motherboard ......................... We gave you the VECTOR 1
You asked for a rugged, reliable chassis .......................................... We gave you the VECTOR 1

Then . . . You asked for the compactness and convenience of installing your mini-floppy disk directly in the front panel. .......... NOW . . . We give you the VECTOR 1+
can be illustrated by walking verbally through a typical sequence of operations. First, let's assume that the machine is in RUN mode, which is indicated by a low level on the output of the execution state flip flop, IC49b pin 9. This is the normal situation for a fully executing 6502 program contained in the system's main program memory region. Next, press the front panel's HALT switch, S1. Upon release of the HALT switch the debounce logic completes one HALT pulse which is processed by the command encoding logic of figure 1.5. When the HALT line makes

Text continued on page 128

---

Figure 2.3: Pull up resistors for backplane address lines, and inverting receivers for local use in the front panel interface.
• ANY NUMBER OF FILES MAY BE OPEN (IN USE) AT ONE TIME
• THE NUMBER OF FILES AND SIZE OF FILES IS LIMITED ONLY BY THE SIZE OF THE DISC
• MERGING FILES REQUIRES NO EXTRA DISC SPACE
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Our Basic Floppy Disc System (BFD-6S) must modestly be called superb. It comes completely assembled with a disc controller that is plug compatible with the SWTPC 6800. In fact all our products use the 6800 standard SS-50 (Smoke Signal 50) bus used by SWTPC. The cabinet and power supply are capable of handling up to 3 Shugart Mini-Floppy Drives. One drive is included in the price of the BFD-6S and others may be added easily at any time. Or you may save money by ordering the dual-drive BFD-6S-2 or triple drive BFD-6S-3 (picted). Price: BFD-6S $795, BFD-6S-2 $1139, BFD-6S-3 $1479, SA-400 Drive $360.

The BFD-6S includes our Disc Operating System Software. Our software provides for a soft-sector disc format consisting of 128 bytes per sector, 18 sectors per track and 35 tracks per disc. The software provides direct commands to name and rename files, transfer memory to disc and disc to memory and to automatically jump to the starting location of any program loaded from disc to memory. The direct command names are: RUN, GET, GETHEX, CLOSE, SAVE, DELETE, APPEND, RENAME, COPY, LIST, FIND, LINK, and PRINT. In addition, the Disc File Management subroutines are available to create files under your program control.

A bootstrap PROM is included on the controller board to initiate the Disc Operating System which loads into a 4K memory board located at 7000 or optionally at 0000. Thus, you can be up and running from a cold start in just a few seconds.

SUPER SOFTWARE

Free patches are provided for SWTPC BASIC version 2.0 and Co-Resident Editor/Assembler. These patches allow the SAVE and LOAD commands to work with the disc or the cassette at your option. SUPER EDITOR: Smoke Signal Broadcasting now has its own editor. It is a content oriented editor with string search and block move capability. Changes may be made by referring either to line number or string content or a combination of references. Naturally, it is designed for file transfer to and from the BFD-6S. Price: SE-1 $29 on diskette or cassette.

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NEED A FULL SIZE FLOPPY? Our P-38-FF is a plug-in interface card to the ICOM Frugal Floppy™. It includes all the features of the P-38-I plus one 2708 EPROM containing the ICOM bootstrap software. Just plug the P-38-FF into your SWTPC 6800 and your ICOM into the P-38-FF and you're ready to use the Frugal Floppy and ICOM's 6800 software package. Price $299.

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BANKAMERICARD, VISA AND MASTER CHARGE WELCOME.
FROM FIGURE 23

IC CONNECTIONS FOR CUSTOM PROM 512X8

FROM FIGURE 23

IC 36 b

IC 36 a

IC 39 a

IC 39 b

74260

7400

XFE7C

XFE7F

FROM BACKPLANE

TO FRONT PANEL

BF-AM

FP-AM

BP-AM

BP-AM5

BP-AM6

BP-AM8

IC 32 b

IC 33 b

IC 34 b

IC 35 a

IC 36 a

IC 37 a

IC 38 a

IC 39 a

IC 40 a

FIGURE 2.4: A continuation of the front panel interface module address decode logic. This is a 512 by 8 bit fusible link program code module that only memory module with decoding logic and responds to addresses F000 thru FFFF in memory address space. This PROM contains the front panel monitor program of listing 1 in the figure. Output is directly to the data bus which is also connected to the back panel and to the front panel assembly.
24 Channel LOGIC ANALYZER, complete with 2 cards and 3 sets of probes (only one set shown).

Features
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Designed to plug easily into your S-100 Bus, the DATALYZER is a complete system — for only $495. Display of disassembled program flow is a standard feature, not an extra. And the low price includes 30 logic probes, so you can hook up immediately, without additional expense.

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☐ Assembled and Tested (manual included) $595.00
☐ Operators’ manual only $7.50
Delivery of all items in four weeks to:
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Address
City State Zip
Telephone
Payment Enclosed: ☐ Check ☐ Money Order
☐ BankAmericard ☐ Master Charge Exp. Date
Number
Signature
Figure 2.5: Mechanical layout of the front panel interface module. This board is built on a standard Vector Electronic Co prototyping card, and plugs into the 44 pin backplane connector (two sides with 22 pins each).

Figure 3.1: Processor module diagram. The 6502 processor module contains the 6502, its data bus and address bus buffering logic, and logic of the priority interrupt structure which substitutes one of six interrupt vector addresses on the low order address lines based on the priority of an interrupt. This overrides the processor generated address of FF00 or FFFF for an interrupt via the IRQ input. IRQ interrupt vectors are located at addresses FF49 to FFFH in memory address space, with six priority levels. Note that the BRK instruction maps to vector FF00 (see listing I).
Text continued from page 122
its rising transition at the end of the pulse, the state of the execution state flip flop changes, causing the halt mode to be entered.

The logic which drives the RDY and NMI lines is responsible for assuring that the processor runs one extra instruction before dropping off into a halt. The process of going into a halt is accomplished through the nonmaskable interrupt. A halting of the user program really means return to the front panel control program through the NMI signal generated here, so that the front panel control program can use the register information stacked up during the interrupt to update the external displays.

After such a halt, the front panel address display shows the location of the next instruction which can be executed in the program just halted. By setting the data display

Text continued on page 134

---

Figure 3.2: Processor module mechanical layout. This map shows placement of the processor integrated circuits on a Vector prototyping card.
Peripheral Vision is a young, fast-moving company that's dedicated to selling reasonably priced peripherals for various manufacturers' CPU's.

So now, when you build your microcomputer system, you'll know where to look for all the peripherals that will make your system do what it's supposed to do.

Peripheral Vision may be young, but we have some old-fashioned ideas about how to run our business. We know there are serious incompatibilities among the various manufacturers' peripherals and CPU's. We want to get them together. And we want to bring significant new products to market—products consisting of everything from adaptation instructions/kits for hardware and software to major new designs.

Most important to our customers, Peripheral Vision is committed to helping you get along with your computer. We'll do all we can to make it easy.

Our first product is a real reflection of this philosophy. It's a full-size floppy disk for the Altair-Lmsai plug-in compatible S-100 BUS. And it's available for as low as $750.00.

Our floppy disk has many exciting features:

- 1 interface card supports 4 or more drives
- Stores over 300,000 bytes per floppy
- Bootstrap EPROM included—no more toggling or paper tape
- Completely S-100 plug-in compatible
- Drive is from Innovex (the originator of the floppy concept)—assembled and tested
- Disk operating system with file management system included on floppy
- Cabinet and power supply optional

Also in the works are many new products we'll be letting you know about soon, if you'd like to take a closer look. Like I/O cards, tape drives, an impact printer—all for the S-100 BUS—and we're designing peripherals for a lot of other CPU's too.

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Peripheral Vision Inc.
P.O.Box 6267 Denver, Colorado 80206 303.777.4292

Name ______________________________________
Address ____________________________________
City State Zip _______________________________
Figure 4.1: TIM interface module details. The MOS Technology TIM monitor program resides in a single MC6830 ROM and peripheral interface circuit. The TIM interface module allows Komputer to be used with any serial terminal.
NOW! Every Business Can Own One

A secretary, accountant, and financial advisor all rolled into one for less than $1.50 per hour. Sound too good to be true? Let the ADMINISTRATOR do it for you.

Our "General Ledger Program" is a complete comprehensive business system designed to keep all of your company's records without the need for updating from other programs and there is no need to keep monthly tear sheets to be added together for the end of the year reports as our system will provide you with year end account totals for cash, accural, hybrid and chart of accounts systems. This program generates over 30 major reports. Including: 941's, P/L's, Balance Sheets, and year end account totals for filing Federal Income Tax Schedule C's and/or 1120's plus a lease purchase plan and 24-hour field service in most areas. Hard to believe! For less than $250/month you can lease your very own, nothing else to purchase.

ADMINISTRATOR I includes a miniature micro computer; S-100 Buss, with over 65K of user RAM. No switches to set, Power-on operation, multiple I/O interfaces, line printer, Video Terminal, Double-Density Disk, Disk Extended Basic and applications Software diskettes complete with full documentation (includes General Ledger, Payroll, Word Processing, Medical A/R, A/P, Engineering, Statistics, more) includes "Help" and Tutorial Software.

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(301) 721-1148
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J4: Parallel Interface

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DO</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>D1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>D2</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>D3</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>D4</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>D5</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>ground</td>
</tr>
<tr>
<td>9</td>
<td>D6</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>D7</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>DRY</td>
<td>data ready</td>
</tr>
<tr>
<td>12</td>
<td>DAKN</td>
<td>data acknowledge</td>
</tr>
<tr>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>ground</td>
</tr>
</tbody>
</table>

*Jacks 2, 3 and 4 are standard IC wire wrap sockets. They are used as cable connectors by mating with special "Augat" plugs.

J2: RS-232 Interface

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RS-232 OUT</td>
<td>seal data standard (out)</td>
</tr>
<tr>
<td>3</td>
<td>+10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>4</td>
<td>-10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>5</td>
<td>RS-232 IN</td>
<td>seal data standard (in)</td>
</tr>
<tr>
<td>6</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>ground</td>
</tr>
<tr>
<td>8</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>RS-232 OUT</td>
<td>seal data standard (out)</td>
</tr>
<tr>
<td>10</td>
<td>+10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>11</td>
<td>-10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>12</td>
<td>RS-232 IN</td>
<td>seal data standard (in)</td>
</tr>
<tr>
<td>13</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>ground</td>
</tr>
</tbody>
</table>

J3: Teletype Interface

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>2</td>
<td>TTYOT</td>
<td>Teletype (out)</td>
</tr>
<tr>
<td>3</td>
<td>+10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>4</td>
<td>+10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>5</td>
<td>TTYIN</td>
<td>Teletype (in)</td>
</tr>
<tr>
<td>6</td>
<td>BIASIN</td>
<td>pull up voltage source</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>ground</td>
</tr>
<tr>
<td>8</td>
<td>-10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>9</td>
<td>TTYOT</td>
<td>Teletype (out)</td>
</tr>
<tr>
<td>10</td>
<td>+10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>11</td>
<td>-10 V</td>
<td>voltage source to peripherals</td>
</tr>
<tr>
<td>12</td>
<td>TTYIN</td>
<td>Teletype (in)</td>
</tr>
<tr>
<td>13</td>
<td>BIASIN</td>
<td>pull up voltage source</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>ground</td>
</tr>
</tbody>
</table>

Figure 4.2: TIM interface module mechanical layout. This shows the physical arrangement of the wire sockets used to implement the TIM terminal interface for Kompuutar.
Building a better computer wasn't easy. But we did it.

Introducing the MSI 6800 Computer System

When we set out to build the new MSI 6800 Computer System, we knew we had our work cut out for us. It had to be at least as good as the now famous MSI FD-8 Floppy Disk Memory System which is also pictured below. So, the first thing we did was analyze all the problems and drawbacks we had encountered with other 6800 systems, and then put our engineers to work on solutions. The objective: Build a better computer.

We started with power supply. We had big ideas, so we used a hefty 18 amp power supply. You can run full memory and several peripherals without the worry of running out of juice. We also put it in the front of the cabinet so it's out of the way.

The next step was the CPU Board. A separate baud rate generator with strappable clock outputs allows any combination of baud rates up to 9600. A separate strappable system clock is available and allows CPU speeds of up to 2 MHz. The new MSI monitor is MIKBUG software compatible, so you will never have a problem with programs. Additional PROM sockets are available for your own special routines and to expand the monitor. The CPU also contains a single step capability for debugging software.

When we got to the Mother Board, we really made progress. It has 14 slots to give you plenty of room to expand your system to full memory capability, and is compatible with SS-50 bus architecture. Heavy duty bus lines are low impedance, low noise, and provide trouble-free operation.

With all this power and potential, the interface had to be something special. So instead of an interface address in the middle of memory, we put it at the top . . . which gives you a full 56K of continuous memory. Interfaces are strappable so they may be placed at any address. An interface adapter board is compatible with all existing SS-50 circuit boards and interface cards. All MSI interface cards communicate with the rear panel via a short ribbon cable which terminates with a DB-25 connector. All baud rate selection and other strappable options are brought to the connector so they may be automatically selected by whatever plug is inserted into the appropriate interface connector. Straps may also be installed on the circuit board.

To complete the system, we used an MSI 8K Memory Board which employs low power 2102 RAM memory chips and is configured to allow battery back-up power capability. A DIP switch unit allows quick selection of a starting address of the board at any 8K increment of memory.

If you're one of those people who understands the technical stuff, by now you'll agree the MSI 6800 is a better computer. If you're one who does not understand it yet, you'll be more interested in what the system can do . . . play games, conduct research and educational projects, control lab instruments, business applications, or just about anything else you might dream up that a microcomputer can do. The point is . . . the MSI 6800 will do it better.

The MSI 6800 Computer System is available in either kit form or wired and tested. Either way, you get a cabinet, power supply, CPU board, Mother board, Interface board, Memory board, documentation, instructions, schematics, and a programming manual. Everything you need.

There is more to say about the MSI 6800 than space permits. We suggest you send for more information which includes our free catalog of microcomputer products.

Building a better computer was not easy. Becoming the number one seller will be.

Midwest Scientific Instruments

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TWX 910 749 6403 (MSI OLAT) • Telex 42525 (MSI A OLAT)

NAME ____________________________
ADDRESS ____________________________
CITY __________________ STATE _____ ZIP ______

011177

Circle 92 on inquiry card.
Text continued from page 128

selection switch to point to the DATA position, the contents of memory at this location are displayed, having been transferred to the front panel scratch pad location 800D by the service program during the halt operation. At other positions of the switch, it is possible to view copies of the X register, Y register, accumulator A or the stack pointer register. The current contents of the processor status register are shown in the eight discrete LED outputs at location 8013 in memory address space.

If it is desired to modify a status flag, the flag select switch can be rotated to the desired bit, and the flag set or flag reset function be used to alter the flag state. If desired, memory can be examined or altered using the deposit, deposit next, examine or examine next routines activated by appropriate panel switches. Pressing RUN con-

Text continued on page 137

<table>
<thead>
<tr>
<th>IC Type</th>
<th>+5 V</th>
<th>GND</th>
<th>Map Location in Figure 1.9</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MSC6502</td>
<td>8</td>
<td>1.21</td>
<td>A3, 4, 5</td>
</tr>
<tr>
<td>2 74121</td>
<td>14</td>
<td>7</td>
<td>B7</td>
</tr>
<tr>
<td>3 7402</td>
<td>14</td>
<td>7</td>
<td>C7</td>
</tr>
<tr>
<td>4 7414</td>
<td>14</td>
<td>7</td>
<td>C6</td>
</tr>
<tr>
<td>5 DM8835</td>
<td>16</td>
<td>8</td>
<td>C5</td>
</tr>
<tr>
<td>6 DM8835</td>
<td>16</td>
<td>8</td>
<td>C4</td>
</tr>
<tr>
<td>7 7404</td>
<td>14</td>
<td>7</td>
<td>C1</td>
</tr>
<tr>
<td>8 7416</td>
<td>14</td>
<td>7</td>
<td>D6</td>
</tr>
<tr>
<td>9 74148</td>
<td>16</td>
<td>8</td>
<td>D4</td>
</tr>
<tr>
<td>10 7416</td>
<td>14</td>
<td>7</td>
<td>B2</td>
</tr>
<tr>
<td>11 74260</td>
<td>14</td>
<td>7</td>
<td>C3</td>
</tr>
<tr>
<td>12 7416</td>
<td>14</td>
<td>7</td>
<td>B1</td>
</tr>
<tr>
<td>13 74260</td>
<td>14</td>
<td>7</td>
<td>C2</td>
</tr>
<tr>
<td>14 7410</td>
<td>14</td>
<td>7</td>
<td>D3</td>
</tr>
<tr>
<td>15 74157</td>
<td>16</td>
<td>8</td>
<td>D2</td>
</tr>
<tr>
<td>16 7417</td>
<td>14</td>
<td>7</td>
<td>E2</td>
</tr>
<tr>
<td>17 7404</td>
<td>14</td>
<td>7</td>
<td>B5</td>
</tr>
<tr>
<td>18 Intel3624-4</td>
<td>22, 24</td>
<td>12</td>
<td>A2</td>
</tr>
<tr>
<td>19 7414</td>
<td>14</td>
<td>7</td>
<td>D2</td>
</tr>
<tr>
<td>20 7414</td>
<td>14</td>
<td>7</td>
<td>D4</td>
</tr>
<tr>
<td>21 7438</td>
<td>14</td>
<td>7</td>
<td>D6</td>
</tr>
<tr>
<td>22 7414</td>
<td>14</td>
<td>7</td>
<td>C6</td>
</tr>
<tr>
<td>23 7404</td>
<td>14</td>
<td>7</td>
<td>A4</td>
</tr>
<tr>
<td>24 7420</td>
<td>14</td>
<td>7</td>
<td>C5</td>
</tr>
<tr>
<td>25 74138</td>
<td>16</td>
<td>8</td>
<td>C1</td>
</tr>
<tr>
<td>26 74138</td>
<td>16</td>
<td>8</td>
<td>C2</td>
</tr>
<tr>
<td>27 74138</td>
<td>16</td>
<td>8</td>
<td>C3</td>
</tr>
<tr>
<td>28 74138</td>
<td>16</td>
<td>8</td>
<td>C4</td>
</tr>
<tr>
<td>29 74260</td>
<td>16</td>
<td>7</td>
<td>B2</td>
</tr>
<tr>
<td>30 74260</td>
<td>14</td>
<td>7</td>
<td>B3</td>
</tr>
<tr>
<td>31 74260</td>
<td>14</td>
<td>7</td>
<td>B4</td>
</tr>
<tr>
<td>32 74260</td>
<td>14</td>
<td>7</td>
<td>B5</td>
</tr>
<tr>
<td>33 74260</td>
<td>14</td>
<td>7</td>
<td>B6</td>
</tr>
<tr>
<td>34 74260</td>
<td>14</td>
<td>7</td>
<td>A7</td>
</tr>
<tr>
<td>35 74148</td>
<td>16</td>
<td>8</td>
<td>A3</td>
</tr>
<tr>
<td>36 74260</td>
<td>14</td>
<td>7</td>
<td>A1</td>
</tr>
<tr>
<td>37 74260</td>
<td>14</td>
<td>7</td>
<td>A6</td>
</tr>
<tr>
<td>38 74279</td>
<td>16</td>
<td>8</td>
<td>A5</td>
</tr>
<tr>
<td>39 7400</td>
<td>14</td>
<td>7</td>
<td>B1</td>
</tr>
</tbody>
</table>

Table 5: Integrated circuit summary for Kompuutar. This table summarizes the 85 integrated circuits used in Kompuutar, arranged in groupings by the circuit modules of the system. The column labelled "Map Location" identifies the physical position of the circuits on the various boards of the system, as shown in the physical layout diagrams in the figures. Note that the physical layouts represent a good workable arrangement of sockets. There is no logical requirement that the particular map positions used in these diagrams be followed to the letter in another implementation of the system.
A 50% LARGER EXHIBITION IS PLANNED

The sales results IMM obtained for its 1977 exhibitors is clearly indicative that in 1978 more and more producers will be displaying products for use in every type of industrial, commercial, consumer and military application. Their enthusiasm has prompted many additional manufacturers of small computers (firms which attended and observed in 1977) to make serious commitments regarding participation in the next show. With these new exhibitors and the increased space already requested by 1977 participants, IMM '78 will be a much larger show!

In 1978, the kind of people you want to meet — executives, engineers, designers, manufacturing and support supervisors, and others — will be out in force . . . to see, to learn, to BUY. And you will want to be there with YOUR products and services.

PROGRAMME DESIGNED TO ATTRACT MANY MORE VISITORS

The remarkably large audience of highly qualified and seriously interested visitors who attended the first IMM exposition was obviously pleased with the technical programme. Comments indicate that the programme, as well as the exhibition, will be a key factor in attracting an even larger group of attendees to the next show.

The 1978 programme, chaired and presented by internationally recognised experts, again will be designed to offer the kind of practical solutions to day-to-day problems that attendees seek. A special session on "Tips for Hobby Microcomputers" is being planned.

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Polyscope (Switzerland)
Micomp (Switzerland)
Markt Und Technik (West Germany)
Listing 1: The front panel service program. This program is resident in a programmable read only memory part wired for addresses FE00 to FFFF, as shown in figure 2.4. The listing is a symbolic assembly language version of the program combined with the hand assembled object code provided by author Braden. The information at the end of the PROM area includes the interrupt vectors which are implemented in the Komputer system.
continues execution of the program at the currently displayed address.

After building the design, I found a couple of subtle points in the operation of the control panel. The first point to note is that when using the RESET switch, the processor must be in the RUN mode of the RUN versus STOP switch. Second, bit 5 of the status display is useless and unimplemented in the 6502 hardware. The register load switch (RLG LOAD) is best used for modifying the contents of the accumulator, index registers, but not the stack pointer. Using the register load switch to modify the stack pointer can result in problems when resuming execution of a program. Once whatever memory loading or register alteration chores required by a program have been accomplished, execution can be resumed using the RUN switch to cause the control panel program to return from interrupt using the register contents stored in the control panel scratch area.

A Versatile Configuration

The design of Komputer is quite readily adaptable to the 6800 processor as a substitute for the 6502 if personal programming preference or availability of chips dictates such a switch. The similarities between the two processors are quite extensive, and in fact were the bone of contention of a lawsuit (since settled) shortly after the 6502 came out. At the system level, here are the major differences to be aware of:

- The pinouts of the 48 pin package used for each processor are different, but the signal definitions of NMI, data bus lines, IRQ, reset, address bus, etc., are equivalent.

- The 6800 uses four read only memory interrupt vectors at addresses FF80 to FFFF in memory address space, whereas the 6502 uses only three interrupt vectors; the definitions of the interrupt vectors for reset, non-maskable interrupt and maskable interrupts are similar.

- The instruction set differs, so the front panel service programs shown with this article would need to be recoded if a 6800 is used.

- The definition of the clock used by the processor differs in the details of its drive circuit.

The major features of either a 6502 or 6800 system at the level of the backplane bus defined here would be nearly identical.

**Listing 1, continued:**

<table>
<thead>
<tr>
<th>Hexadecimal Address</th>
<th>Hexadecimal Code</th>
<th>Label</th>
<th>Op</th>
<th>Operand</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF13 FF13 FF13 FF13</td>
<td>47 FF FF FF FF</td>
<td>JMP ADVANCE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF15 FF15 FF15 FF15</td>
<td>48 FF FF FF FF</td>
<td>JMP ADVANCE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF16 FF16 FF16 FF16</td>
<td>AD 00 FF FF FF</td>
<td>FLAG REGISTER CHANGE SERVICE ROUTINE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF17 FF17 FF17 FF17</td>
<td>AD 00 FF FF FF</td>
<td>FLAG REGISTER CHANGE SERVICE ROUTINE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF18 FF18 FF18 FF18</td>
<td>4A 00 00 00</td>
<td>LDA SVAAA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF19 FF19 FF19 FF19</td>
<td>70 00 00 00</td>
<td>BNE SETFLG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF1A FF1A FF1A FF1A</td>
<td>FF 00 00 00</td>
<td>JMP PROCFLAG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF1B FF1B FF1B FF1B</td>
<td>4E 00 00 00</td>
<td>PROCFLAG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF1C FF1C FF1C FF1C</td>
<td>AD 00 FF FF FF</td>
<td>LDX $000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF1D FF1D FF1D FF1D</td>
<td>FF 00 00 00</td>
<td>JMP PROCFLAG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF1E FF1E FF1E FF1E</td>
<td>CA 00 00 00</td>
<td>DEX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF1F FF1F FF1F FF1F</td>
<td>4C FF FF FF</td>
<td>JMP FLGLOOP</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Komputer Peripheral and Scratch Pad Data Symbols**

<table>
<thead>
<tr>
<th>Address</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8000</td>
<td>SVACC</td>
<td>Saved accum value, scratch pad</td>
</tr>
<tr>
<td>8001</td>
<td>SVX</td>
<td>Saved X index register value, scratch pad</td>
</tr>
<tr>
<td>8002</td>
<td>SVY</td>
<td>Saved Y index register value, scratch pad</td>
</tr>
<tr>
<td>8003</td>
<td>SVFFLG</td>
<td>Saved processor status, save register, scratch pad</td>
</tr>
<tr>
<td>8004</td>
<td>SVAAA</td>
<td>Scratch value</td>
</tr>
<tr>
<td>8005</td>
<td>SVSTK</td>
<td>Saved stack register value</td>
</tr>
<tr>
<td>8006</td>
<td>DATAPTR</td>
<td>First operation of scratch pad program; absolute addressing through SVADDIR</td>
</tr>
<tr>
<td>8007</td>
<td>SVADDIR</td>
<td>Low order saved address value, scratch pad program absolute address for DATAPTR</td>
</tr>
<tr>
<td>8008</td>
<td>SVADDIR+1</td>
<td>High order saved address value</td>
</tr>
<tr>
<td>8009</td>
<td>DUMMY2</td>
<td>Balance of scratch pad program</td>
</tr>
<tr>
<td>8010</td>
<td>DUMMY3</td>
<td>Balance of scratch pad program</td>
</tr>
<tr>
<td>8020</td>
<td>DUMMY4</td>
<td>Balance of scratch pad program</td>
</tr>
<tr>
<td>8040</td>
<td>DUMMY5</td>
<td>Balance of scratch pad program</td>
</tr>
<tr>
<td>8050</td>
<td>DUMMY6</td>
<td>Balance of scratch pad program</td>
</tr>
<tr>
<td>8060</td>
<td>SVADDIR</td>
<td>Data value at current SVADDIR</td>
</tr>
<tr>
<td>8061</td>
<td>LSSTCK</td>
<td>Accum in Scratch, temporary</td>
</tr>
<tr>
<td>8062</td>
<td>SVSTK</td>
<td>Scratch value</td>
</tr>
<tr>
<td>8063</td>
<td>REFTP</td>
<td>Front panel request input value</td>
</tr>
<tr>
<td>8064</td>
<td>OSWLOW</td>
<td>Low order data switch register input data of address information shift</td>
</tr>
<tr>
<td>8065</td>
<td>OSWHIGH</td>
<td>High order data switch register input data of address information shift</td>
</tr>
<tr>
<td>8066</td>
<td>STATUS</td>
<td>Status lamp output</td>
</tr>
<tr>
<td>8067</td>
<td>LAUDIR</td>
<td>Low order address display output</td>
</tr>
<tr>
<td>8075</td>
<td>HADDR</td>
<td>High order address display output</td>
</tr>
</tbody>
</table>
the "Thorsen Memory Tube," a magical device which can be programmed with the data necessary for controlling an interactive mechanism. In the real world, technology has developed the semiconductor memory and microprocessors, charge coupled devices and magnetic bubble memories.

In the fictional account, various societal conditions have led to a predilection for garage shop and cottage industry experimentation represented by the efforts of the hero of the story, Dan Davis. In the real world, the technological and economic conditions of today have made the same sort of individualized experimentation with the high technology of computers an everyday occurrence practiced by large numbers of people.

In the story, the protagonists face a world in which mass-produced robotic mechanisms for domestic use have yet to be produced. In the real world, we face a similar situation in which the first mass-produced, intelligent robotic mechanisms for domestic use are on the threshold of invention and possibility.

With this possibility of innovation and invention in robotics growing out of the computer experimenter's natural inclination towards artificial intelligence and robotics work, I can begin to build the concept of an ideal type, "The Compleat Robotics Experimenter" and what it takes to become one. Perhaps we'll see a few examples in real life as the next few years roll by.

Categories of Experimentation

In order to put a finger on the categories of experimentation in the general field of robotics, we need a definition of just what is meant by the concept of a robot. I propose the following definition as a working concept for purposes of discussion. This is not necessarily the ultimate definition of what a robot is, but it serves as a standard of measurement useful in this context.

A robotic system is an intelligent mechanism which is mechanically mobile and which operates with feedback from sensors in a specific environment with general but well defined behavioral goals.

With this definition and given our current levels of technology, I am explicitly attempting to eliminate the classical general purpose robot of science fiction from the discussion. The characters C3PO and R2D2 of George Lucas' film Star Wars may be use-
ful as long term developmental goals, but current technology just does not support practical implementation of such delightful pseudo-persons. The kind of robotic mechanism which is likely to be realizable in the near future by real world personal computing experimenters will be more specialized.

The "intelligent" of intelligent mechanism in the definition might be better expressed as "intelligently designed," for it is the crystallization of the designer's intelligence and creativity in the control algorithms of the machine which enables the robotic mechanism to act "intelligently." "Mechanically mobile" in the definition could be as simple as the mobility of the end of a simple arm mechanism, as complicated as the three-dimensional mobility of a remote flying and hovering mechanism, or as conventional as the rolling mobility of Ralph Hollis' robot NEWT. Sensory feedback is essential to the definition, for I wish to exclude from discussion such conventional mechanisms as plotters, printers, and mass storage devices which use limited forms of mechanical mobility.

A "specific environment" is essential to the practicality of the concept if it is to be accomplished at current levels of understanding of artificial intelligence research and engineering.

A quite practical system for the personal computing experimenter with a mechanical flair is the construction of an "arm" mechanism to act as an output device for a chess program. But the practicality of the possibility comes from the limitation of the environment to a three-dimensional region of space above a well defined chess board, with chess pieces designed to fit the design of the arm's grasping mechanisms and object sensors.

Similarly, the person designing the robotic vacuum cleaner appliance can initially implement a practical design only by limiting its environment, requiring that it:

- Avoid precipices (as at the top of stairs).
- Roll on a plane surface of normal gravity.
- Bounce off walls and furniture.
- Only swallow items smaller than a critical size, while sorting and classifying loose objects above that size but below a maximum size.
- Sense presence of animals, children and adults as a cue to enter standby mode of operation.

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<thead>
<tr>
<th>Item</th>
<th>Kit Price</th>
<th>Assembled Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>MATX 15 Module (Upper Case only)</td>
<td>N A</td>
<td>175</td>
</tr>
<tr>
<td>MATX 1632 Module (Upper and Lower Cases)</td>
<td>N A</td>
<td>275</td>
</tr>
<tr>
<td>MATX 1632 Module (Street with 256-257)</td>
<td>N A</td>
<td>225</td>
</tr>
<tr>
<td>MATX 4248 Count Board</td>
<td>N A</td>
<td>395</td>
</tr>
<tr>
<td>MATX 256-2 Count Board</td>
<td>N A</td>
<td>630</td>
</tr>
</tbody>
</table>

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household robot would specifically exclude any attention to global details such as what to do when it gets wet, what to do in case of fire, how to wash dishes, how to teach children symbolic logic, etc. (Incidentally, the vacuum cleaner just described is one of the robotic mechanisms designed by the hero of Robert Heinlein's Door Into Summer.)

The behavioral design of the robot is a part of this process of limiting the environment. By deciding what the robot is to do, as in the vacuum cleaner case or the chess playing arm case, we impart constraints on its behavior.

The strongest theme of research and experimentation with robotic mechanisms for the near future, then, is that of picking and choosing a particular flavor of environment in which the system is to operate, using this environment definition as the evaluation standard for the design. The environment chosen is what drives the design of mechanisms to interact with that environment; image and sensor processing needs of the system in that environment; software requirements of the computers which implement the processing; and possible avenues of exploration for application concepts.

Defining the Compleat Robotics Experimenter

The personal computer experimenter is well on the way to becoming a robotics experimenter. The intellectual challenge of the robot is a step up in abstraction and difficulty, as well as a step up in fascination and unknowns. What are the requirements of a person who expects to achieve measurable results from experimentation with robotics?

First and foremost, the compleat robotics experimenter is well rounded and virtually the classical Renaissance man. A narrow specialization in one particular aspect of computer science, machine design, etc., may be a useful attribute to possess, but to implement comprehensive systems, comprehensive knowledge is required. For the person just beginning formal education at a college level, a combination of liberal arts and philosophy with computer science, physics, biology and engineering is what I would consider a necessary groundwork for later work in robotics. Getting to more specific details, here are some areas of study with reasons for their usefulness to the aspiring robotics experimenter:

Philosophy, particularly epistemology, is crucial. Epistemology is the philosophical discipline concerned with the question "how do we know what we know?" A
practical understanding of epistemology is a necessary starting point for anyone who would design a knowledge oriented or "artificially intelligent" system.

Related to epistemology is the necessity for a thorough and practical understanding of the mathematical basis for programming and computer science: concepts of logic, proof of theorems, organization of knowledge, etc, form a background for much work with computers.

Progressing to more specific technical areas, the aspiring roboticist must obtain a mastery of computer science, natural and artificial languages, information theory, electrical engineering (at the level of utilizing "black boxes" of function), mechanical engineering and biology or physiology. The knowledge of computer science is a must, for no robot is possible without a computer to implement its intelligence. Natural and artificial language understanding is a requirement for any form of high level command and control structures to be built into the software of the robotic system. Information theory and its attendant discussions of the possibility of error and strategies for coping with error is essential. Electrical engineering and mechanical engineering are obvious for design of interactive real world mechanisms. Biology, particularly the physiology of natural mechanisms, is essential background information to this process of robotic mechanism design: not necessarily for its value as a direct model, but certainly for its inspirational value and value as a source of detail ideas about possible approaches which might work out in robotic mechanisms. Thorough familiarity with current technologies is a must as well.

A final requisite is a thorough familiarity with science fiction literature, for its imagination inputs. The science fiction writer is at once a frustrated engineer and a daring source of imagination. The frustrated engineer aspect comes from the lack of a technological context to fulfill the imaginations; the imagination side is the reason why science fiction is a necessary input for the complete robotics experimenter. Many design ideas can be found in the writings of science fiction thinkers.

Summing it all up, the personal experimentation with technological concepts which so characterizes the amateur computer person finds a natural extension in the application area of robotics. The challenges and problems of building "smart" machines at once provides a form of an answer to the traditional "what do you do with your computer?" question and a fascinating area for exploration.
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stations. Most receivers track a master and two slave stations. This produces two lines of position on a hyperbolic grid; the intersection is the position of the receiver. LORAN-C is a fairly accurate system giving fixes good to from 300 feet to ¼ mile, but it is limited in range. The range is up to 1200 to 1500 miles. Accuracy is degraded at night due to skywave interference. At present LORAN-C coverage is far from worldwide. Since it is principally a system for ship navigation, it is useful mainly in coastal areas. There are lots of receivers on the market, none of which is really inexpensive.

I am familiar with one satellite navigation system in current usage (others are in the developmental stage). This is the Navy Navigational Satellite System. It is a high accuracy system (100 feet for stationary receivers) which measures Doppler frequency of a 150 MHz and a 400 MHz carrier. The use of two frequencies allows for correction for ionospheric refraction. The satellite also transmits digital data which includes time of day and a description of the satellite's orbit. This is usually fed from a receiver into a minicomputer which processes the data and produces a fix in terms of latitude and longitude. This system does not produce continuous navigation since fixes can only be obtained when a satellite passes over the receiver. Since the satellites are in polar orbits the time between fixes normally ranges from 15 minutes to 4 hours with more frequent fixes as the receiver nears either pole. Again a number of companies manufacture receivers, but again they are expensive. A cheap SATNAV receiver and a set of microcomputer programs to produce a fix would certainly be an interesting, though formidable, project.

J. Dean Clamons
Systems Analyst
Shipboard Computing Group
Naval Research Laboratory
Washington DC 20375

SHIMMY?

What causes the shimmy on my video monitor? Sometimes it looks like it's doing a hula.

John C. Ford
9724 Tweedy Ln
Downey CA 90240

The problem superficially sounds like a beat between two frequencies. If the shimmy of which you speak is an amplitude modulation on an otherwise solid picture, you may have some form of cross talk with 60 Hz and some submultiple of your video interface's internal timing references.
Implementing an LSI Frequency Counter

The new generation of programmable large scale integration (LSI) IO devices is proving to be as exciting as the microprocessors to which they are connected. With the aid of these LSI devices, complete functions can be added to a microprocessor system with only a few integrated circuits. One example of an LSI device with this kind of capability is the 8253 programmable interval timer which can be easily interfaced to almost any microprocessor. Using this device, a complete frequency counter can be constructed with just a couple of integrated circuits.

What's on This Chip?

The 8253 contains three independent 16 bit down counters (see figure 1). Each counter has a separate count input, gate input for gating the count and count output. Each can count in binary or binary coded decimal (BCD). Also, each counter can operate in one of four separate modes determined by storing a "mode" word in the device for each of the counters, usually on power up initialization. These mode words stay stored in the 8253 until they are changed by the microprocessor under software control.

In table 2 the format for loading the mode word and reading or loading the count in each counter is shown. The configuration of the mode word is shown in table 3.

The mode word for each counter on the 8253 determines whether the upper or lower half of the counter will be read or written, or whether the counter expects two sequential reads or writes to move 16 bits of data in or out of the device. The type of output the counters will produce is also determined by the mode word. See the shaded box on mode definitions for a discussion of each mode.

Programming the 8253

Each counter is individually programmed by writing a control word to location A1, A0 = 11. The control word format is as follows:

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SC1</td>
<td>SC0</td>
<td>RL1</td>
<td>RL0</td>
</tr>
<tr>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
<tr>
<td>0</td>
<td>M1</td>
<td>M0</td>
<td>BCD</td>
</tr>
</tbody>
</table>

Where D0 - D7 is the contents of the data bus when the mode word is written to the 8253.

In this application the 8253 will be used as a single chip frequency counter. Figure 3 shows the functions of each counter. To determine the frequency of an unknown...
The Two Modes of Operation of the 8253 Used in the Programmable Frequency Counter

Mode 1: Programmable Oneshot

The output will go low on the count following the rising edge of the gate/trigger input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the oneshot pulse until the succeeding trigger. The current count can be read at any time without affecting the oneshot pulse.

Mode 2: Rate Generator

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate/reset input, when low, will force the output high. When the gate/reset input goes high, the counter will start from the initial count. Thus, the gate/reset input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

Table 1: Gate pin operations summary.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Signal Status</th>
<th>Low Or Going Low</th>
<th>Rising</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>●</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1) Disables counting 2) Sets output immediately high</td>
<td></td>
<td>●</td>
<td></td>
</tr>
</tbody>
</table>

Table 2: The configuration of the mode word, which determines whether the upper or lower half of the counter will be read or written, or whether the counter expects two sequential reads or writes to move 16 bits of data in or out of the device.

<table>
<thead>
<tr>
<th>SC</th>
<th>RD</th>
<th>WR</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 3: The format for loading the mode word and reading or loading the count in each counter:

<table>
<thead>
<tr>
<th>SC1</th>
<th>SC0</th>
<th>RL1</th>
<th>RL0</th>
<th>M1</th>
<th>M0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Where

CS = Chip select
RD = Control signal to read data from the 8253
WR = Control signal to write data to the 8253
A₁A₀ = Address lines to select various sections of 8253

Figures 2a and 2b: Two possible modes of operation for the 8253 programmable interval timer. (There are six in all.)
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incoming signal we must count the number of cycles of the signal during a precise predetermined interval called the timebase.

In figure 3 we generate this timebase using counters 2 and 0. The 8080 2 MHz TTL clock, which is crystal controlled at 2.048 MHz, is input to counter 0 operating mode 2. The output of this counter, which divides the output by 20,180, is a precise 10 ms signal. In this mode counter 0 produces 10 ms pulses and produces an oneshot output which serves as a precise interval for counting the unknown frequency.

This timebase interval is programmable by the microprocessor and can be varied from 100 ms to 100 seconds by storing the appropriate divider ratio in counter 2. This oneshot action is initiated under software control by strobing the gate input of counter 2. Note that after the strobe the oneshot action does not start until the next falling clock edge, so the interval is precise.

Next the output of counter 2 goes to the gate input of counter 1 which is operating in mode 2. This counter is allowed to count the unknown frequency of the incoming signal during the period that the gate input is high. The rising edge of the oneshot output of counter 2 is used to interrupt the microprocessor and signal that the frequency to digital conversion is complete. The processor then reads the resultant count in counter 1.

The software for servicing this programmable frequency counter is shown in listing 1. Note that, since these are down counters, the software initializes counter 1 with all 1's and the value stored in this counter at any particular time is the complement of the number of counts received from the unknown frequency. For example, if one count has been received, counter 1 will contain 1111 1111 1111 1110; the complement is 0000 0000 0000 0001.

The maximum count with a 16 bit counter is 65,535. (Note: with time base constants in listing set up for a 1 second count period, this 16 bit range measures frequencies from 1 Hz to 65,535 Hz). If the rising edge of the output of counter 1 (which signals an underflow) is used to interrupt the microprocessor, then the processor can count the number of interrupts in software. The processor can therefore keep a running total of the number of times the counter has passed through 65,535 counts and can therefore adjust the final count appropriately. This will enable counts much larger than 65,535 to be accumulated without having to use additional integrated circuits.

Listing 1: Software for servicing the programmable frequency counter.

```
INITIALIZING THE 8253 COUNTERS FOR THEIR VARIOUS MODES THE 8253 IS CONNECTED IN A MEMORY MAPPED CONFIGURATION IN THIS APPLICATION AND THEREFORE IS ADDRESSED THROUGH MEMORY REFERENCE INSTRUCTIONS

LXI H,P8253 ; INITIALIZE THE 8253
MVI M,COUNT 0 ; INITIALIZE COUNTER 0 TO MODE 2
MVI M,COUNT 1 ; INITIALIZE COUNTER 1 TO MODE 2
MVI M,COUNT 2 ; INITIALIZE COUNTER 2 TO MODE 1

. INITIALIZE COUNTER 2 WITH DIVIDER RATIO TO PRODUCE APPROPRIATE TIMEBASE
DCX H ; POINT TO COUNTER 2
LXI H,TIMEBASE ; TIMEBASE 3EH FOR 10 SEC
MOV M,C ; 64H FOR 1 SEC
MOV M,B ; 0AH FOR 100MS

INITIALIZE COUNTER 1 WITH ALL 1'S SINCE THIS COUNTER WILL BE COUNTING DOWN
DCX H ; POINT TO COUNTER 1
MVI M,OFFH
MVI M,OFFH

INITIALIZE COUNTER 0 WITH A DIVIDE BY 20480
DCX H ; POINT TO COUNTER 0
MVI M,00H
MVI M,50H

THIS SUBROUTINE SERVICES THE FREQUENCY COUNTER INTERRUPT BY READING THE FREQUENCY IN COUNTER 0 AND STARTING A NEW CYCLE
COUNTDONE PUSH A ; SAVE REGISTERS WHICH ARE MODIFIED BY THIS ROUTINE
LXI H,P8253 2 ; POINT TO COUNTER 1
MOV A,M ; GET LSB OF RESULT
CMA ; COMPLEMENT THE DATA
STA COUNTRSLT
MOV A,M ; GET MSB OF RESULT
CMA ; COMPLEMENT DATA
STA COUNTRSLT^1
MVI M,OFFH ; STORE ALL 1's
MVX M,OFFH
OUT START ; CLEAR INTERRUPT AND START NEW CYCLE
POP H ; RESTORE STATUS
POP A ; AND RETURN
EI RET

THIS ROUTINE SERVICES AN OVERFLOW INTERRUPT FROM COUNTER 1 AND KEEPS A RUNNING TOTAL OF THE NUMBER OF OVERFLOWS FOR THIS CYCLE. OTHER SOFTWARE IN THE SYSTEM SHOULD CLEAR THIS QUANTITY WHEN A NEW CYCLE IS STARTED
OVERFLOW
PUSH A ; SAVE SYSTEM STATUS
PUSH H ; INCREMENT OVFLO
LXI H,OVFLO
INC M
OUT CLINT ; CLEAR THE INTERRUPT
POP H
POP A
EI
RET

BY 11 November 1977

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```
While writing Apple BASIC for a 6502 microprocessor I repeatedly encountered a variant of Murphy's Law. Briefly stated, any routine operating on 16 bit data will require at least twice the code that it should. Programs making extensive use of 16 bit pointers (such as compilers, editors and assemblers) are included in this category. In my case, even the addition of a few double byte instructions to the 6502 would have only slightly alleviated the problem. What I really needed was a hybrid of the MOS Technology 6502 and RCA 1800 architectures, a powerful 8 bit data handler complemented by an easy to use processor with an abundance of 16 bit registers and excellent pointer capability. My solution was to implement a nonexistent 16 bit "metaprocessor" in software, interpreter style, which I call SWEET16. This metaprocessor was sketched at the end of my article in May 1977 BYTE, and the purpose of this article is to fill in the details of SWEET16.

SWEET16 is based around sixteen 16 bit registers called R0 to R15, actually implemented as 32 memory locations. R0 doubles as the SWEET16 accumulator (ACC), R15 as the program counter (PC), and R14 as the status register. R13 holds compare instruction results and R12 is the subroutine return stack pointer if SWEET16 subroutines are used. All other SWEET16 registers are at the user's unrestricted disposal.

SWEET16 instructions fall into register and nonregister categories. The register operations specify one of the 16 registers to be used as either a data element or a pointer to data in memory depending on the specific instruction. For example, the instruction INR R5 uses R5 as data and ST @R7 uses R7 as a pointer to data in memory. Except for the SET instruction, register operations only require one byte. The nonregister operations are primarily 6502 style branches with the second byte specifying a ±127 byte displacement relative to the address of the following instruction. If a prior register operation result meets a specified branch condition, the displacement is added to SWEET16's program counter, effecting a branch.

SWEET16 is intended as a 6502 enhancement package, not a stand alone processor. A 6502 program switches to SWEET16 mode with a subroutine call, and subsequent code is interpreted as SWEET16 instructions. The nonregister operation RTN returns the user program to the 6502's direct execution mode after restoring the internal register contents (A, X, Y, P and S). The example of listing 1 illustrates how to use SWEET16 in some program segment.

### Instruction Descriptions

The SWEET16 op code list is short and uncomplicated. Excepting relative branch displacements, hand assembly is trivial. All register op codes are formed by combining two hexadecimal digits, one for the op code and one to specify a register. For example,
up codes 15 and 45 both specify register R5 while codes 23, 27 and 29 are all ST (store) operations. Most register operations of SWEET16 are assigned to numerically adjacent pairs to facilitate remembering them. Thus LD and ST are op codes 2n and 3n respectively, while LD @ and ST @ are codes 4n and 5n.

Operation codes 00 to 0C (hexadecimal) are assigned to the 13 nonregister operations. Except for RTN (op code 0), BK (0A), and RS (B), the nonregister operations are 6502 style relative branches. The second byte of a branch instruction contains a 127 byte displacement value (in two's complement form) relative to the address of the instruction immediately following the branch. If a specified branch condition is met by the prior register operation result, the displacement is added to the program counter effecting a branch. Except for BR (branch always) and BS (branch to subroutine), the branch operation codes are assigned in complementary pairs, rendering them easily remembered for hand coding. For example, Branch If Plus and Branch If Minus are op codes 04 and 05 respectively, while LO @ and ST @ are codes 00012 and 00013.

Theory of Operation

SWEET16 execution mode begins with a subroutine call to SW16 (see listing 2), an assembly of SWEET16. The user must insure that the 6502 is in hexadecimal mode upon entry. If for those unfamiliar with the 6502, arithmetic is either decimal or hexadecimal (binary) depending on a programmable flag, CH. All 6502 registers are saved at this time, to be restored when a SWEET16 subroutine return control to the 6502. If you can tolerate indefinite 6502 register contents upon exit, approximately 30 µs may be saved by entering SWEET16 at location SW16 + 3. Because this might cause an inadvertent switch from hexadecimal to decimal mode, it is advisable to enter at SW16 the first time through.

After saving the 6502 registers, SWEET16 initializes its program counter (R15) with the subroutine return address off the 6502 stack. SWEET16's program counter points to the location preceding the next instruction to be executed. Following the subroutine call are 1 byte, 2 byte, or 3 byte long SWEET16 instructions, stored in ascending

Listing 2: SWEET16 assembly. The SWEET16 program, assembled to reside at location 8000 hexadecimal, is presented by this listing. The primary entry point is at the beginning location SW16. An alternate entry point if there is no need to save processor registers is at location 803 in this assembly, SW16+3.

```
Listing 2: SWEET16 assembly. The SWEET16 program, assembled to reside at location 8000 hexadecimal, is presented by this listing. The primary entry point is at the beginning location SW16. An alternate entry point if there is no need to save processor registers is at location 803 in this assembly, SW16+3.
```
Listing 2, continued:

memory locations like 6502 instructions. The main loop at SW168 repeatedly calls the “execute instruction” routine at SW166, which examines one op code for type and branches to the appropriate subroutine to execute it.

Subroutine SW16C increments the program counter (R13) and fetches the next op code which is either a register operation of the form OP R5-6 (2 hexadecimal digits) with OP between hexadecimal 1 and F, or a nonregister operation of the form 0 OP with OP between hexadecimal 0 and D. Assuming a register operation, the register specification is doubled to account for the 2-byte SWEE116 registers and placed in the X register for indexing. Then the instruction type is determined. Register operations place the doubled register specification in the high order byte of R14 indicating the “prior result register” to subsequent branch instructions. Nonregister operations treat the register specification (right-hand half-byte) as their op code, increment the SWEE116 PC to point at the displacement byte of branch instructions, load the A-Reg with the “prior result register” index for branch condition testing, and clear the Y-Reg.

When Is an RTS Really a JSR?

Each instruction type has a corresponding subroutine. The subroutine entry points are stored in a table which is directly indexed by the op code. By assigning all the entries to a common page, only a single byte of address need be stored per routine. The 6502 indirect jump might have been used as follows to transfer control to the appropriate subroutine:

LDA $ADRHI High order address byte
STA IND+1
LDA OPTBL.X Low order byte
STA IND
JMP (IND)

To save code the subroutine entry address (minus 1) is pushed onto the stack, high order byte first. A 6502 RTS (ReTurn from Subroutine) is used to pop the address off the stack and into the 6502 program counter (after incrementing by 1). The net result is that the desired subroutine is reached by executing a subroutine return instruction! [This ironic situation is an example of what is commonly referred to as “leverness.”]

Op Code Subroutines

The register operation routines make use of the 6502 “zero page indexed by X” and “indexed by X indirect” addressing modes to access the specified registers and indirect data. The “result” of most register ops is lett
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Listing 2, continued:

SWEET16 Operation Code Summary: Table 1 summarizes the list of SWEET16 operation codes, which are explained in further detail one by one in the descriptions which follow the table. The program of listing 2 implements the execution of these interpretive operation immediately following the RTN instruction. The BK operation actually executes a 6502 break instruction (BRK), transferring control to the interrupt handler. Any number of subroutine levels may be implemented within SWEET16 code via the BS (Branch to Subroutine) and R5 (Return from Subroutine) instructions. The user must initialize and otherwise not disturb R12 if the SWEET16 subroutine capability is used since it is utilized as the automatic subroutine return stack pointer.

Memory Allocation and User Modifications

The only storage that must be allocated for SWEET16 variables are 32 consecutive locations in page zero for the SWEET16 registers, four locations to save the 6502 register contents, and a few levels of the 6502 subroutine return address stack. If you don’t need to preserve the 6502 register contents, delete the SAVE and RESTORE subroutines and the corresponding subroutine calls. This will free the four page zero locations ASAV, XSAV, YSAV and PSAV.

You may wish to add some of your own

Table 1:

<table>
<thead>
<tr>
<th>SWEET16 OP CODE SUMMARY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Ops</td>
</tr>
<tr>
<td>--------------</td>
</tr>
<tr>
<td>1n SET Rn Constant (Set)</td>
</tr>
<tr>
<td>2n LD Rn (Load)</td>
</tr>
<tr>
<td>3n ST Rn (Store)</td>
</tr>
<tr>
<td>4n LD @Rn (Load indirect)</td>
</tr>
<tr>
<td>5n ST @Rn (Store indirect)</td>
</tr>
<tr>
<td>6n LDD @Rn (Load double indirect)</td>
</tr>
<tr>
<td>7n STD @Rn (Store double indirect)</td>
</tr>
<tr>
<td>8n POP @Rn (Pop indirect)</td>
</tr>
<tr>
<td>9n STP @Rn (Store pop indirect)</td>
</tr>
<tr>
<td>An ADD Rn (Add)</td>
</tr>
<tr>
<td>Bn SUB Rn (Sub)</td>
</tr>
<tr>
<td>Cn POPD @Rn (Pop double indirect)</td>
</tr>
<tr>
<td>Dn CPR Rn (Compare)</td>
</tr>
<tr>
<td>En INR Rn (Increment)</td>
</tr>
<tr>
<td>Fn DCR Rn (Decrement)</td>
</tr>
</tbody>
</table>

SWEET16 - REGISTER OPERATIONS

The 2 byte constant is loaded into Rn (n = 0 to F, hexadecimal) and branch conditions set accordingly. The carry is cleared.

Example:

15 34 A0 SET R5, A034 R5 now contains A034

The ACC (RO) is loaded from Rn and branch conditions set according to the data transferred. The carry is cleared and the contents of Rn are not disturbed.

Example:

15 34 A0 SET R5, A034
25 LD R5 ACC now contains A034

Text continued on page 159
The ACC (R0) is stored into Rn and branch conditions set according to the date transferred. The carry is cleared and the ACC contents are not disturbed.

Example:

<table>
<thead>
<tr>
<th>LD R5</th>
<th>ST R6</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>36</td>
</tr>
<tr>
<td>Copy the contents of R5 to R6.</td>
<td></td>
</tr>
</tbody>
</table>

The low order ACC byte is loaded from the memory location whose address resides in Rn, and the high order ACC byte is cleared. Branch conditions reflect the final ACC contents which will always be positive and never minus 1. The carry is cleared.

Example:

<table>
<thead>
<tr>
<th>SET R5, A034</th>
<th>LD @R5</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 34 A0</td>
<td>45</td>
</tr>
<tr>
<td>ACC is loaded from memory location A034 and R5 is incremented to A035.</td>
<td></td>
</tr>
</tbody>
</table>

The low order ACC byte is stored into the memory location whose address resides in Rn. Branch conditions reflect the 2 byte ACC contents. The carry is cleared. After the transfer, Rn is incremented by 1.

Example:

<table>
<thead>
<tr>
<th>SET R5, A034</th>
<th>LD @R5</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 34 A0</td>
<td>45</td>
</tr>
<tr>
<td>Load pointers R5 and R6 with A034 and 9022.</td>
<td></td>
</tr>
<tr>
<td>Move a byte from location A034 to location 9022. Both pointers are incremented.</td>
<td></td>
</tr>
</tbody>
</table>

The low order ACC byte is loaded from the memory location whose address resides in Rn, and Rn is then incremented by 1. The high order ACC byte is loaded from the memory location whose address resides in the (incremented) Rn and Rn is again incremented by 1. Branch conditions reflect the final ACC contents. The carry is cleared.

Example:

<table>
<thead>
<tr>
<th>SET R5, A034</th>
<th>LDD @R5</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 34 A0</td>
<td>65</td>
</tr>
<tr>
<td>The low order ACC byte is loaded from location A034, the high order byte from location A035, R5 is incremented to A036.</td>
<td></td>
</tr>
</tbody>
</table>

The low order ACC byte is stored into the memory location whose address resides in Rn, and Rn is then incremented by 1. The high order ACC byte is stored into the memory location whose address resides in (the incremented) Rn and Rn is again incremented by 1. Branch conditions reflect the ACC contents which are not disturbed. The carry is cleared.

Example:

<table>
<thead>
<tr>
<th>SET R5, A034</th>
<th>LDD @R5</th>
<th>STD @R6</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 34 A0</td>
<td>65</td>
<td>76</td>
</tr>
<tr>
<td>Load pointers R5 and R6 with A034 and 9022, Move double byte from locations A034 and A035 to locations 9022 and 9023. Both pointers are incremented by 2.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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### POP @Rn

The low order ACC byte is loaded from the memory location whose address resides in Rn after Rn is decremented by 1 and the high order ACC byte is cleared. Branch conditions reflect the final 2 byte ACC contents which will always be positive and never minus 1. The carry is cleared. Because Rn is decremented prior to loading the ACC, single byte stacks may be implemented with the ST @Rn and POP @Rn operations (Rn is the stack pointer).

**Example:**

<table>
<thead>
<tr>
<th>Hex</th>
<th>OpCode</th>
<th>Decs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 34 A0</td>
<td>SET R5, A034</td>
<td>Init stack pointer.</td>
<td></td>
</tr>
<tr>
<td>10 04 00</td>
<td>SET R0, 4</td>
<td>Load 4 into ACC.</td>
<td></td>
</tr>
<tr>
<td>35 ST @R5</td>
<td>Push 4 onto stack.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 05 00</td>
<td>SET R0, 5</td>
<td>Load 5 into ACC.</td>
<td></td>
</tr>
<tr>
<td>35 ST @R5</td>
<td>Push 5 onto stack.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 06 00</td>
<td>SET R0, 6</td>
<td>Load 6 into ACC.</td>
<td></td>
</tr>
<tr>
<td>35 ST @R5</td>
<td>Push 6 onto stack.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>85 POP @R5</td>
<td>Pop 6 off stack into ACC.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>85 POP @R5</td>
<td>Pop 5 off stack.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>85 POP @R5</td>
<td>Pop 4 off stack.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### STP @Rn

The low order ACC byte is stored into the memory location whose address resides in Rn after Rn is decremented by 1. Then the high order ACC byte is stored into the memory location whose address resides in Rn after Rn is again decremented by 1. Branch conditions will reflect the 2 byte ACC contents which are not modified. STP @Rn and PLA @Rn are used together to move data blocks beginning at the greatest address and working down. Additionally, single byte stacks may be implemented with the STP @Rn and LDA @Rn ops.

**Example:**

<table>
<thead>
<tr>
<th>Hex</th>
<th>OpCode</th>
<th>Decs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 34 A0</td>
<td>SET R4, A034</td>
<td>Init pointers.</td>
<td></td>
</tr>
<tr>
<td>15 22 90</td>
<td>SET R5, 9022</td>
<td></td>
<td></td>
</tr>
<tr>
<td>84 POP @R4</td>
<td>Move byte from A033 to 9021.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>95 STP @R5</td>
<td>Move byte from A032 to 9020.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ADD Rn

The contents of Rn are added to the contents of the ACC (R0) and the low order 16 bits of the sum restored in ACC. The 17th sum bit becomes the carry and other branch conditions reflect the final ACC contents.

**Example:**

<table>
<thead>
<tr>
<th>Hex</th>
<th>OpCode</th>
<th>Decs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 34 76</td>
<td>SET R0, 7634</td>
<td>Init R0 (ACC)</td>
<td></td>
</tr>
<tr>
<td>11 27 42</td>
<td>SET R1, 4227</td>
<td>and R1,</td>
<td></td>
</tr>
<tr>
<td>A1 ADD R1</td>
<td>Add R1 (sum = 885B, carry clear)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A0 ADD R0</td>
<td>Double ACC (R0) to 7086 with carry set.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SUB Rn

The contents of Rn are subtracted from the ACC contents by performing a two's complement addition:

\[
\text{ACC} = \text{ACC} + Rn + 1
\]

The low order 16 bits of the subtraction are restored in the ACC. The 17th sum bit becomes the carry and other branch conditions reflect the final ACC contents. If the 16 bit unsigned ACC contents are greater than or equal to the 16 bit unsigned Rn contents then the carry is set, otherwise it is cleared. Rn is not disturbed.

**Example:**

<table>
<thead>
<tr>
<th>Hex</th>
<th>OpCode</th>
<th>Decs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 34 76</td>
<td>SET R0, 7634</td>
<td>Init R0 (ACC) and R1,</td>
<td></td>
</tr>
<tr>
<td>11 27 42</td>
<td>SET R1, 4227</td>
<td>Subtract R1 (diff = 340D with carry set)</td>
<td></td>
</tr>
<tr>
<td>A1 SUB R1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A0 SUB R0</td>
<td>Clears ACC (R0)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
POPD @Rn

Rn is decremented by 1 and the high order ACC byte is loaded from the memory location whose address now resides in Rn. Then Rn is again decremented by 1 and the low order ACC byte is loaded from the corresponding memory location. Branch conditions reflect the final ACC contents. The carry is cleared. Because Rn is decremented prior to loading each of the ACC halves, double byte stacks may be implemented with the STD @ Rn and POPD @ Rn operations. (Rn is the stack pointer).

Example:
15 34 A0  SET  R5, A034  Init stack pointer.
10 12 AA  SET  R0, AA12  Load AA12 into ACC.
75 STD @R5  Push AA12 onto stack.
10 34 BB  SET  R0, BB34  Push BB34 onto stack.
75 STD @R5  Load BB34 onto stack.
75 10 56  SET  R0, CC56  Clear CC56 off stack.
75 STD @R5  Load CC56 off stack.
C5 POPD @R5  Pop BB34 off stack.
C5 POPD @R5  Pop AA12 off stack.

CPR Rn

The ACC (RO) contents are compared to Rn by performing the 16 bit binary subtraction ACC-Rn and storing the low order 16 difference bits in R13 for subsequent branch tests. If the 16 bit unsigned ACC contents are greater than or equal to the 16 bit unsigned Rn contents then the carry is set, otherwise it is cleared. No other registers, including ACC and Rn, are disturbed.

Example:
15 34 A0  SET  R5, A034  Pointer to memory.
16 BF A0  SET  R6, A0BF  Limit address.
10 00 LOOP  SET  R0, 0  Zero data.
75 STD @R5  Clear 2 locs, inc R5 by 2.
25 LD R5  Compare pointer R5 to limit R6.
D6 CPR R5  to limit R6.
02 F8  BNC LOOP  Loop if carry clear.

INR Rn

The contents of Rn are incremented by 1. The carry is cleared and other branch conditions reflect the incremented value.

Example:
15 34 A0  SET  R5, A034  Init R5 (pointer).
10 00 00  SET  R0, 0  Zero to R0.
55 ST @R5  Clears loc A034 and incrs R5 to A035.
E5 INR R5  Incr R5 to A036.
55 ST @R5  Clear loc A036 (not A035).

DCR Rn

The contents of Rn are decremented by 1. The carry is cleared and other branch conditions reflect the decremented value.

Example: (Clear nine bytes beginning at loc A034)
15 34 A0  SET  R5, A034  Init pointer.
14 00 00  SET  R4, 9  Init count.
10 00 00  SET  R0, 0  Zero ACC.
55 LOOP ST @R5  Clear a mem byte.
F4 DCR R4  Decr count.
07 FC  BNZ LOOP  Loop until zero.

SWEET16 Nonregister Instructions

RTN

Control is returned to the 6502 and program execution continues at the location immediately following the RTN instruction. The 6502 registers and status conditions are restored to their original contents (prior entering SWEET16 mode).
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**BR ea 0 1 d d (Branch Always)**

An effective address (ea) is calculated by adding the signed displacement byte (dd) to the program counter. The program counter contains the address of the instruction immediately following the BR, or the address of the BR operation plus 2. The displacement is a signed two's complement value from -128 to +127. Branch conditions are not changed. Note that effective address calculation is identical to that for 6502 relative branches.

Some examples:

- dd = $80 ea = PC + 2 - 128
- dd = $81 ea = PC + 2 - 127
- dd = $FF ea = PC + 2 - 1
- dd = $00 ea = PC + 2 + 0
- dd = $01 ea = PC + 2 + 1
- dd = $7E ea = PC + 2 + 126
- dd = $7F ea = PC + 2 + 127

Example:

$300: 01 50 BR $352

**BNC ea 0 2 d d (Branch if No Carry)**

A branch to the effective address is taken only if the carry is clear, otherwise execution resumes as normal with the next instruction. Branch conditions are not changed.

**BC ea 0 3 d d (Branch if Carry set)**

A branch is effected only if the carry is set. Branch conditions are not changed.

**BP ea 0 4 d d (Branch if Plus)**

A branch is effected only if the prior "result" (or most recently transferred data) was positive. Branch conditions are not changed.

Example: (Clear mem from loc A034 to A03F)

```
15 34 A0 SET R5, A034 Init pointer.
14 3F A0 SET R4, A03F Init limit.
10 00 00 LOOP SET R0, 0
55 ST @R5 Clear mem byte, incr R5.
24 LD R4 Compare limit to
05 CPR R5 pointer.
04 FB BP LOOP Loop until done.
```

**BM ea 0 5 d d (Branch if Minus)**

A branch is effected only if the prior "result" was minus (negative, MSB = 1). Branch conditions are not changed.

**BZ ea 0 6 d d (Branch if Zero)**

A branch is effected only if the prior "result" was zero. Branch conditions are not changed.

**BNZ ea 0 7 d d (Branch if NonZero)**

A branch is effected only if the prior "result" was nonzero. Branch conditions are not changed.

**BM1 ea 0 8 d d (Branch if Minus 1)**

A branch is effected only if the prior "result" was minus 1 ($FFFF hexadecimal). Branch conditions are not changed.

**BNM1 ea 0 9 d d (Branch if Not Minus 1)**

A branch is effected only if the prior "result" was not minus 1 ($FFFF hexadecimal). Branch conditions are not changed.
instructions to this implementation of SWEET16. If you use the unassigned op codes $0E$ and $0F$, remember that SWEET16 treats these as 2 byte instructions. You may wish to handle the break instruction as a SWEET16 call, saving two bytes of code each time you transfer into SWEET16 mode. Or you may wish to use the SWEET16 BK (Break) operation as a "CHAROUT" call in the interrupt handler. You can perform absolute jumps within SWEET16 by loading the ACC (R0) with the address you wish to jump to (minus 1) and executing a ST R15 instruction.

And as a final thought, the ultimate modification for those who do not use the 6502 processor would be to implement a version of SWEET16 for some other microprocessor design. The idea of a low level interpretive processor can be fruitfully implemented for a number of purposes, and achieves a limited sort of machine independence for the interpretive execution strings. I found this technique most useful for the implementation of much of the software of the Apple II computer; I leave it to readers to explore further possibilities for SWEET16.

### RS

RS terminates execution of a SWEET16 subroutine and returns to the SWEET16 calling program which resumes execution (in SWEET16 mode). R12, which is the SWEET16 subroutine return stack pointer, is decremented twice. Branch conditions are not changed.

```
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O B</td>
<td>Return from SWEET16 Subroutine</td>
</tr>
</tbody>
</table>
```

### BRK

A 6502 BRK (break) instruction is executed. SWEET16 may be reentered non-destructively at SW150 after correcting the stack pointer to its value prior to executing the BRK.

```
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O A</td>
<td>(Break)</td>
</tr>
</tbody>
</table>
```

### BS ea

A branch to the effective address (PC + 2 + d) is taken and execution is resumed in SWEET16 mode. The current PC is pushed onto a "SWEET16 subroutine return address" stack whose pointer is R12, and R12 is incremented by 2. The carry is cleared and branch conditions set to indicate the current ACC contents.

```
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O C d d</td>
<td>Branch to SWEET16 Subroutine</td>
</tr>
</tbody>
</table>
```

**Example:** (Calling a "memory move" subroutine to move A034-A03B to 3000-3007)

```
300: 15 34 AO SET R5, A034 Init pointer 1.
303: 14 3B AO SET R4, A038 Init limit 1.
306: 16 00 30 SET R6, 3000 Init pointer 2.
309: 0C 15 BS MOVE Call move subroutine.
     ...
320: 45 MOVE LD @R5 Move one byte.
321: 56 ST @R6 byte.
322: 24 LD R4
323: DS CPR R5
324: 04 FA BP MOVE Test if done.
326: 0B RS Return.
```

---

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Switching ROMs

in the Fairchild F8 Evaluation Kit

Many people who use the Fairchild F8 Evaluation Kit supplied with the Fairbug Monitor would like to try the Mostek DDT Monitor. Unfortunately, the read only memory chip containing the DDT Monitor cannot be directly substituted into the available socket as wired for the Fairbug read only memory chip. The scheme shown below permits the use of either chip without modifications to the printed circuit board.

The DDT monitor chip is plugged into a wire wrap socket. This socket is wired to a printed circuit socket that plugs into the Fairbug socket. Most of the wire wrap pins can be plugged directly into the socket in piggyback style. The pins marked NC are not connected and can be cut off of the wire wrap socket.

This same type of rewiring scheme must also be performed on QS which is a 7406, since the Mostek and Fairchild boards use mutually inverted signals. Although both chips use the same instructions they seem to be complements of each other to the outside world. Tables 1 and 2 show the interconnections for the two ICs. Note that this scheme of simulating one memory or processor integrated circuit with another similar, but pinout-incompatible, chip can be used quite generally.

Table 1: These are the pin interconnections for the DDT monitor memory to the Fairbug socket. Of the 40 pins that need connecting, 23 of them can be plugged directly into the socket; 14 of them have their pins cut off and aren't used, leaving three pins that need to be rewired.

DDT READ ONLY MEMORY 3851

<table>
<thead>
<tr>
<th>Top wire wrap socket containing DDT</th>
<th>Top wire wrap socket containing DDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - - - - - - 2</td>
<td>21 - - - - - - 21</td>
</tr>
<tr>
<td>2 - - - - - - NC</td>
<td>22 - - - - - - 22</td>
</tr>
<tr>
<td>3 - - - - - - 3</td>
<td>23 - - - - - - NC</td>
</tr>
<tr>
<td>4 - - - - - - 4</td>
<td>24 - - - - - - NC</td>
</tr>
<tr>
<td>5 - - - - - - 2</td>
<td>25 - - - - - - NC</td>
</tr>
<tr>
<td>6 - - - - - - 6</td>
<td>26 - - - - - - NC</td>
</tr>
<tr>
<td>7 - - - - - - 7</td>
<td>27 - - - - - - NC</td>
</tr>
<tr>
<td>8 - - - - - - 8</td>
<td>28 - - - - - - NC</td>
</tr>
<tr>
<td>9 - - - - - - 9</td>
<td>29 - - - - - - NC</td>
</tr>
<tr>
<td>10 - - - - - - 10</td>
<td>30 - - - - - - NC</td>
</tr>
<tr>
<td>11 - - - - - - 11</td>
<td>31 - - - - - - NC</td>
</tr>
<tr>
<td>12 - - - - - - 12</td>
<td>32 - - - - - - NC</td>
</tr>
<tr>
<td>13 - - - - - - 13</td>
<td>33 - - - - - - NC</td>
</tr>
<tr>
<td>14 - - - - - - 14</td>
<td>34 - - - - - - NC</td>
</tr>
<tr>
<td>15 - - - - - - 15</td>
<td>35 - - - - - - NC</td>
</tr>
<tr>
<td>16 - - - - - - 16</td>
<td>36 - - - - - - NC</td>
</tr>
<tr>
<td>17 - - - - - - 17</td>
<td>37 - - - - - - NC</td>
</tr>
<tr>
<td>18 - - - - - - 18</td>
<td>38 - - - - - - 19</td>
</tr>
<tr>
<td>19 - - - - - - NC</td>
<td>39 - - - - - - 39</td>
</tr>
<tr>
<td>20 - - - - - - NC</td>
<td>40 - - - - - - 40</td>
</tr>
</tbody>
</table>

Bottom printed circuit socket. Bottom printed circuit socket.

Table 2: This is the rewiring diagram for the 7406 hexadecimal inverters. This chip must be rewired since the signals coming from the Fairbug monitor are complements of the signals from the Mostek DDT monitor.

Q5 7406

<table>
<thead>
<tr>
<th>Top wire wrap socket containing 7406.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - - - - - - 1</td>
</tr>
<tr>
<td>2 - - - - - - 4</td>
</tr>
<tr>
<td>3 - - - - - - NC</td>
</tr>
<tr>
<td>4 - - - - - - NC</td>
</tr>
<tr>
<td>5 - - - - - - 5</td>
</tr>
<tr>
<td>6 - - - - - - 8</td>
</tr>
<tr>
<td>7 - - - - - - 7</td>
</tr>
<tr>
<td>8 - - - - - - NC</td>
</tr>
<tr>
<td>9 - - - - - - NC</td>
</tr>
<tr>
<td>10 - - - - - - 10</td>
</tr>
<tr>
<td>11 - - - - - - 11</td>
</tr>
<tr>
<td>12 - - - - - - 12</td>
</tr>
<tr>
<td>13 - - - - - - 13</td>
</tr>
<tr>
<td>14 - - - - - - 14</td>
</tr>
<tr>
<td>Bottom printed circuit socket.</td>
</tr>
</tbody>
</table>

Table 2: This is the rewiring diagram for the 7406 hexadecimal inverters. This chip must be rewired since the signals coming from the Fairbug monitor are complements of the signals from the Mostek DDT monitor.
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--- Basic BASIC by James S. Coan. If you're not already familiar with BASIC, James Coan's Basic BASIC is one of the best ways to learn about this popular computer language. BASIC (which stands for Beginner's All-purpose Symbolic Instruction Code) is easy to learn and easy to apply to many problems. Basic BASIC gives you step-by-step instructions for using a terminal, writing programs, using loops and lists, solving mathematical problems, understanding matrices and more. The book contains a wealth of illustrations and example programs, and is suitable for beginners at many different levels. It makes a fine reference for the experienced programmer, too. $7.95.

--- Some Common BASIC Programs by Lon Poole and Mary Borchers, published by Adam Osborne and Associates. At last, a single source for all those hard to find mathematics programs! Some Common BASIC Programs combines a diversity of practical algorithms in one book: matrix multiplication, regression analysis, principal on a loan, integration by Simpson's rule, roots of equations, operations on two vectors, chi-square test, check writer, geometric mean and variation, coordinate conversion and a function plotting algorithm. These are just some of the many programs included. For only $7.50 you can buy the kind of programs previously available only as part of software math package systems for large scale computers. All the programs are written in a restricted BASIC suitable for most microcomputer BASIC packages, and have been tested and debugged by the authors. $7.50.

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An IEEE Microcomputer Course

The IEEE's PHP Group in the San Francisco area is sponsoring a series of talks entitled "Microcomputers: Practical Applications." This Thursday evening series, beginning November 3, will be tutorial in nature, focusing on such "how to" topics as: which microcomputer to use (from the user's viewpoint); architecture and memory; getting started, at work and at home. The series will run for five weeks, with registration set at $35 ($25 for IEEE members; $10 students), and will be in the Palo Alto and San José area. Contact David Guidici at Siltec, 3717 Haven Av, Menlo Park CA 94025, (415) 365-8600.

An Opinion: SOFTWARE AND PATENTABILITY, 1977

While perusing some of the electronic data processing (EDP) literature of the past few years, it struck me that the subject of software patentability had been completely exhausted, and that another article on the subject would cause readers to shy away in revulsion. However, the ebullient EDP industry, in its constant state of change, has preferred a new development which makes all of the irrelevant jabberings of the past (some of them my own) now of considerable importance.

Why have I dismissed the plethora of past writings as irrelevant jabbering? Because the simple and direct answer to the question of whether software is patentable is "no!" Volumes have been filled discussing the point, yet it should have been apparent from the beginning that one insurmountable obstacle stood in the way: namely, that a patentable invention must have a physical existence and not be merely a methodology or mental process.

Hence we see the illogical result of hard wired programming being patentable but pure software not. But all of this really didn't make a great deal of difference because the industry was able to protect its investment in software development through other legal avenues such as trade secrecy and was therefore spared the labyrinthine procedures of the patent law.

All of this is soon to change. As microprogramming state of the art brings us closer to the point where a programmer can sit down with a few integrated circuit chips and a soldering iron rather than a pencil and coding sheet, his/her product (now a black box rather than a source listing) very clearly becomes a candidate for patentability because it is not just a mental process or algorithm any longer, but rather is a physical object.

This means that the arcane and convoluted laws of patents, together with those who administer them, suddenly become relevant in much the same way that a bull in a china shop is relevant. Let us examine a few of the more salient features of patent law and see how they might apply to microprogramming situations.

Novelty

An invention, both in Canada and the United States, must be a "new and useful art, process, machine or composition of matter" to qualify for patent protection (emphasis mine). A new way of achieving a known result, or simply creating a new result, would permit an invention to qualify if the patent officer could be convinced of its novelty.

The reader can appreciate the Alice in Wonderland world which would soon be created by disputed claims revolving around the definition of "new."

Expense

Because all of this jousting is done by high priced lawyers, the cost of obtaining a patent and prosecuting infringement quickly becomes prohibitive for all but the largest corporations; so does defending against an accusation of infringement.

This means that a helligerent patent holder is armed with a big legal stick, the
Introduction to Biomedical Electronics by Edward J. Bukstein. What’s been done in robot doctors? Nothing so far. But in terms of electronic aids to physicians and practices of health researchers, consult this background review of the field of biomedical electronics $5.95.

Security Electronics by John E. Cunningham. To catch a thief, apply liberal doses of ingenuity and a modicum of cleverness. Find out what’s been tried in conventional alarm systems before you go off computerizing your home security system, though. New 2nd edition $5.95.

Practical Microcomputer Programming: The Intel 8080 by W.J. Weller, A.V. Shatzel, and H.Y. Nice. Here is a comprehensive source of programming information for the present or prospective user of the 8080 microcomputer, an architecture which appears in the MITS Altair, 8800, Processor Technology SOL, IMSAI 8080, Polymathics POLY-88, and other popular microcomputer system products.

After several preliminary chapters, the authors get down to practical details with topics such as moving data, binary arithmetic operations, multiplication and division, use of the stack pointer, subroutines, arrays and tables, conversions, decimal arithmetic, various I/O options, real time clocks and interrupt driven processes, and debugging techniques. Most examples are given in symbolic assembly form, with occasional listings of assembled code using a Computer Automation software development system.

This 306 page hardcover book is well worth its $21.95 price and should be in every 8080 or Z-80 user’s library.
The author was obviously working with a nonstandard unit.

A revised figure which agrees with the help rather than a hindrance had the author supplied the connections for the standard version of this device (as was claimed) in his figure 2. I offer a revised figure which agrees with the code assignment charts supplied in both the GI and SMC data sheets and, I belatedly discovered, Don Lancaster’s *TVT Cookbook*. There is very little in common between these two charts. The author was obviously working with a nonstandard unit.

Dr Samuel I Green
13052 Ferntrails Ln
Cree Coeur MO 63141

This is confirmed by a communication from GI, who informs us that the unit by Mr Brehm was indeed a surplus part obtained from a manufacturer of custom encoded keyboards.

Continued from page 37

is part of a feature that allows statements numbers to be interpreted. Readers are welcome to contact me for further information on this interpreter.

I found one additional error: In the right center section of figure 5 on page 61, the second line in the block above the ERROR 2 terminal should read “+S(1) /10 COUNT”.

My thanks to Mr Dickey and to the many other eagle-eyed readers who wrote in to report these errors.

A Revision to “Using a Keyboard ROM”

The article on using a KR2376 keyboard encoder ROM in the May 1977 BYTE, page 76, would have been a great help rather than a hindrance had the author supplied the connections for the standard version of this device (as was claimed) in his figure 2. I offer a revised figure which agrees with the code assignment charts supplied in both the GI and SMC data sheets and, I belatedly discovered, Don Lancaster’s *TVT Cookbook*. There is very little in common between these two charts. The author was obviously working with a nonstandard unit.

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This is confirmed by a communication from GI, who informs us that the unit by Mr Brehm was indeed a surplus part obtained from a manufacturer of custom encoded keyboards.

A Hands-Off Policy

In 1971 I prepared a report for the Canadian Federal Government in which software patentability was examined and recommendation made. At that time I recommended that no changes need be made to the Patent Act so as to extend its application to computer software because the Act would prove inadequate and also because the EDP industry had found trade secrecy laws to meet its needs reasonably well.

I also recommended that no further study in the area would be required until the nature of programming underwent a fundamental change. Although I cannot claim to have foreseen the advent of microprogramming (much less the astonishing speed of its arrival) one can now say that such a fundamental change has occurred.

I therefore recommend that a review be undertaken immediately for the purpose of amending the Patent Act so as to exclude black box microprogramming from its operation.

Such heresy will probably be rejected by bureaucrats who see a golden opportunity to expand their little kingdoms and also by the many patent law firms which would stand to do a land office business.

However, it is accepted that the Patent Act has had serious limitations even in those traditional areas of industry for which it was originally designed. How much less useful it would be in the world of EDP is made plain by that industry’s general avoidance of patent law wherever possible. That being so, it is this writer’s view that the industry should not be dragged kicking and screaming into a morass which it has until now successfully sidestepped.

Daniel A Mersich, Attorney
1262 Don Mills Rd, Suite 17
Don Mills, Ontario

CANADA

[Daniel Mersich is a Toronto lawyer whose practice is restricted to EDP matters...CM/]

<table>
<thead>
<tr>
<th></th>
<th>X0</th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>X4</th>
<th>X5</th>
<th>X6</th>
<th>X7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y0</td>
<td>NUL</td>
<td>NUL</td>
<td>DLE</td>
<td>NUL</td>
<td>NUL</td>
<td>DLE</td>
<td>NUL</td>
<td>NUL</td>
</tr>
<tr>
<td>Y1</td>
<td>SCH</td>
<td>K</td>
<td>FS</td>
<td>SCH</td>
<td>FS</td>
<td>VT</td>
<td>SCH</td>
<td>FS</td>
</tr>
<tr>
<td>Y2</td>
<td>STX</td>
<td>L</td>
<td>FS</td>
<td>STX</td>
<td>FF</td>
<td>SCH</td>
<td>FS</td>
<td>FF</td>
</tr>
<tr>
<td>Y3</td>
<td>EOT</td>
<td>M</td>
<td>US</td>
<td>EOT</td>
<td>CR</td>
<td>US</td>
<td>NUL</td>
<td>CR</td>
</tr>
<tr>
<td>Y4</td>
<td>ENQ</td>
<td>NAK</td>
<td>BS</td>
<td>ENQ</td>
<td>NAK</td>
<td>BS</td>
<td>NUL</td>
<td>BS</td>
</tr>
<tr>
<td>Y5</td>
<td>ACK</td>
<td>SYN</td>
<td>b</td>
<td>ACK</td>
<td>SYN</td>
<td>c</td>
<td>ACK</td>
<td>SYN</td>
</tr>
<tr>
<td>Y6</td>
<td>BEL</td>
<td>ETB</td>
<td>y</td>
<td>BEL</td>
<td>ETB</td>
<td>z</td>
<td>BEL</td>
<td>ETB</td>
</tr>
<tr>
<td>Y7</td>
<td>DCE</td>
<td>CAN</td>
<td>SP</td>
<td>DCE</td>
<td>CAN</td>
<td>SP</td>
<td>DCE</td>
<td>CAN</td>
</tr>
<tr>
<td>Y8</td>
<td>P</td>
<td>EM</td>
<td>LF</td>
<td>DLE</td>
<td>EM</td>
<td>NUL</td>
<td>LF</td>
<td>DLE</td>
</tr>
<tr>
<td>Y9</td>
<td>0</td>
<td>SUB</td>
<td>DEL</td>
<td>0</td>
<td>SUB</td>
<td>DEL</td>
<td>0</td>
<td>SUB</td>
</tr>
<tr>
<td>Y10</td>
<td>SI</td>
<td>SUB</td>
<td>DEL</td>
<td>SI</td>
<td>SUB</td>
<td>DEL</td>
<td>SI</td>
<td>SUB</td>
</tr>
</tbody>
</table>
Do You Need the Real Time?

There are a number of ways of implementing a real time clock for a microcomputer system. With the many different clock chips available on the market, it would seem natural to try to interface to one of these. If the requirements set for a real time clock design are: the computer should be able to read the clock when necessary, the clock should keep time while other programs are executing, and one should be able to set the clock by computer commands, then use of external hardware can be a most difficult challenge. Taking a software approach using minimal hardware can be a most attractive alternative. In the implementation described here, the computer itself counts 1/10 second pulses, derived from the 50/60 Hz line, in four memory bytes, one each for hours, minutes, seconds and deciseconds. Setting the time becomes a process of writing the correct time to memory; reading the time, one of reading memory.

To enable other programs to execute while the clock is being maintained, the computer is forced into the clock counting routine only on the arrival of each 1/10 second pulse, and stays in the routine for only as long as necessary to perform the rather simple calculations before returning to the program that was executing. In my version this is achieved by using the interrupt request line of the 6800 processor, although it is conceivable that the NMI (nonmaskable interrupt) of the 6800 could be used as well.

Pin 4 of the 6800 processor is designated the IRQ line. When this line has a transition from logic 1 (~ +5 V) to logic 0 (ground), the processor finishes its current instruction, stacks all the registers and the address of the next instruction, then branches to the memory location contained in the memory bytes that respond to hexadecimal addresses FFF8 and FFF9. In systems using Motorola’s MIKBUG monitor, such as the SwTPC 6800 computer, the interrupt vector addresses are in MIKBUG and point to another address in MIKBUG so that control of the processor is passed to MIKBUG after the interrupt has happened. MIKBUG dutifully passes control on by branching to the address contained in its volatile user memory at hexadecimal locations A000 and A001. If this address happens to be that of clock counting routine, it will receive control. Since all the registers and machine states have been saved, we can use them to do the

Listing 1a: The real time clock software for a 6800 system which uses an IRQ interrupt input from a PIA port. This routine is intended to be used with the Motorola MIKBUG software, and includes provision for setting time of day in hours, minutes and seconds.

Note: This assembler uses a format in which explicit indication of address type is indicated where one mnemonic has several possibilities. Thus, for example, LDA A # 7 means use immediate (#) addressing of the operand 7, while LDA A E 7 means use extended addressing (E) of the operand at memory location 7. Other abbreviations seen in this listing are R for relative addressing (branches only), I for immediate 2 byte operand; and A designates an assembler directive.
counting without worrying. When we have done all that needs to be done, the RTI instruction restores the registers and branches back to the program that was interrupted.

But how do we interface a signal to IRQ? The simplest way might be to connect it directly, but if one wishes to preserve the option of finding out what caused the interrupt, some additional logic is necessary. While there are probably all sorts of clever ways of doing this, a convenient way to implement it is by using a peripheral interface adapter (PIA). The SwTPC 6800 computer which I use has a parallel interface card which has a PIA. This has 16 data lines and four control lines. We will use one of the control lines, CBI, to latch the clock pulses and provide input conditioning of the interrupt signal. Part of the clock setting routine must be to configure the PIA properly, and part of the interrupt routine to acknowledge the interrupt, which is achieved by reading the PIA B data register, but more of the details later.

A self-supporting real time clock package is given in listing 1b. The package is assembled at hexadecimal location 0700 so as to

The more astute students of MIKBUG will notice that the control line CA1 of the MIKBUG serial control PIA is configured by MIKBUG to cause an interrupt on its transition; CA1 is left free in the SwTPC serial control interface, and interrupts can be implemented in the IRQ line. It is possible to implement the clock, then, by routing the clock pulses to this MIKBUG oriented PIA, with one proviso: that the interface not be used for IO! It is an idiocy of the PIA that if you happen to be reading the data register when the interrupt occurs, the IRQ bit in the control register will not set, even though the interrupt routine will be entered ~ 99.99% of the time. Thus if MIKBUG is doing its IO at the same time as the clock pulse occurs, there is a small, but non-zero chance, that some interrupts will be lost, causing long term timing inaccuracies for a continuously running real time clock.

```
Listing 1a, continued:
```

```
Listing 1b: Object code listing in MIKBUG format for the real time clock program of figure 1a.
```

```

```

```

```
be at the top end of the 2 K supplied with the SwTPC machine, as it was originally sold before 4 K became standard. Modifications to load at other locations are only minor. The package consists of a number of separate segments as follows.

The Clock Counters

Four bytes are reserved for the hours, minutes, seconds and deciseconds clock counters. Each actually contains the natural complement of the value, eg: (24-hours) or (60-minutes).

The Clock Initialization Routine.

On entering this routine, two pairs of two digits must be entered. These are read using the MIKBUG INHEX routine at hexadecimal E0AA. The first of the pair is multiplied by 10, by shifting and adding, and added to the second. The first sum is used to set the hours, the second, minutes. Seconds and split seconds are set to zero. The fourth digit is entered only on the time signal, generated by WWV, for example. To prevent the time from being changed while waiting for the time signal, the clock is inhibited by the SEI instruction and freed when the clock is set by the CLI instruction.

The Clock Counting Routine

This routine is entered when the processor is interrupted, provided the entry point is placed in the MIKBUG programmable memory at hexadecimal A000 and A001. The routine first checks that the clock PIA did in fact cause the interrupt, and acknowledges it by reading the PIA data register. The decisecond counter is decremented and tested. If it has not reached zero, the routine returns to the interrupted program, via the RTI. If it has, the counter is reset to 10 and the minutes counter decremented and tested, and so on. While it may seem that the computer has a lot to do to keep up with the clock, it utilizes only a tenth of a percent of real time during the worst case midnight rollover, and about half that normally.

A Clock Demonstration Routine

A clock demonstration routine has been included in the package and need only be loaded for testing purposes, as ordinarily the clock would be accessed by the main program. The routine prints the time, in hours, minutes and seconds at 1 or 2 second intervals depending on the printer speed. A short routine is used to convert the binary complement of the clock to binary coded decimal (BCD) so that it can be printed in hexadecimal by the OUT2HS routine in MIKBUG at hexadecimal E0CA. After sending CR/LF/* using the MIKBUG PDATA1 to send the MIKBUG MCL string, the seconds timer is read. The program waits in a loop comparing this value with the seconds timer and when a difference is found, the routine loops to print the time again. Also in the loop the routine tests the high order bit of the A data register of the control interface. If this is not 1, it means the operator pressed a key, so the routine

---

Figure 1: A way to derive the power line base of 60 cycles per second (North America) or 50 cycles per second (Europe). The low voltage secondary of the transformer in the power supply drives the Motorola MC14566, a programmable divider with ratios of 5 or 6. A second stage can optionally create 1 Hz as well as the 10 Hz signal assumed by the software of listings 1.
branches back to the MIKBUG CONTROL.
This kind of approach should always be used to return to MIKBUG, for the RESET button will stop the clock by setting the interrupt mask. Also if bit 4 of condition codes on the stack (hexadecimal A043) is 1, the mask will be set upon execution of the G command, which should be avoided.

The timing pulses themselves are derived from the 50 or 60 Hz line using the circuit given in figure 1. The components can be mounted on a small piece of Micro-Vector board, supported at right angles to the base plate of the SwTPC 6800's box, near the +12 V supply board. Three short wires can then be run to one of the 12 VAC transformer leads, to the unregulated 7-8 VDC, and to ground. The output pulses can be strung directly to the C1 pin of a PIA board. The heart of the circuit is the Motorola MC14566 Industrial Time Base Generator. This MOS device contains a divide by 10 ripple counter and a divide by 5 or divide by 6 ripple counter for counting from a 50 or 60 Hz line. Pulse shapers on the inputs accept slow rise time inputs, but it is necessary to filter the line signal with R1 and C1 to remove noise. The two diodes and R2 convert the signal approximately to a square wave for the counters. 1/6 is achieved by strapping pin 11 to ground, to +5 V for 1/5.

Programming Considerations

A potentially dangerous way of moving a string of bytes from one location to another is to use the stack pointer as an index register. It is only dangerous in a case where interrupts are continuously allowed, as with this clock. For example, one might use the routine of listing 2 to move the 100 bytes starting at OLD to 100 bytes starting at NEW.

If an interrupt occurs during the execution of this segment, those bytes just before the stack pointer will be zapped with the register information, which is probably undesirable! In general, when such a technique is used to coordinate multibyte operations, it would be desirable to inhibit the interrupt. This can be done with the instruction SEI which sets the interrupt mask, thereby preventing the interrupts. The companion instruction CLI clears the mask, enabling the interrupt. Thus the segment given would be preceded by an SEI and followed by a CLI. All is fine, provided we do not set the mask for so long that the next interrupt is lost. This is a perfect example of why at least two full index registers should be incorporated in each microprocessor's design. With the routine given, one can

| OLD   | RMB  | 100 |
| NEW   | RMB  | 100 |
| SAVSP | FDB  |     |
|       |      |     |
| STS   | $AVSP|     |
| LDS   | #OLD-1|    |
| LDX   | #NEW |     |
| LOOP  |      |     |
| PUL A |      |     |
| STA A X|     |     |
| INX   |      |     |
| CPX   | LOOP |     |
| BNE   | LOOP |     |
| LDS   | SAVSP|     |

Listing 2.

move about 4 K bytes in 1/10 second, which is probably adequate for most purposes. When used with other software, you'll thus need to check carefully to make sure that any such manipulations of the stack pointer are consistent with the existence of a steady interrupt source. But once you've got a steady clock program going, a number of new possibilities will be open: time tagging files, extending the counters to keep track of days, weeks and years for scheduling personal events to be signalled when the time is ripe, etc.

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In reference to the Technical Forum item in the July 1977 BYTE on page 150, "Is this a valid hot board placement procedure?" I have the following comments:

The suggested procedure in the reference has a near certain probability of causing catastrophic overstress of parts because of the virtual impossibility of maintaining sufficient alignment accuracy during board removal or installation.

The close intercard spacing on most systems makes it very difficult to visually check alignment during installation. Even a rigid card frame will allow sufficient misalignment in the plane of the board to cause a momentary short between two or more pins.

Once installed, the board misalignment can typically be as much as one third of the pin to pin spacing. This reduces the margin for error to a misalignment angle of only about ten degrees. Even with card ejectors working against a rigid metal card frame, a momentary misalignment approaching this magnitude is still possible.

The procedure could be especially disastrous with the most popular 100 pin bus where logic signals and high voltage supply lines use adjacent pins.

Certain boards in high priced integrated systems use special buffering to allow power-on removal and installation where system down time is especially costly. Such would not seem to be true of personal computer systems. It would seem to be an unacceptable risk to use any live board removal or installation procedure considering the large number of damaged, degraded, and potentially degraded parts that would have to be replaced should a momentary pin to pin short occur. The parts replacement time and effort would far outweigh the time saved in not reinstalling the system for each board replacement.

---

BYTE - A Collection of Programming Problems and Techniques, by H A Maurer & M R Williams. Here's a book that presents you with problems! Nearly 400 of them, in fact: problems in games like chess, bridge, and NIM; practical problems such as applications of the law of sines, Cramer's rule for solving simultaneous equations, and applications of Latin squares to problems in probability; and more advanced computer science topics such as the use of Backus-Naur form. One quarter of the book is devoted to an appendix that gives stymied readers hints on how to proceed with solutions to the problems. The most valuable feature of the book, though, is its careful and thorough explanation of the use of algorithms to solve problems. No dyed-in-the-wool programmer or experimenter will be able to read this book for very long before trying to solve the tantalizing and well-presented problems. $13.50.

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NIM is a 2 player game in which the players alternately remove counters from a pile according to some rule. The player removing the last counter is either the winner or loser depending upon the variation. One important characteristic of NIM is that exactly one player has a winning strategy available to him at the start of the game. That is to say, if the game is played "perfectly," the winner will be determined before the game begins.

Two examples will better illustrate these points. Suppose that there are 100 counters and that each player in his turn must take at least one, but no more than ten, counters. In case 1 consider the player taking the last counter as the winner and in case 2 the loser.

The winning strategy in case 1 belongs to player 1. He must take one counter on his first move, and in each successive turn take enough counters so that both players together will remove 11 counters. After player 2 has taken his turns, the number of counters remaining after each round will be 89, 78, 67, and so on down to 12 and finally 1. On his last turn, player 1 will be obliged to take the last counter and therefore lose the game.

With either of these games you will doubtless beat an unsuspecting opponent several times, even if you let him play in the favored position. But eventually, even the most casual observer will notice the invariance of your line of play regardless of what he does. Once he catches on you must find yourself another victim.

NIMBLE is the extension of NIM to a game with several piles and a slightly different rule for removing counters. It, too, has a winning strategy for exactly one of the players. This strategy is slightly more difficult to explain than the earlier ones, but much more difficult to spot. In fact, trying to learn the correct line of play from watching a knowledgeable player is like trying to catch a housefly in your hand: very often you will think you have him but when you open your hand, he's gone. It is for this reason that the game described here was called NIMBLE. It is similar to NIM but requires greater mental agility.

The rules of NIMBLE may be stated very simply. It is played with any number of piles, each of which may contain any number of counters; these numbers are fixed at the start of each game. Each player in turn

<table>
<thead>
<tr>
<th>Game 1</th>
<th>Game 2</th>
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<tbody>
<tr>
<td>Pile 1</td>
<td>Pile 1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
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<tr>
<td>Pile 3</td>
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<td>1</td>
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</table>

<table>
<thead>
<tr>
<th>Game 3</th>
<th>Game 4</th>
</tr>
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<tbody>
<tr>
<td>Pile 1</td>
<td>Pile 1</td>
</tr>
<tr>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>Pile 3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
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</tbody>
</table>

Figure 1: These are the starting positions of four simple NIM type games. If the game is played so that the player removing the last counter wins, player 1 has the advantage in game 1, and player 2 has an advantage in game 2. Player 1 should win game 3, and player 2 should win game 4 if a perfect game is played.

1 has taken his turns the number of counters remaining will be 99, 88, 77, . . . , 11, and finally 0.

Player 2 has the winning strategy in case 2. In each successive turn he must take enough counters so that both players together will remove 11 counters. After player 2 has taken his turns, the number of counters remaining after each round will be 89, 78, 67, and so on down to 12 and finally 1. On his last turn, player 1 will be obliged to take the last counter and therefore lose the game.

NIMBLE is the extension of NIM to a game with several piles and a slightly different rule for removing counters. It, too, has a winning strategy for exactly one of the players. This strategy is slightly more difficult to explain than the earlier ones, but much more difficult to spot. In fact, trying to learn the correct line of play from watching a knowledgeable player is like trying to catch a housefly in your hand: very often you will think you have him but when you open your hand, he's gone. It is for this reason that the game described here was called NIMBLE. It is similar to NIM but requires greater mental agility.

The rules of NIMBLE may be stated very simply. It is played with any number of piles, each of which may contain any number of counters; these numbers are fixed at the start of each game. Each player in turn
removes a quantity of counters from a single pile. He must remove at least one counter, but he may remove the entire pile. The player removing the last counter wins the game. For illustration, consider games 1 and 2 in figure 1. Player 1 has the favored position in game 1. If he is to win, he must remove two counters from pile I at his first play. Then player 2 must remove one of the two remaining counters and player 1 takes the other. In game 2 the advantage is not so obvious, but it belongs to player 2. No matter what player 1 does, player 2 will reduce the game to two equal piles. Then player 2 must remove from one pile whatever player 1 removed from the other.

It is not always so obvious which player has the advantage or, in fact, how to use it; for example, consider the two slightly more difficult examples in games 3 and 4. Unless you know the game strategy, it is not obvious that player 1 should win game 3, and player 2 should win game 4, assuming they play correctly. Before reading on, assume that you are player 1 in game 3 and player 2 should win game 4, assuming they play correctly. Before reading on, assume that you are player 1 in game 3 and player 2 should win game 4, assuming they play correctly.

After becoming an expert at NIMBLE, you will get greater enjoyment from the game if you can empathize with your uninitiated friends' feelings of frustration, feelings which can be better appreciated if you have been in the same situation yourself. So, if you enjoy making your own discoveries, put this program on your computer (without going too deeply into the logic) and play against it for a while as a novice.

Before typing in the program, there are some statements that may have to be changed to make them more digestible to your computer.

1. The BASIC package I used does not have a RANDOMIZE statement. Statements 300 to 350 serve that purpose.
2. Colons (:) were used in statements 10 to 70 to signify remarks in place of REM.

Jack play NIMBLE
Jack be quick,
Jack must learn
The computer's trick.

Listing 1: A BASIC language source listing for NIMBLE.

```
100       **** NIMBLE ****
200
300       WRITTEN BY IRWIN DOLINEN
400       AUGUST, 1976
500
600
700
800 PRINT "NIMP INSTRUCTIONS":
900 GOSUB 1900
100 IF AS="N" GOTO 290
110
120 PRINT "IN THIS GAME OF NIMBLE TWO PLAYERS ARE COMPETING WITH":"
130 PRINT "TWO OR MORE PILES OF OBJECTS WITH M1, M2, M3, M4:""7
140 PRINT "OBJECTS IN PILE I, EACH PLAYER IN TURN MUST SELECT ONE:""7
150 PRINT "FILE ANY TAKE ANY QUANTITY KNOW THAT PILA FROM 1 TO ALL:""7
160 PRINT "THE PLAYER TO TAKE THE LAST OBJECT IS THE WINNER:""7
170 PRINT "THE GAME IS BEGIN WITH A COIN TOSS-THE WINNER OF THAT TOSS:""7
180 PRINT "HAS THE RIGHT TO INDICATE A PREFERENCE FOR GOING FIRST:""7
190 PRINT "SECON:""7
200 PRINT "YOU INICATE YOUR MOVE BY P. 4 "THE PILA NUMBER:""7
210 PRINT "AND THE QUANTITY:""7
220 PRINT "ONCE YOU LEARN THE PROPER TACTIC YOU SHOULD BE THE:""7
230 PRINT "MACHINE ABOUT 50% OF THE TIME-THERE IS A WINNING STRATEGY:""7
240 PRINT "WHICH THE PROGRAM USES:""7
250
260 PRINT "G O O D L U C K I T T!
970 PRINT
280 PRINT
290 DIM G(6,6),V(6),N(6),P(6),W(2)
300 PRINT "Pick a number:""7
310 INPUT X
320 PRINT "Now in instructions";
330 INPUT X
340 PRINT "Thank you!";
350 FOR I=1 TO 19
360 IF I<>9 GOTO 110
370 PRINT "You are 1";
380 IF I<>9 GOTO 190
390 PRINT "You are 2";
400 PRINT "Let us choose the difficulty level:";
410 PRINT "1 = EASY, 2 = MEDIUM, 3 = HARD":
420 INPUT J
430 PRINT "How many piles?";
440 PRINT "Machine about 50% of the time-there is a winning strategy:";
450 PRINT "Which the program uses:";
460 PRINT "Good luck!";
470 PRINT "Now in instructions!";
480 PRINT "How many piles?";
490 PRINT "Machine about 50% of the time-there is a winning strategy:";
500 PRINT "Which the program uses:";
510 PRINT "Good luck!";
520 PRINT "How many piles?";
530 PRINT "Machine about 50% of the time-there is a winning strategy:";
540 PRINT "Which the program uses:";
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790 PRINT "Good luck!";
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820 PRINT "Which the program uses:";
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840 PRINT "How many piles?";
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940 PRINT "Which the program uses:";
950 PRINT "Good luck!";
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970 PRINT "Machine about 50% of the time-there is a winning strategy:";
980 PRINT "Which the program uses:";
990 PRINT "Good luck!"

Jack be quick,
Jack must learn
The computer's trick.
```

By EE November 1977
Listing 1, continued:

100 PRINT "You can choose 1 or 2. You want to be first?"
120 INPUT A, B
140 IF A = B THEN GOTO 160
160 PRINT USING 1790, N
180 NEXT I
190 IF N = 1 THEN 590
200 PRINT USING 1610: "You go first:"
210 PRINT USING 1610: "You lose!"
220 GOTO 110
230 IF P < I > THEN 110
240 PRINT USING 1790, N
250 NEXT K
260 IF N = 1 THEN 590
270 PRINT USING 1600: "You win!"
280 END
290 IF N = 2 THEN 590
300 PRINT USING 1600: "You lose!"
310 GOTO 110
320 IF P < I > THEN 110
330 PRINT USING 1790, N
340 NEXT K
350 IF N = 1 THEN 590
360 PRINT USING 1600: "You win!"
370 END
380 IF N = 2 THEN 590
390 PRINT USING 1600: "You lose!"
400 GOTO 110
410 IF P < I > THEN 110
420 PRINT USING 1790, N
430 NEXT K
440 IF N = 1 THEN 590
450 PRINT USING 1600: "You win!"
460 END
470 IF N = 2 THEN 590
480 PRINT USING 1600: "You lose!"
490 GOTO 110
500 IF P < I > THEN 110
510 PRINT USING 1790, N
520 NEXT K
530 IF N = 1 THEN 590
540 PRINT USING 1600: "You win!"
550 END
560 IF N = 2 THEN 590
570 PRINT USING 1600: "You lose!"
580 GOTO 110
590 PRINT "Your choice - 00 You create 10 piles:
600 FOR J = 1 TO 10
610 IF S < I > THEN GOTO 110
620 PRINT USING 1790, N
630 NEXT J
640 IF S = I THEN GOTO 110
650 PRINT "You should have been first."
660 GOTO 110
670 PRINT USING 1790, N
680 NEXT J
690 IF S = I THEN GOTO 110
700 PRINT "You are the second player."
710 PRINT "Pick a quantity from 1 to 10:"
720 INPUT J
730 IF S < I > THEN GOTO 110
740 PRINT USING 1790, N
750 NEXT J
760 IF S = I THEN GOTO 110
770 PRINT "You should have been first."
780 GOTO 110
790 PRINT "You should have been first."
800 END
810 IF S < I > THEN GOTO 110
820 PRINT USING 1790, N
830 NEXT J
840 IF S = I THEN GOTO 110
850 PRINT "You should have been first."
860 GOTO 110
870 PRINT "You should have been first."
880 END
890 IF S < I > THEN GOTO 110
900 PRINT USING 1790, N
910 NEXT J
920 IF S = I THEN GOTO 110
930 PRINT "You should have been first."
940 GOTO 110
950 PRINT "You should have been first."
960 END
Figure 2: Three example moves from a typical NIMBLLE game. Figure 2a illustrates the board set up before the first move. Notice that all the rows have an even number of Is. Figure 2b shows the board after the first move. The first column now has an odd number of Is. The second player restores the binary balance by removing four counters from the third pile and leaves an even number of Is in each column.

<table>
<thead>
<tr>
<th>(2a)</th>
<th>Pile Number</th>
<th>Quantity</th>
<th>Decimal</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>0 1 1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>6</td>
<td>1 1 0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>5</td>
<td>1 0 1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>(2b)</th>
<th>Pile Number</th>
<th>Quantity</th>
<th>Decimal</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>0 1 1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>0 1 0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>5</td>
<td>1 0 1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>(2c)</th>
<th>Pile Number</th>
<th>Quantity</th>
<th>Decimal</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>0 1 1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>0 1 0</td>
<td></td>
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<tr>
<td>3</td>
<td>3</td>
<td>1</td>
<td>0 0 1</td>
<td></td>
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</table>

3. PRINT USING uses a format statement rather than a format variable (see 1080, 1220, 1230, 1780, 1970, and 1980). This may not be acceptable to your BASIC.

Looking at the sample run, you will see that you have a choice of setting up the game yourself and determining the number of piles and the quantity in each pile, or letting the computer do it. If the computer sets up the game, you must select a difficulty level which determines the maximum number in each pile.

When the game is set up, the computer will simulate a coin toss; the winner will have the privilege of determining who should play first. (If the computer ever wins the toss and loses the game, look for an error in copying the program.) Once you learn the strategy, the game will be decided on the coin toss (unless you win the toss and make an error). You should begin your play by letting the computer set up the games at difficulty levels 1 and 2. When you think that you have discovered the winning strategy, test your theory at the higher levels.

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V The binary value vector $V(I) = 2^{I-1}$.

N The pile quantity vector $N(I) = \text{the number of counters in pile I}$.

G The binary value matrix. $G(I, J) = 1 \text{ or } 0 \text{ depending on whether or not } V(I) \text{ is in the binary representation of } N(J)$.

P The parity vector. $P(I) = 0$ if row $i$ of the $G$ matrix has an even number of 1s; otherwise $P(I) = 1$.

Figure 4: A typical NIMBLL game showing the contents of $G$ matrix and $P$ table for each move in the game.
that looks like figure 2c. The game will continue this way, with player 1 disrupting the balance and player 2 restoring it. Player 1 must ultimately leave a single pile which player 2 will remove. Therefore, if the initial system is in binary balance, it is preferable to go second; otherwise, it is preferable to go first. The strategy is simply to restore binary balance each time your opponent disrupts it.

Now that you know the winning strategy, you will want to learn how the program knows to play it. First we must think of writing binary numbers vertically from bottom up rather than horizontally from left to right. For example, the numbers 3, 5, 7 and 8 would be represented as:

```
3 5 7 8
1 1 1 0
1 0 1 0
0 1 1 0
0 0 0 1
```

This method is used to represent the pile quantities in the G table (matrix).

Figure 3 demonstrates the relationships between the major program tables and how they are used to find the optimal move.

When it is the computer's turn to play, it looks at the P vector, statements 1020 to 1040 of listing 1. If it is not equal to 0 there is no optimal move and the computer plays at random as shown in statements 1050 to
Figure 5, continued:

```
YOUR MOVE 2
MY MOVE IS 3, 3

1 2 3
2 3 1
YOUR MOVE 2
MY MOVE IS 1, 1

1 2 3
1 8 1
YOUR MOVE 2
THAT PILE IS EMPTY

1 2 3
1 8 1
YOUR MOVE 1
MY MOVE IS 3, 1

1 2 3
PTTs PTTs PTTs - PLAY AGAIN
SHOULD I SET UP GAME?
HOW MANY PILES 3 - 6
2 15
1 12
I AM ABOUT TO TOSS A COIN - CALL H OR T
THE TOSS IS T
THERE ARE 3 PILES

1 2 3
6 5 3
MY CHOICE - PONDER PONDER PONDER - YOU GO FIRST - YOUR MOVE 1
MY MOVE IS 3, 2

1 2 3
4 2 1
YOUR MOVE 2
MY MOVE IS 1, 2

1 2 3
2 1 1
YOUR MOVE 2
MY MOVE IS 1, 1

1 2 3
1 8 1
YOUR MOVE 1
MY MOVE IS 3, 1

1 2 3
PLAY AGAIN
FINAL SCORE - ME 4 YOU 0
```
by Rodnay Zaks. Ref. C201

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Dr. Rodnay Zaks has been responsible for the design of industrial microprocessor systems since their inception in 1972. He is the author of 11 educational books in the field and more than 20 scientific publications.

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<td></td>
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</tbody>
</table>

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<tr>
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</tr>
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<td>copies of</td>
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</tbody>
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Figure 5: A flowchart of the floating point addition or subtraction routine.
number of digits can be expanded.

This format has its list of disadvantages, though; but for these the commercial computer industry might have adopted it long ago. The program size required for performing just the basic operations and the conversion routines is about the same as for the other formats, but execution times are significantly slower. Many hobbyists are not as concerned with the number of milliseconds as with the number of bytes, but another disadvantage is the larger memory required to store the floating point numbers. For most assembly language applications the impact is negligible. It does become noticeable, however, when the floating point package is part of higher level language programs such as interpreters or compilers. One major disadvantage is more subtle. Many of the transcendental functions are best implemented using algorithms which are binary based. Using these algorithms, the BCD format is awkward at best and at worst consumes large quantities of time and memory.

The binary floating point format provides the fastest execution times, despite the fact that its format allows representation of 7 digit numbers at all times. Because the entire format is in binary, implementing the basic operations and all of the transcendental functions is easier than when using either of the other two formats.

The major drawback is the small range of numbers representable, relative to the other formats (10^+38 to 10^-38). This is because its exponent is only a power of two compared with bases of 10 and 16 respectively. Two other minor drawbacks are the need for routines to convert floating point numbers from a decimal base to a binary base (and vice versa), and the need to expand the binary format to perform actual calculations.

The hexadecimal floating point format permits a much larger number range (10^+76 to 10^-76) than the binary format, and the conversion routines are similar for both. Although slightly slower than the binary format, the hexadecimal format is still much faster than any BCD format of comparable capability.

It is somewhat more difficult to implement scientific functions such as square root, exponential and logarithm with this format than with the binary format, and its precision is not as good as the binary format's precision because it is digit rather than bit oriented. Even though the most significant digit is nonzero, the most significant three bits of the digit itself may be zeroes, resulting in only 21 bits of accuracy. This translates to only six digits of accuracy.

In describing the four basic floating point operations and the format conversions, the hexadecimal format will be used to illustrate examples.

Floating Point Operations

The software uses three floating point registers, an accumulator, argument register and scratch register. The floating point accumulator contains one of the operands prior to a calculation, and the result after the calculation is performed. The argument register contains the other operand, which is loaded by the routine, and the scratch register is used to hold temporary results.

In each of the basic operations there are two parts: exponent calculation and mantissa calculation. Fixed point operations require only the mantissa calculation, which turns out to be the easier of the two.

Add and Subtract Routine

Figure 5 is a flowchart of the add and subtract routine. The two operations are described together because the algorithms
Two numbers $A$ and $B$, which differ from one another by less than one part in $2^{24}$, but which were represented as two different numbers.

Figure 6a: Two numbers $A$ and $B$, which differ from one another by less than one part in $2^{24}$, but which were represented as two different numbers.

![Mantissa](Mantissa.png)

$A = 100000 \times 16^1$

$B = FFFFFF \times 16^0$

Figure 6b: The same numbers as figure 6a, but with $B$ shifted to the right one digit, and the extra digit stored in the guard byte in preparation for the subtraction shown in figure 6c. This shifting aligns mantissa radix points (makes exponents equal).

![Mantissa](Mantissa.png)

$A = .100000 \times 16^1$

$B = .0FFFFF \times 16^1$

Figure 6c: The subtraction of $B$ from $A$ to give $C$. There is only one significant digit in the result, which is entirely located within the guard byte.

![Mantissa](Mantissa.png)

$A = 100000 \times 16^1$

$B = FFFFFF \times 16^0$

$C = .000000 \times 16^1$

Figure 6d: If the guard byte is omitted, as in this example, the apparent result is off by a factor of 16 due to truncation prior to the mantissa addition (or subtraction).

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Multiplication

Figure 7 is a flowchart of the multiplication routine. Calculation of the exponent for the multiplication and division routines is achieved by adding or subtracting the operand exponents respectively. Since the exponents are in excess-64 notation, the offset (64) will have to be subtracted from or added to the result. If the resultant exponent is less than the smallest exponent or greater than the largest, an underflow or overflow condition exists and the appropriate action is taken (for example, displaying an error message or setting the result to a fixed value). Sign calculation for both multiply and divide is a simple exclusive or of the two operand signs.

The partial product method is the most widely used in fixed point multiplications, decimal or binary based. Using binary numbers, this algorithm rotates the multiplier right one bit and tests the bit rotated out. The multiplicand is conditionally added to the accumulated result if the bit is a one. The result is then rotated right one bit, retaining 32 bits, and the whole procedure repeated for all 24 bits of the multiplier. An example of this algorithm implemented in hardware was found in the article "This Circuit Multiplies" by Tom Hall, page 36 in July 1977 BYTE...CH.

Though the fixed point calculation is straightforward and uncomplicated, it is extremely time consuming because the loop is repeated 24 times. One method of reducing the execution time is to cut out all subroutines within the loop and use only in line code. A complete multiplication routine can then have a worst case multiply time of about 2.5 ms using an 8080 processor with 2 MHz clock.

Division

Figure 8 is a flowchart of the division routine. The fixed point divide algorithm is analogous to the partial product method and is also commonly used. It compares the absolute value of the divisor to that of the dividend. If it is equal to or less than the dividend's absolute value, it is subtracted from the dividend, and a one is rotated into the least significant bit of the quotient. Otherwise there is no subtraction and a zero is rotated in. The dividend is then shifted left one bit and the loop repeated for a total of 32 times, generating a 32 bit quotient. Long division by hand goes through the identical procedure, but it operates on digits instead of bits.

Since more processing is done in each loop cycle than in the multiply routine, division execution times are longer than multiplication times. The worst case times are still around 5 ms for an 8080 with 2 MHz clock.

In both the multiply and divide routines, the normalization procedure is identical to the one in the subtract routine. Therefore it usually turns out to be shared code.

These routines are the core for other floating point functions such as format conversions and scientific mathematical functions. Because of this it is important that these routines execute as fast as possible so that the other functions' execution times are not increased to several seconds instead of fractions of seconds.

BCD to Binary and Binary to BCD conversions are probably the most difficult to implement in a binary floating point package. There are several simple methods of converting integers from one format to the other, but I haven't seen any published literature to date on either floating point arithmetic or number base conversions.
The methods described here were chosen because of their simplicity rather than their speed. The slow base conversions are still relatively fast compared to the character oriented input and output operations in which they are used, so for most purposes the conversion speed is not noticeable.

Decimal to Binary Conversion

The Decimal to Binary (DB) routine (figure 9) converts a free format floating point BCD number in ASCII to binary floating point format, converting from ASCII BCD floating point to formatted BCD floating point, and then to binary floating point in one operation.

After initialization the DB routine first checks for a plus or minus sign, which is optional. It ignores a plus sign and sets a flag if there is a minus sign. It then reads in one or more digits (and possibly a decimal point). When it encounters a decimal point, it tests a flag to see if another decimal point has already occurred and sets the flag if not. If a decimal point has already occurred, the routine jumps to the last section. For each decimal digit input, the routine multiplies the accumulated result by ten in floating point format, creates a floating point number from the digit, and adds the number to the accumulated result. If a decimal point has previously occurred, a decimal exponent count is decremented, keeping track of the number of digits in the fractional part. This process is repeated until a character which is neither a digit nor decimal point has occurred, at which point control passes on to the exponent evaluation routine.

Here the decimal exponent of the number, if any, is processed. The routine first searches for the presence of an E character. If none is present, control jumps to the last section. If the character is present, one or two BCD digits are inputted with an optional plus or minus sign. The BCD digits are converted to an 8 bit binary, two's complement number and added to the decimal exponent count.

Finally, the mantissa is normalized by either repeatedly multiplying or dividing by ten, depending upon the decimal exponent count. Multiplication is performed if the count is greater than zero, and division is performed if it is less than zero. The count is either decremented or incremented respectively toward zero for every multiplication or division. When the count reaches zero, the sign is corrected if the number is negative, and the routine returns.

The Binary to Decimal (BD) routine shown in figure 10 converts a binary floating point number to packed BCD floating point.

The number is left in packed BCD notation so the user can define his or her own format for the decimal point and exponent.

Initially, the binary number is normalized so that it is in the range of 0.1 to 1.0, with a decimal exponent kept separate. This is done by repeatedly multiplying or dividing by 10 until the number is equal to or greater than 1.0 and less than 10.0, and then dividing it by 10.0. During this operation, each multiplication or division by 10 is tabulated in a count. Next, a round off of 0.0000005 is added and a correction, if necessary, is made to make sure the number remains between 0.1 and 1.0.

The number is then converted to a binary fixed point fraction, and finally to a BCD fixed point fraction of eight digits, but accurate to only six digits because of the added round off.

After completing mantissa conversion, the binary count of the decimal exponent is converted to a signed BCD pair and stored with the BCD fraction.
Figure 9: Flowchart of a decimal to binary routine used to convert a free format floating point BCD number in ASCII format to binary floating point format.
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These two algorithms for conversion of bases between BCD (base 10) and binary (base 2) are valid for any binary floating point format, not just the one used here.

Concluding Remarks

It is hoped that this discussion along with the flowchart specifications of the algorithms can be used by readers as a basis for coding a floating point arithmetic package for any general purpose microprocessor system. I have used this information in particular to code an 8080 version of the routines for the basic arithmetic functions, as well as extensions for functions such as square root, exponential, natural logarithm, sine, and cosine, and arc tangent. The extensions all use the basic multiplication, division, addition and subtraction operations to evaluate the more complex functions involved. Readers interested in a detailed copy of this 8080 mathematical function software documentation can purchase it for $10 by writing to me at POB 447, Maynard MA 01754.

Figure 10: Flowchart of a binary to decimal conversion routine used to convert a binary floating point number to packed BCD floating point format.
The notes supplied by Peter Skye in May 1977 BYTE (page 68) created a flurry of correspondence activity from numerous sources. One of the best proposals we've seen is that provided by Glen A Taylor in his letter titled "Language Development: A Proposal." The main theme of his ideas is proposal of what might be called a personal computers language development society. For our part, to help foster such efforts, we will provide a "Languages Forum" platform for individuals wishing to participate in print with ideas on personal computing languages. This forum is open to all who have technical contributions or suggestions to make in the field of language design for personal computing systems.

A fundamental ground rule is that persons submitting letters should supply a complete address and be willing to correspond with other readers. Telephone numbers will be printed if authors of letters to this forum supply them and indicate a willingness to get together via that medium.

Language Development: A Proposal

Glen A Taylor
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Madison WI 53706

After reading Peter Skye's note in May 1977 BYTE and exchanging correspondence with him on the subject of a high level language for personal computing, I am moved to offer the following comments and suggestion. I have two fears. My first is that BASIC may become for home computing what FORTRAN is for large computers, an anachronism which is the definitive programming language. My quarrel with both these languages derives from the following. They are vast improvements over the tedium of programming in assembly language. They are sufficiently powerful to allow most problems to be solved. They are almost universally available. Herein lies their insidious threat. For all these apparent benefits, the programmer still pays an invisibly high cost in their lack of well-structured syntax. Programs cannot be given good clear logical structure as an automatic consequence of the language; only rudimentary mnemonic naming and labelling are permitted; and large amounts of fairly tedious detail must still be attended to in coding reasonably complex programs. Of course, I'm simply restating the often heard arguments for structured programming, but it is a concept gaining rapid widespread acceptance in mainstream computing.

My suggestion is that a group be formed for the purpose of defining a suitable personal computing language. I see this as a unique opportunity and high moral responsibility. We are actively engaged in developing a technology that promises to touch the lives of millions of people who are as yet naive to computing. What finer ambition than to develop a language that is human oriented, powerful, flexible, and that is well-suited to the capabilities of home systems for the foreseeable future. We are fortunate that there are years of research into programming languages and a vast store of programming concepts at our disposal. We need not fashion a language of dated language concepts and practices. We absorb state of the art software technology as soon as it is marketed. We should lead the computing field in readily utilizing state of the art software technology.

Therefore, I challenge readers of BYTE to take the lead and place their support behind such an effort. Here too there are valuable lessons to be learned from the successes and failures of similar ventures...
in the mainstream computing field. The development of such a language must not be delayed until there is little chance of displacing a firmly entrenched BASIC. The effort must enlist the support and assistance of several of the major manufacturers who are committed to offering the language as part of their major software line and providing continuing support for it. Finally, the services of a group of people who have experience with present home systems, a clear vision of where the field is most likely to go, and an expert knowledge of modern language design must be enlisted.

I hope you will consider this suggestion. I hope the readers of BYTE will provide vocal support for this idea, thereby encouraging you to support such a project and demonstrating its ultimate economic feasibility to those who would have to support its cost. I am almost certain that you will find the persons with the necessary technical qualifications to serve on the language designing group among your readership. I challenge these persons to step forward.

Comments on Peter Skye’s Language Proposal

Peter Skye’s proposal to develop a higher level language for microcomputer use is a fine idea, but it seems to be going astray. If the project goes forward as described in the May 1977 Technical Forum it will be an expanded PL/I with added features from APL and SNOBOL and an apparently huge character set. It appears it was planned to be all things to all people (a replacement for all general purpose languages), and I think it will fail for that reason.

Programming languages have been developed to meet particular needs, and they can best be judged on the power and appropriateness of their constructs for dealing with the intended class of problems. SNOBOL, TRAC and LISP do arithmetic poorly but are quite powerful when dealing with strings and natural languages (English, for example). RPG, despite its somewhat primitive nature, is widely used because it is simple and oriented specifically towards producing business reports. (The business world would be far more interested in RPG running on a micro than anything else I can think of!)

The proposed PL/Skye will make no one happy. The comment that nothing a particular language can do can’t be done in PL/I misses the point. BASIC is simple and interactive; APL is powerful and elegant; PL/I is a poor substitute for either. PL/I is fine in large EDP shops which want to convert all their FORTRAN and COBOL programmers to a single, powerful language. It doesn’t need APL as a subset. Furthermore, it might pay to remember early experience with PL/I. The first compilers produced atrocity object code, and some of the features never did work. It took compiler writers quite a while before they learned to produce accurate, optimized

Jeffrey L Kenton
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Wellesley MA 02182

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Notes on Floating Point and Critique of PL/Skye

Stephen R. Alpert
Assoc Prof of CS, WPI
Vice Chairman, SIGMINI (ACM)
11 Ridgewood Dr
Auburn MA 01501

I would like to add a few comments on the articles that appear in May 77 BYTE.

1. In Sheldon Linker's article "What's in a Floating Point Package?", page 62, there are a few items that should be considered.
   a. Usually one tries to keep all floating point information normalized. Let's consider an example: let the exponent be base 10 and assume we have four decimal digits of storage. Then

   \[0.0025 \times 10^5 = 0.2500 \times 10^3 = 250\]

   Clearly I have a choice of storage. But what about 2576? Then I can only use 0.2576\times10^4. Chances are if my operands aren't normalized then the result may not be also.
   b. In conjunction with normalized data, a hexadecimal base will yield a larger range than a binary base, but it will not carry the significance of a binary base. Hexadecimal base means that a leading hexadecimal digit of 1 will waste three binary bits!

c. In all my years of computing (14) I have never had a need for numbers greater than \(10^{38}\) except for the legendary $24 Manhattan Purchase at 6% for 300+ years. I would suggest the following compromise:

\[
\begin{array}{ccc}
\text{EXP} & \text{S} & \text{MANTISSA} \\
8\text{ bit} & \text{1} & 23\text{ bit mantissa} \\
\end{array}
\]

The exponent is a two's complement (excess 200) binary exponent. The dynamic range is \(10^{76}\). The sign bit is stored in place of the normalized most significant bit of the mantissa. Simple shifts or tests will determine the sign (and hence insertion of the MSB is easy).

2. Is Peter Skye serious? I just finished an 8 month project (on the side) writing a compiler for a pseudo-subset of PASCAL. It was a real job. He will require the user to have 32 K bytes just to load the compiler.
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3. A suggestion: following the example of the Communications of the ACM, unless programs are for specific hardware tasks, they should be written in a single “standard” language. My current choice would be PASCAL for the following reasons:

a. It has a very strong (precise) standard. Anyone can purchase a user’s manual and report from Springer-Verlag for about $6.

b. There is a strong user’s group that is international in scope.

c. The language permits definition of user defined data types. One could add bytes, bits, etc. Pointers are standard constructs in PASCAL.

d. If a standard were expounded, I’m sure that in short order actual compilers would soon appear.

e. A top down (or recursive descent) compiler for PASCAL is made easier if the output is, in fact, an assembly language source. This output can then be fed to your favorite assembler. Additionally, by using PASCAL type switches one could imbibe assembler code directly into the higher level code.

f. PASCAL programs would then be highly portable, enhancing the standard even more.

Lest you think PASCAL is my only language, I have also used and taught most of FORTRAN, ALGOL, APL, LISP, FOCAL, BASIC, BLISS and SNOBOL (and a little PL/I).

I hope this letter stirs the pot a bit.

The only problem with making a highly desirable standard representation for published programs is the problem of actually achieving the representations in that form. Documentation of an adequate “representation language” is a necessary first step to a highly desirable end. A syntax and semantic checking program (a compiler minus code generation) would also be most useful from a publication’s point of view to verify and correct superficial details of programs. But such a standardization also requires authors and designers literate in the language as well. Would anyone care to make further comments on this subject of adopting a representation standard for programs in print?

What’s Wrong with PASCAL, Mr. Skye?

David A Mundie
1048 Oakhurst Cir
Charlottesville VA 22903

I am writing in response to the ongoing dialogue in your pages over the choice of a high level language for microcomputers.

Mr. Crone’s analogy with English (May 1977 BYTE, page 112) is misguided. English, though archaic, is both beautiful and well-suited to its purpose; FORTRAN is neither. His letter conjures up visions of our grandchildren using dream computers, yet still struggling with format statements and amorphous programs simply because we lacked the courage to junk our outdated languages as readily as we junk our outdated machines. They will curse us for it.

I do not design computers, so perhaps I am missing something, but Mr. Skye’s comment on PASCAL (May 1977 BYTE, page 68) puzzled me. The point is not that PASCAL does nothing other languages can’t do; the point is rather that PASCAL does virtually everything the other languages do, but starts from a much simpler set of basic constructs. I should have thought that sort of efficiency was just what was needed for microprocessors.

Questioning APL

Rich Snodgrass
229 Liano Dr
Portland TX 78374

I greatly enjoyed the August 1977 issue of BYTE on APL. The articles were well-done and contained much useful information.

I do wish, however, to take issue with some of the views expressed by L. H. Anthony in the Technical Forum. I became weary with superlatives such as “one of the greatest intellectual achievements of this century,” “the teacher of the century,” and “computer languages scarcely bear close comparison with APL.” I hear similar comparisons every year when Detroit comes out with a new model.

Such statements are subjective by nature and hence a total matter of opinion. However Mr. Anthony’s statement that APL is the most “general-purpose mental tool”
in comparison with other computer languages is just too sweeping to let pass without comment.

Generality is an important criterion in judging programming languages and, to a limited extent, APL is blessed in this regard. However, when all the features of APL are examined, it is rather specific.

For example, only homogeneous multi-dimensional arrays, programming of numbers, and single characters are allowed as data structures; COBOL's heterogeneous arrays and list structures available in LISP and SNOBOL are completely lacking. Formatted IO and external data files are not specified in the language definition, features found even in lowly FORTRAN. Structured programming is very difficult in APL, and even the most basic control structures are missing [except, of course, for the computed (GOTO)].

Ironically, that "regrettable language" mentioned in the article, PL/I, has all the features listed above. PL/I also excels in readability and run time efficiency, especially in comparison with APL. Now PL/I is not even close to the "perfect computer language," although it does have more generality than many other languages, including APL.

It will now hopefully be evident that no computer language is best at everything, even APL. The incredible variety of tasks that the computer is now given makes it impossible for one language to be proficient at them all. System programmers should keep an open mind when deciding which languages to implement: LISP, SNOBOL and ALGOL, as well as several other important languages, can be implemented on microcomputers with reasonable memory requirements. All it takes is someone to do it.

Suggestions for APL Optimization

Jon D Roland
Micro Mart
1015 Navarro
San Antonio TX 78205

There seem to me to be three important difficulties with APL that are unnecessary, and that might be corrected in the development of APL for microcomputer systems.

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The attractiveness of APL arises not only from the efficient coding and powerful primitives it provides, but from the ways it facilitates interactive programming, so that the computer user can write programs
on the terminal with a minimum of preparation on paper.

Interaction

The first difficulty arises from the fact that APL is entered from left to right, but executes from right to left. I, like many users, do not always know when I begin a line of program how I am going to finish it, which means that if I am at the terminal, I must either make frequent corrections to what I have already entered, or prepare the statement on paper before I key it into the terminal. I see no fundamental reason why APL could not be reversed, or a reverse APL made an option for the convenience of programmers who think in RPN. There would be no need to change the character set; just make execution from left to right.

Character Displays

The APL character set is not ideal for use with 5 by 7 dot matrix printers or video displays. Some overstruck combinations are not readily distinguishable. Could we not choose characters that are optimal for legibility and aesthetic appeal, even when overstruck?

Keyboard Layout

The arrangement of APL characters on the keyboard is not convenient for rapid, error-avoiding typing. Why could not the APL characters be arranged in some pattern that is optimal for the user who wants to touch-type his input, as the Dvorak keyboard is for ASCII characters (except the special command keys).

If APL, in some form, is destined to become a kind of universal high level computer language, then let us avoid features that are unnecessarily cumbersome for interactive usage, and resolve now to develop a language that is optimal in practical terminal interaction. Let’s not make a mistake like the QWERTY keyboard!

Some Comments on “An APL Bigot Speaks”

Henry Brandt
Ithaca NY 14850

In reference to the letter from Gary Luther in the August 1977 BYTE, page 12 (“An APL Bigot Speaks”), I would like to offer a few points of clarification.

First, the European APL implementation that he speaks of is described in the IBM
The authors of this paper took a full APLSV interpreter and broke it up into 289 128 word modules which are paged into main memory of a System/7. This technique should still prove popular among hobbyists for whom processor costs are overshadowed by the cost of large amounts of main memory.

Second, the IBM 5100 doesn't really put the full APL language in 16 K, as Mr Luther indicated. The 16 K to which he refers is the user workspace, which is available in 16 K increments up to a maximum of 64 K. The APL interpreter is resident in 108 K bytes of read only storage. I suspect a commercially available ROM offering of this nature is still a number of years away.

Lastly, unless we see dramatic changes in the cost of memory, we are most likely doomed to implementing a subset of APL in either ROM or a complete version of it in an overlay fashion for those who possess secondary storage devices such as floppy disks.

---

**Programming Quickies**

A 6800 Program Relocator

Andrew A Carpenter

POB 841

Gordonsville VA 22942

Here is a short program relocator that may be of interest and use to readers of BYTE. The program to be relocated must presently reside in memory. Hexadecimal addresses A002 and A003 are set to the address of the program. Addresses A004 thru A007 are set to the beginning and ending addresses of the new location for the program. This program was written for a SwIPC 6800 system:

```
LOC B: F: F'
1000
1000: FF A002  EDX A002
1005: A000  LDA A00 X
1005: 98  INX
1006: FF A002  STX A002
1007: FF A004  EDX A004
1008: A000  STA A00 X
1008: BF A006  CFX A006
1009: F0 100  BF 2 1219
100A: 34  INX
100B: FF A004  STX A004
100C: 1F 00  BRA 1000
100D: 1F 00  'W'
100E: 96
*** UNRESOLVED ITEMS
*** SYMBOLS SORT
```
Relocatable Object Code Formats

In the July 1977 issue we published a document handed out into the public domain by Peter Formaniak and David Leitch of Mostek. (See "A Proposed Microprocessor Software Standard," page 34, July 1977 BYTE.) Our purpose for publishing the document was to get some interchange started on the issue of relocatable object code formats.

In this continuation of the discussion of the subject of relocatable formats, we have three items. One is a letter reacting to the published information and making some suggestions. The second item is a format used by Technical Design Labs, originated by Neil Colvin. This text was given to us at the TDL booth at the National Computer Conference in Dallas last June, and offered as documentation of a standard which is in use by that firm, and is reportedly being examined for adoption by two other major software vendors in the personal computing marketplace. The third item is a letter from Tom Pittman critiquing the TDL standard, an item which resulted from a recent phone conversation.

As an addition to the discussion, the note following Tom’s critique was received from Philip Tubb, and has a bearing on the process of compiling and making available standards documentation for this field.

A Response to “A Proposed Microprocessor Software Standard”

Carol Anne Ogdin
100 Pommander Walk
Alexandria VA 22314
(703) 549-0646

The proposal put forth by Formaniak and Leitch is certainly a step in the right direction, but it also sets unreasonable limits on the lengths of symbols permitted. By imposing a limit of six bytes on symbol length, the authors propose to throw back programming techniques to the 1960s. A simple analysis of their standard shows a clear and obvious format that permits symbols of virtually unlimited length, although an imposition of a length limit of (say) 64 bytes would not be unreasonable.

In record types 02 and 03, I propose the following modification of their conventions:

<table>
<thead>
<tr>
<th>Byte Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Dollar sign ($) delimiter</td>
</tr>
<tr>
<td>2, 3</td>
<td>Length of the symbol (or zero,</td>
</tr>
</tbody>
</table>

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4, 5 Most significant byte of the address (definition for record type 02, address of chain for type 03)

6, 7 Least significant byte of the address

8, 9 Record type (02 or 03)

10... Symbol text

Last 2 Checksum bytes

CRLF Carriage return, line feed (Delimiter of end of record and end of symbol text)

The advantage of this format is that it permits (but does not require) longer symbols. If the particular assembler author needs to impose some arbitrary restriction on mnemonic and symbolic names, so be it. But, to impose such arbitrary restrictions in a proposed standard assures that the standard will not be adhered to in practice.

Finally, a note about proposed standards themselves. Unless and until the personal computing movement gains a coherent voice through a single forum, standards will remain nonstandard. It behooves the users to get behind the standards movement. Unfortunately, the ANSI mechanism is too burdensome for our needs. If some enterprising publisher (hint, hint) were to dedicate a half a page to listing the currently accepted user standards and the references where the final definition can be found, it might begin to serve as that needed central forum. Could such a list be published every couple of months or so? I should point out that without such a single point of reference, proposed amendments (and general acceptance of the original or amended proposal) will never get properly promulgated to the necessary readers.

Technical Design Labs
Relocatable Object Module Format

DEFINITIONS

Object Module: The output from a language processor. Object modules may be loaded into memory for execution at fixed addresses.

Relocatable Object Module: An object module containing information which allows the loader to place it anywhere in memory address space.

Internal Symbol: A symbol whose location is available to other modules besides the one in which it is defined.

External Symbol: A symbol which is used in a module but is defined as an internal symbol in some other module.

Entry Point: An internal symbol in a module which is used to select the module for loading as a

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result of its being referenced in another module as an external symbol.

**Linkable Object Module**: An object module containing information identifying external, internal, and entry point symbols which can be “linked” to other similar modules by the loader.

**Relocation Base**: The external symbol whose address is the base for the relocation of an object module. The external symbol may represent a program, data, or common area of memory.

**Object Module Format Definition**

The object module format is an extension of the Intel “hex file” format, but is not compatible with that format. The module consists of a sequential file of ASCII characters representing the binary data, symbol and control information required to construct a final program from the module. All binary bytes within this structure are represented as two ASCII characters corresponding to the hexadecimal value of the byte (eg: 11001001 -> C9). All ASCII values are represented by the corresponding ASCII character (eg: A -> A).

Each of the different records within the module is indicated by the use of a prompt character as the first character of the record (in the Intel format, this is the “:”). The valid prompt characters are:

<table>
<thead>
<tr>
<th>Character</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>!</td>
<td>module identification record</td>
</tr>
<tr>
<td>@</td>
<td>entry point record</td>
</tr>
<tr>
<td>=</td>
<td>internal symbol record</td>
</tr>
<tr>
<td>\</td>
<td>external symbol and relocation base record</td>
</tr>
<tr>
<td>&amp;</td>
<td>symbol table record</td>
</tr>
<tr>
<td>:)</td>
<td>data or program or end of file record</td>
</tr>
</tbody>
</table>

Every record in the module is terminated by a one byte binary checksum of all of the preceding bytes in the record except for the prompt character. The checksum is the two's complement of the sum of the preceding bytes. Either output format (two character binary or one character ASCII) still counts as only one byte in the checksum (ie: before conversion for output).

In addition, each record is preceded by a carriage return and line feed sequence to facilitate listing the module on an external device.

**Module Identification Record (“!”)**

<table>
<thead>
<tr>
<th>Byte Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>CR/LF</td>
</tr>
<tr>
<td>3</td>
<td>Exclamation point (!) prompt.</td>
</tr>
<tr>
<td>4-9</td>
<td>ASCII module name. [See comments on length in letter by CA Ogden.]</td>
</tr>
<tr>
<td>10-11</td>
<td>Checksum.</td>
</tr>
</tbody>
</table>
### Entry Point Record ("@")

<table>
<thead>
<tr>
<th>Byte Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>CR/LF</td>
</tr>
<tr>
<td>3</td>
<td>At sign (@) prompt.</td>
</tr>
<tr>
<td>4-5</td>
<td>Number of entry points in this record.</td>
</tr>
<tr>
<td>6-??</td>
<td>ASCII names of entry points, six bytes per name. The names are left justified and blank filled.</td>
</tr>
<tr>
<td>??</td>
<td>Checksum.</td>
</tr>
</tbody>
</table>

### Internal Symbol Record ("#")

<table>
<thead>
<tr>
<th>Byte Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>CR/LF</td>
</tr>
<tr>
<td>3</td>
<td>Pound sign (#) prompt.</td>
</tr>
<tr>
<td>4-5</td>
<td>Number of internal symbols in this record.</td>
</tr>
<tr>
<td>6-11</td>
<td>ASCII name of internal symbol, left justified and blank filled.</td>
</tr>
<tr>
<td>12-13</td>
<td>Relocation base for symbol. The value of this symbol is relative to the relocation base specified.</td>
</tr>
<tr>
<td>14-17</td>
<td>Symbol value (16 bit).</td>
</tr>
<tr>
<td>* * * *</td>
<td>The above three fields are repeated for each internal symbol in the record.</td>
</tr>
<tr>
<td>??</td>
<td>Checksum.</td>
</tr>
</tbody>
</table>

### External Symbol and Relocation Base Record ("\")

<table>
<thead>
<tr>
<th>Byte Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>CR/LF</td>
</tr>
<tr>
<td>3</td>
<td>Backslash () prompt.</td>
</tr>
<tr>
<td>4-5</td>
<td>Number of external or relocation symbols in this record.</td>
</tr>
<tr>
<td>6-11</td>
<td>ASCII name of the symbol, left justified and blank filled.</td>
</tr>
<tr>
<td>12-13</td>
<td>Relocation number assigned to this symbol in this module. This number is unique for each symbol. It starts with one and increases sequentially for each subsequent external or relocation base symbol.</td>
</tr>
</tbody>
</table>
| 14-17       | Relocation segment size or external reference flag. If this value is zero, it represents a reference to a symbol defined externally to this module (usually a subroutine or global data item). If it is nonzero, then the value is the size of the relocation segment as
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defined in this object module. This segment can contain either code or data, and may be located anywhere in memory by the loader, independent of any other segment.

The above three fields are repeated for each symbol contained in this record.

?? Checksum.

• Symbol Table Record ("&")

<table>
<thead>
<tr>
<th>Byte Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>CR/LF</td>
</tr>
<tr>
<td>3</td>
<td>Ampersand (&amp;) prompt</td>
</tr>
<tr>
<td>4-??</td>
<td>The remainder of this record is identical to the internal symbol record. All symbols defined in this module are contained in these records.</td>
</tr>
</tbody>
</table>

• Data/Program Record (";")

<table>
<thead>
<tr>
<th>Byte Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>CR/LF</td>
</tr>
<tr>
<td>3</td>
<td>Semicolon (;) prompt</td>
</tr>
<tr>
<td>4-5</td>
<td>Number of binary data bytes in this record. The maximum is 32 binary bytes (64 bytes of ASCII representation). If this value is zero, this record is a end of file record, described below.</td>
</tr>
<tr>
<td>6-9</td>
<td>Load address of the data relative to the specified relocation base.</td>
</tr>
<tr>
<td>10-11</td>
<td>Relocation base for all relocation in this record. All relocatable values in this record are added to the current value of the specified relocation base before being put into memory.</td>
</tr>
<tr>
<td>12-13</td>
<td>Relocation control byte. This byte controls the relocation of the next eight bytes in the re record if the number of binary bytes remain according to the count field. The bits are used from left to right. The bits have the following meanings:</td>
</tr>
<tr>
<td>0</td>
<td>a single absolute byte implies load unmodified.</td>
</tr>
<tr>
<td>10</td>
<td>a two byte relocatable value, least significant byte first implies add the 16 bit value to the current relocation base, and load the result.</td>
</tr>
<tr>
<td>110</td>
<td>a three byte reference to a different relocation base. The first byte is the relocation base number, and the two after that are the 16 bit value, least significant byte first. This implies add the specified relocation base to the 16 bit value, and load the result.</td>
</tr>
</tbody>
</table>

202 BYTE November 1977 Circle 132 on inquiry card.
Note that a two or three byte combination is never broken across a record boundary.

14-29 Data bytes controlled as above.

30-?? The above control and data byte combinations are repeated as specified by the count.

?? Checksum.

● End of File Record (";")

<table>
<thead>
<tr>
<th>Byte Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>CR/LF</td>
</tr>
<tr>
<td>3</td>
<td>Semicolon (:) prompt.</td>
</tr>
<tr>
<td>4-5</td>
<td>Zero to indicate end of file record.</td>
</tr>
<tr>
<td>6-9</td>
<td>Starting address for module relative to the specified relocation base. This address is optionally generated by the language processor, and may be zero.</td>
</tr>
<tr>
<td>10-11</td>
<td>Relocation base for starting address.</td>
</tr>
<tr>
<td>12-13</td>
<td>Checksum.</td>
</tr>
</tbody>
</table>

Relocation Bases

One of the important capabilities of this object module format is the ability to specify multiple relocation bases for the module contents. These relocation bases may represent ROM versus user programmable memory shared common areas, special memory areas such as video refresh areas, etc. Within a module, each of these relocation bases is assigned a name, and implicitly, a sequentially generated number. The relocation bases are actually assigned values at load time, but all memory references within the module are made relative to one of these bases.

Four of the relocation bases (0 to 3) have predefined names and meanings, and are treated differently at load time than the remainder of the bases. Base 0 represents absolute memory locations (i.e., it always has the value 0). Base 1 has the name ".PROG." and represents the program area (may be ROM or PROM). Most program code is generated relative to this relocation base. Base 2 has the name ".DATA." and represents the local data areas for each module. Most local data is defined relative to this base. Base 3 has the name ".BLNK." and represents the global "blank common." This relocation base is always assigned the value of the first free address in memory after the local data storage (.DATA) and other data relocation segments. Because it is
always the last allocated, modules referencing this area can be loaded in any order, regardless of the amount of the area they use.

Relocation segments relative to bases 1 and 2 (.PROG. and .DATA.) are always loaded additively. (i.e. After each module is loaded, the value of the relocation base is increased by the size of the segment.) All other relocation bases are assumed to have constant values during the load process and may be allocated by the loader.

Comments on the TDL Relocatable Loader Format

It begins to look like we are going to see the same diversity in design of software in the personal computer industry that we have seen in the hardware design. This remark is prompted by a document describing Technical Design Labs' "Relocatable Object Module Format" which I recently had a chance to examine.

TDL is not the first to promote a relocatable format, and you may be sure they will not be the last. Let me suggest some reasons. But first I should remark that the people at TDL have obviously put a lot of thinking and work into their format. It will serve them for much software, some of which is clearly still in the future. My personal impression is that the format tries so hard to be "efficient" that it has acquired the distinct flavor of a kluge, but I will admit that to be a matter of taste and not a matter of substance.

The problem with the TDL format, and also with the other formats which have come before, is that it is limited to the relocation of 16 bit addresses. This may be satisfactory for relocating jumps and subroutine calls, but it is quite unworkable for data references where the actual address of the reference must be computed from a relocated base address plus some computed offset. It is true that you can use an LXI instruction in the 8080 or Z80 and do the arithmetic through the register accumulator ADD instructions, but in the 6800 there is no convenient way to do arithmetic from an address loaded into the index register with an immediate mode. Even worse, the 6502 has no 16 bit register which may be loaded immediate, and the programmer would be forced to such subterfuges as defining an address constant containing the relocated address, then using extended addressing to refer to it. Another hazard which does not affect the 8080 and Z80 is the problem of relocating base page addresses. So far I have seen nobody address this problem, and yet the 6502 is effectively inoperable without reference to page 00. Are we to continue to force users to laboriously allocate page 00 even after relieving them of the same drudgery with respect to the rest of memory?

I should also like to mention two other problems which have not been addressed, but which are considerably less severe. One has to do with the problem of the difference between two relocated addresses. Most assemblers do not allow constructs of the form (LXI B, ALPHA-BETA), where ALPHA and BETA are both externals.
construct is not allowed because there is no way to pass expressions to the loader. It is a useful construct, and at present the only way to accomplish the same effect with a relocatable code costs seven extra instructions. But as I said, this is less important. More important is the problem of error checking. For reliable media, who cares? But if we are going to bother to put checksums in the format, we should be sure that everything important is checked. As far as I know, only the hex absolute format defined by MOS Technology does this, unless the TDL loader insists on the presence of the carriage return linefeed and requires the next character to be either a colon or dollar. Most loaders simply ignore all text until the header character is recognized, which gives rise to the possibility that lines may be dropped, an occurrence I know to have happened. I think the loader should ignore control characters (CRLF should be optional) but have some safety against dropped lines.

I said we would be seeing several relocatable formats. Like the hardware designers, no software designer is completely satisfied with what someone else has designed, so he/she wants to do her/his own. But more than that, when a proposed standard has serious deficiencies, it will not be widely accepted. As you no doubt have suggested by now, I think I can do better. Time alone can tell whether we actually achieve any standards in this area.

Announcing the Central Standards Library

To help solve some of the standards problems in the small computer and microcomputer field, ALF Products is sponsoring a Central Standards Library (CSL). After discussions with several manufacturers in this field at the West Coast Computer Faire, ALF has set up the CSL as a means of standards information exchange for manufacturers, consumers, hobbyists, and others interested in standards. The Library will collect submitted standards and distribute them on a nonprofit basis. For more information on available standards, on how to submit standards, and on the Library's services, send $1 (to cover printing and mailing costs) to The Central Standards Library, c/o ALF Products Inc, 128 S Taft, Denver CO 80228. You will receive a copy of the first CSL newsletter and the first submitted standard (a parallel interface standard). Manufacturers currently participating include: ALF Products, IMSAI Manufacturing, PolyMorphic Systems, Proko Electronics, Vector Graphic, and Video Terminal Technology.

Among the things I like about the computer field is that it inspires a new style of solitaire: It's me against the computer, and, if I'm persistent, I can always win. A frequent problem, however, is finding a game which will both bring satisfaction and sharpen my skills. Many beginning programming books give only modest examples and problems which do not challenge the intermediate student. Since the trip from apprentice to journeyman is paid for only with experience, a good selection of programming problems is a must.

For the enthusiast seeking a challenge, or the novice wishing to become a pro, Messrs Maurer and Williams have filled this need with nearly 400 problems of varying degrees of difficulty. These exercises provide experience in most of the common problems encountered by programmers. Working your way through the book will provide an insight into the mysteries of applied higher mathematics, even though no knowledge of mathematics above the high school level is required. You'll find sections on number theory, random numbers and equations in one variable. The chapter on games discusses chess and checkers, and there are number games throughout the book. The IO section challenges you to print bridge hands, or perhaps a calendar. You can make maps, circles and family trees. Some of the great problems and legends of history are also described; perhaps you can solve them.

The problems are couched in general terms so that any of the common programming languages may be used. Introductory problems range from the reading and printing of data to the calculation of a bowling score. More difficult problems address satellite orbits and language translation. There is an excellent advanced section dealing with simple compilers and three-dimensional plotting, as well as the sorting and merging of data. In working out these problems the programmer will gain a facility in common applications.

An appendix of partial answers to prob-

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lems is provided. Since there are many ways to program a given task, sample programs are not given. A well thought out index provides a reference to any particular problem or concept.

The excellence of this book lies not only in its graduated problems, but also in the truly great variety of the exercises. It is not an introductory text, but of course there are many of those. It does promise to make the reader a "tackle anything" programmer, which is the very best kind.

Noel K Julkowski
18755 Van Buren St
Salinas CA 93901


This excellent book is perfectly suited for the technically inclined reader who wants to know more about artificial intelligence (AI) and robotics. Written by one of the pioneers in AI research, it provides comprehensive, up-to-date coverage of the field in a style that adroitly balances technical depth against readability and understandability. Raphael is especially effective in illustrating abstract ideas with memorable examples, like a "cryptarithmetic" puzzle which is explored via a tree search, and a butler and maid mystery which is solved by theorem proving techniques.

The book's introduction, which provides a basic orientation to computers for the uninitiated, also discusses special AI peripherals and software, and deals, albeit briefly, with two common misconceptions about computers: that they are just giant arithmetic calculators, and that they are dumb
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with these approaches are described, leading to a consideration of the interplay between syntax and semantics, and more recent approaches such as case grammars and conceptual dependency theory. Actual systems which understand English are reviewed, with a special emphasis on Winograd’s very successful program, SHRDLU. The chapter concludes with comments on the promise of current research into speech understanding systems.

Succeeding chapters deal with perception and picture processing, and robot systems. Techniques such as smoothing and sharpening, finding edges and lines, and dealing with light and shadow are described in enough detail to give the reader an idea of how these things are done, with illustrations from the work of Guzman, Huffman and Waltz. The history of robots is reviewed, with examples from Ross Ashby’s Homeostat, Grey Walter’s tortoises, the Johns Hopkins “beast,” the MIT robot arm, and Meredith Thring’s inventions. Then a case study is presented of Shakey, the SRI robot.

The final chapter comments on “frontier applications” in which the fruits of AI research can be used to better our world. Examples are drawn from work in education, psychology and medicine, as well as other fields. The book concludes with an eloquent commentary on the potential for dehumanization and the promise of enrichment of our society posed by intelligent machines. The key, of course, is understanding, and Raphael has made a real contribution to popular understanding of artificial intelligence research by writing this book.


John A N Lee, a professor of computer science at Virginia Polytechnic Institute and State University, has written a book that bridges the information gap between the elementary explanations of compilers which are usually found in the last chapters of introductory textbooks, and the very abstract theoretical explanations, ie: those that speak in terms of “given a set S.” Dr Lee’s clear, precise prose possesses a great deal of flair leading the motivated reader from first principles to complex operations.

This book is a “how to” book, abundant
in explanation, striving to impress upon the reader the hows and whys of current day symbolic language definition and execution. Dr Lee places a great deal of emphasis upon the differences between compilers and interpreters by emphasizing that compilers produce separate code (object code) that is executed after the compilation phase of execution is finished; but interpreters execute the source code on a line by line basis which may not be optimal in terms of processor time. Compilers, as contrasted with interpreters, output object code to some intermediate storage medium for later execution. This means that execution of compiled programs is often more efficient, in terms of processor time, than interpretive execution each time the program is run. However, source code errors are more difficult to correct in compilers than similar errors in interpreters because there may not be a clear relationship between compiled object code and the original source code. Interpreters, on the other hand, by virtue of their line by line execution characteristic, retain a definite relationship between object code and source code. This simplifies the debugging of source code. As a result of these considerations, we may find an increasing interest in compilers among computer hobbyists as high speed mass storage devices become less expensive.

Dr Lee also discusses, in great detail, lexical analysis and syntactical analysis. He explains that lexical analysis serves to remove redundancy, condense statements and delimit phrases from the source code. Syntactical analysis serves to recognize phrases, parse statements and generate parsed text. After discussing symbol tables which are used by the compiler to reference symbols from the source code, he covers string manipulation and Polish string conversions in great depth. Program control also receives thorough treatment.

Throughout the book Dr Lee draws profusely upon examples of actual implementations of the techniques he describes. Examples are taken from ALGOL, APL, BASIC, FORTRAN, PL/I, and other languages, thereby avoiding the trap of producing a one language book. Also, much to the author's credit, the book is profusely illustrated with flowcharts illustrating the algorithms described. In summary, Dr Lee's book is clear, readable and certainly useful to the serious home computerist. Its wealth of practical information should be welcome to any computerist's bookshelf.

Michael E Sullivan
OZ Division USS Saratoga (CV-60)
FPO NY 09501-
Stock Market Anyone?

An association of persons who have a serious personal interest in using a microcomputer for stock and commodity market investment purposes is being formed. If you are a brave soul with something interesting on your mind, send your idea to John Stanton, 7517 Jonquil, San Antonio TX 78233, or phone (512) 657-3069.

LICA

The Long Island Computer Association is a group of hackers, amateurs and even some pros in the Commack, Long Island area. The monthly meetings feature good speakers, fun and refreshments. The group publishes a newsletter called The Stack. Nonmembers are welcome to all meetings; bring the whole family! Write to Long Island Computer Association, c/o Dave Metal, editor, 28 Splitrail Pl, Commack NY 11725.

Washington Amateur Computer Society (WACS)

Every two months or so WACS sends us a rather impressive computer newspaper with items of interest to club members and non-

HP-65 Users' Club

This club was started to support the HP-65 programmable calculator, but now all modes are supported (HP-25, HP-25C, HP-55, HP-67, HP-97 and HP-65). The newsletter, called 65 Notes, is an excellent publication in which members (and even nonmembers) share programs, ideas, frustrations, etc. Even if you are not a programmable calculator devotee (timesharing takes note... you'll find something here. For more information contact Richard J. Nelson, editor, HP-65 Users' Club, 2541 W Camden Pl, Santa Ana CA 92704

SPC-12 Users' Group

Anyone who would like to form an SPC-12 users group in the Chicago area should contact Manuel C Martinez, 7706 W Gregory St, Chicago IL 60656, or call (312) 631-6623.

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**RAMS**

The Rochester Area Microcomputer Society is a group of individuals with the members alike. It is printed in the form of a computer printout by a DECsystem-10. The club meets monthly; for specifics, write to Washington Amateur Computer Society, 4201 Massachusetts Av, Washington DC 20016.

6800 Users in San Jose

Anything and everything to do with 6800 microcomputers is of interest. Hardware and software are always on display by area hobbyists, and everyone is welcome. Meetings are on the first or second Tuesdays of each month. Contact the 6800 Computer Club at POB 18081, San Jose CA 95118 for more information.

The Chicago Area Computer Hobbyist's Exchange

The monthly publication of the Chicago Area Computer Hobbyist's Exchange is The Cache Register. This impressive newsletter has all the necessary club information, some great programs, convention news, editorials and so on. If you want club information, or would like to receive this newsletter, simply write Chicago Area Computer Hobbyist's Exchange, POB 36, Vernon Hills IL 60061, or call (312) 849-1132.

KIM-1

The KIM-1 users' group has introduced The First Book of KIM, designed to help beginning KIM users. Introductions to programming, interfacing to KIM, games and utility programs are all covered.

If you are a KIM-1 user/owner/soon to be owner, then the KIM-1/650X User Notes is for you. All kinds of helpful software and stuff is packed into this bimonthly. For more information, write KIM-1/650X User Notes, 109 Centre Av, W Norriton PA 19401.

South Florida Computer Group

In the Ft Lauderdale/Miami area, meeting times vary. These people put out a newsletter with page numbers in binary. For information on joining the club or receiving the newsletter write to South Florida Computer Group, 1155 NW 14th St, POB 236188, Miami FL 33123, or phone (305) 324-5572, ext 45.

The club meets monthly; for specifics, write to Washington Amateur Computer Society, 4201 Massachusetts Av, Washington DC 20016.
aim of advancing the spread of interest and knowledge in home computing. By bringing together professionals and amateurs, businessmen and women, students, and just plain interested novices, the society acts as a focal point for the distribution of information and help in the field of microcomputing.

RAMS meets on the second Thursday of every month at Rochester Institute of Technology, building 9, room 1030, at 7:30 PM. Meetings usually include a guest lecture on some general interest topic relating to computers, and discussions by members of their own experiences. The "random access" sessions allow anyone with a question to draw upon the help of the entire group. Membership to RAMS costs $5 per year and includes a subscription to the club magazine, Memory Pages. For more information, or a free copy of Memory Pages, write to RAMS, POB D, Rochester NY 14609, or call Glenn Alexander, president, at (716) 377-0697.

Tulsa Computer Society

The TCS had an exhibit at the Woodland Hills CA Personal Computing Expo, and from the look of the photos in the TCS newsletter, it was a success.

Mike McNatt, editor of The IO Port (the newsletter of the TCS) has informed us that they would like to trade the IO Port with other newsletters from other clubs. Write to Mike McNatt, c/o TCS, POB 1133, Tulsa OK 74101.

1802 Users' Group in Ontario

Here is another group of hackers who are building their own systems from the ground up using 1802 chips with a kit similar to the Cosmac Elf. The club, numbering approximately 300, is currently working on more memory and IO hardware, and is soon to start on monitor programs and BASIC interpreters for the 1802. Write Tom Crawford, 50 Brentwood Dr, Stony Creek, Ontario CANADA L8G 2W8.

A Compucolor Users' Group

The Compucolor Users' Group is dedicated to the exchange of programs and technical data for the Compucolor color display system. They anticipate issuing a news bulletin periodically. Subjects such as how to concatenate tapes and disks will be covered. For each accepted program a member will receive a number of other programs in return. The initial membership fee of $10 covers the duplication and mailing of materials. Those wishing to join the group may...
send the fee to S P Electronics, 5250 Van Nuys Blvd, Van Nuys CA 91401. Further information may be obtained by sending a large self-addressed, stamped envelope to the above address.

Among the present programs are an illustrated version of blackjack, an excellent version of Star Trek, a slot machine, and more. For the most part the group tries to exchange recorded media rather than program listings. Anyone interested is welcome to write.

Central Pennsylvania Computer Club

The Central Pennsylvania Computer Club is now forming for people who are interested in all aspects of computers, both large and small. People in the Philadelphia, Pittsburgh, Baltimore or New York area are invited to contact either Joseph Pallas, 1979 Crooked Oak, Lancaster PA 17601, (717) 569-3137, or David M Ciemiewicz, 333 N Holly St, Elizabethtown PA 17022, (717) 367-6512. They are seeking material for their newsletter, the Data Dump.

Montreal Area Computer Society

Over the past year, the Montreal Computer Society has grown from 12 members to over 90! The club meets once a month, usually on second Tuesday evenings at Vauicv College, 5160 Decarie Blvd. For further information, contact John Erikiev, president, at (514) 932-2344, or write Montreal Area Computer Society, POB 613, Stock Exchange Tower, Montreal, Quebec CANADA.

Space Coast Microcomputer Club

The second edition of the Space Coast Microcomputer Club Newsletter has an interesting feature by Paul Rainosek: a tabulated comparison of some of the different microprocessor chips available. The various advantages and disadvantages are clearly listed. Included are the Intel 8080, Motorola M6800, MOS Technology 6502, Signetics 2650, and Cosmac 1802. To find out more about the Space Coast Microcomputer Club, contact Ray Lockwood, 1825 Canal St, Merritt Island FL 32952.

Officially LACC

The Louisville Area Computer Club (LACC), formerly Louisville Users of Microprocessors (LUMP), hereby mentions the fact that the club has a new name. So, those...
of you who have been looking for "LUMP" meetings should now go to "LACC" meetings. These are held on the first Saturday of each month at 1 PM (usually). Check with this address for the locations: LACC, 115 Edgemont Dr, New Albany IN 47150.

An F8 Users' Club

A group of Fairchild F8 users has started in the Hartford CT area. They have three F8s built and running with two systems having 5 K and 16 K memory, and are interested in contacting other F8 users who would be interested in exchanging information and programs. Contact G W Hemphill, 132 Scott Swamp Rd, Farmington CT 06032.

The First Annual Micro-Chess Tournament

The first annual Micro-Chess tourney will be held in Louisville KY in August of 1978, sponsored by the Louisville Area Computer Club. To put on a really fair tournament the club is in the process of drawing up the rules and regulations. The preliminary rules are:

- Competition limited to approved 8 bit microprocessors; no bit slice machines will be allowed. Other microprocessors will be considered. Send request with stamped, self-addressed envelope to address below.
- Programs can be in either machine language or a higher level language.
- 16 K 8 bit words memory maximum. (9 bits if parity is used.)
- Homebrew machines and commercial machines allowed.
- Machines may be loaded from any media but after the program is operating the loading device must be detached.
- A panel of judges will rule promptly on program crashes or other unexpected problems.
- Competition will be timed.

The 1979 Micro-competition will allow up to 32 K bytes of memory; the 1980 will allow 64 K bytes (65,536 bytes) of memory. The sponsoring committee reserves the right to alter the rules to meet unforeseen situations. First, second and third place prizes will be awarded. For further information write: Louisville Area Computer Club, 3028 Hunsinger Ln, Louisville, KY 40220.
Continued from page 22

Listing 1: Most of the lunar landing games I have seen are not flexible enough to run a two degree of freedom real time simulation as described in this article, so I have included this listing. At each initialization, this program finds a random set of starting conditions (speed, position, mass, etc) that is consistent with a safe landing. It then keeps track of speed, position and fuel consumption, printing them as required, and indicating when the surface has been reached. The following adjustments will have to be made by each user:

1. Function USR(X) must be provided to return the current desired thrust settings, 0 to 100% in the vertical direction, and -100% to +100% in the horizontal direction. These inputs are best achieved by analog to digital conversion from joysticks or slide pots.

2. The step size and print interval must be adjusted for your system clock and peripheral speed in order to simulate real time operation accurately.

3. Function RND(1.) is assumed by the program to return values between 0. and 1. Alterations may be necessary to suit your version of BASIC.

4. The comments printed by the program have deliberately been kept short. A better game could be fashioned by adding instructions, comments on performance, low fuel warning, etc. In other words, customize the simulation to suit your own tastes.

The speed of a computer makes it possible to find results quickly for times far into the future, even if the step size is quite small. This is fortunate, because as our simulation stands now, an error is introduced at each step that becomes worse as the step size becomes larger. The error occurs because in a real LEM the mass and speed are changing all the time, but in our simulation they can be changed only between steps. A variety of numerical methods have been developed to cope with this problem. In our example, simply using the average of the beginning and ending values in each step would be quite effective. Actually, if the step size is small, say 0.01 seconds, even this is not necessary. It is true that by using the average values the program could be made to run faster, but it would also need to store several extra variables, require more lines of code, and use more memory. Obviously, there are trade-offs to be made among speed, accuracy, complexity and size. In each simulation, the programmer must decide which combination is best.

For our games application, the combination is not critical. A high degree of accuracy is not required, and the program is short enough that memory requirements should not be a problem. The selection of speed, however, presents an opportunity that is unique to the user of a dedicated system. With a little trial and error, it should be possible to find the step size which causes your system to take exactly 1 second to calculate and display the speed and position
BREWED APPLICATION SOFTWARE

MINI WORD PROCESSING (MWP) enables the user to prepare letters, text and mailing labels or envelopes. When used for correspondence processing, MWP allows each entry in the name/address file to be described by a number of group codes and document codes. For example, an entry could be group coded by date and inquiry type. Phrases, paragraphs or pages can be specified as document codes to produce an individual letter for each name/address. MWP provides on-line editing and page or phrase insertions during text generation. The letter and text output modules provide text insert or replacement margin control and page numbering.

DISK SORT supports fixed or variable length sequential files of any size and will sort or merge on any number of keys anywhere in the record. An interactive generator allows the user to define a customized sort-merge program for each task. Multiple sort-merge tasks can run unattended with user defined job stream links (eg., sort 12 tiles, merge them with another sorted tile, and link to your report program). Memory and disk space are managed by the system to minimize processing time.

UNIVERSAL DATA ENTRY (UDE) system interacts with the operator to generate custom key-to-disk modules. User defined displays provide full on-line complexity. Validation procedures such as check digits, value tables, range tests, batch totals and record counts improve data quality. Selectable field duplicate or increment eliminate repetitive entries. UDE supports fixed or variable length disk files. Specialized UDE modules can be generated for any application that requires keyed input.

The above systems are extremely easy to use and include carefully created prompts and error recovery well written user manuals with varied examples and extensively documented programs with detailed remarks. Each of these systems is priced at $495. The programs are supplied on diskette and run under MITS Disk Extended BASIZ. See your computer dealer or contact us.

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1 second into the future. One machine might do 100 steps of 0.01 seconds and then print the speed, etc. Another might do 64 steps of 0.015625 seconds before displaying new results. Still another, with slow peripherals, might output speed and position only every 2 or 3 seconds. In any case, as long as the simulated data appears at the same time that real data would, your system will be said to be running a real-time simulation. A real-time lunar lander game gives you exactly the same time to react as would be given a real excursion module pilot.

To help you implement this idea on your own system, a BASIC language program has been included with this article as listing 1. It should be easy to follow, but a few points are worth explaining. At each step the program will need to obtain the thrust settings. This is done through a function called USR. Because systems differ widely, the content of USR is left to you. Some systems will be able to use a register to hold the thrust; others will access memory location; and some may have to query an input port. Also left to the user is the manner in which the thrust settings are updated. Obviously, they cannot be entered at the keyboard for each 0.01 second step. The keyboard could be used via an interrupt routine however. Ideally, you could implement Thomas Buschbach's joystick interface (March 1977 BYTE, page 88) to allow continuous control of thrust in both degrees of freedom. What began as a simple game will now have become a real-time lunar landing simulator requiring quick thinking and a good bit of practice to master.

If you use this idea then my article will have succeeded in its purpose of introducing some of the basic concepts of simulation. Techniques like separating the problem into degrees of freedom, determining the effect of each force separately, and stepping the simulation into the future are all fundamental to any prediction of motion. The differences between this lunar lander game and the complex simulations used in the space program lie in the way forces are determined and in the numerical methods used to calculate speed and position. In future articles, other applications for simulation on microcomputers will be discussed as a means for demonstrating some of those advanced techniques. For now, try applying the ideas presented here to create a game of your own.

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The TOOL you have been waiting for. A 6800 Reference Data Guide (similar to the IBM green card) containing just about every piece of pertinent information that you are currently spending valuable time searching for. The guide saves TIME, EFFORT and WORK SPACE when programming, debugging and utilizing the 6800 system.

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Pseudorandom
Number Generator

Daniel Grieser
4326 Kenny Rd
Columbus OH 43220

The following algorithm for generating a pseudorandom number is based on the "power residue" method described in an IBM Data Processing Techniques bulletin. The modification presented here preserves the brevity of the power residue approach and yields 256 8 bit numbers before repeating. Any seed, including zero, can be used prior to initializing the sequence. The algorithm is simply stated: to obtain the next random number, multiply the previous number by 13 and retain only the least significant 8 bits of the product, then add 1 to the product yielding the new random number. In an 8 bit microprocessor this is accomplished by a series of shifts and additions.

Listings 1 and 2 give an 8080 and a 6800 version of this algorithm, requiring 16 and 15 bytes of storage, respectively. Both are simple subprograms which execute straight through without any loops.

---

**Listing 1:** An 8080 version of the random number routine. This routine uses registers of the processor as temporaries, and places its result in memory location RND. Multiplying by the number 13 is accomplished with shifts and additions without any looping by noting the identity:

\[13xN = Nx2^3 + Nx2^2 + N\]

The power-of-two factors are generated by left shifts.

<table>
<thead>
<tr>
<th>Address</th>
<th>Hexadecimal Code</th>
<th>Label</th>
<th>Op Code</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 00</td>
<td>21 0F 00</td>
<td>ENTRY</td>
<td>LXI H,RND</td>
<td>Point to RNDM # storage.</td>
</tr>
<tr>
<td>00 03</td>
<td>7E</td>
<td>MOVA,M</td>
<td>ADD A</td>
<td>Shift left once.</td>
</tr>
<tr>
<td>00 04</td>
<td>87</td>
<td>ADD A</td>
<td>Shift left again.</td>
<td></td>
</tr>
<tr>
<td>00 05</td>
<td>87</td>
<td>ADD A</td>
<td>Store briefly.</td>
<td></td>
</tr>
<tr>
<td>00 06</td>
<td>4F</td>
<td>MOV C,A</td>
<td>ADD M</td>
<td>Add unshifted number.</td>
</tr>
<tr>
<td>00 07</td>
<td>86</td>
<td>MOV M,A</td>
<td>MOV A,C</td>
<td>Store the sum.</td>
</tr>
<tr>
<td>00 08</td>
<td>77</td>
<td>ADD A</td>
<td>Retrieve the temporary number.</td>
<td></td>
</tr>
<tr>
<td>00 09</td>
<td>79</td>
<td>ADD A</td>
<td>Shift left.</td>
<td></td>
</tr>
<tr>
<td>00 0A</td>
<td>87</td>
<td>ADD M</td>
<td>Add the sum again.</td>
<td></td>
</tr>
<tr>
<td>00 0B</td>
<td>86</td>
<td>INR A</td>
<td>Increment the sum.</td>
<td></td>
</tr>
<tr>
<td>00 0C</td>
<td>3C</td>
<td>MOV M,A</td>
<td>Store the new random number.</td>
<td></td>
</tr>
<tr>
<td>00 0D</td>
<td>77</td>
<td>RET</td>
<td>Return calling program.</td>
<td></td>
</tr>
<tr>
<td>00 0E</td>
<td>CB</td>
<td>RND</td>
<td>Random number storage.</td>
<td></td>
</tr>
</tbody>
</table>

**Listing 2:** The equivalent routine specified for a 6800 processor. Note that for both the 8080 and 6800 versions, the code is completely position independent so the absolute object code shown can be used without any modifications.

<table>
<thead>
<tr>
<th>Address</th>
<th>Hexadecimal Code</th>
<th>Label</th>
<th>Op Code</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 00</td>
<td>F6 00 0E</td>
<td>ENTRY</td>
<td>LDA B RND</td>
<td>Load B with last RND #.</td>
</tr>
<tr>
<td>00 03</td>
<td>17</td>
<td>ASL B</td>
<td>Shift B left.</td>
<td></td>
</tr>
<tr>
<td>00 04</td>
<td>58</td>
<td>ASL B</td>
<td>Twice.</td>
<td></td>
</tr>
<tr>
<td>00 05</td>
<td>58</td>
<td>ASL B</td>
<td>Add to A.</td>
<td></td>
</tr>
<tr>
<td>00 06</td>
<td>18</td>
<td>ABA</td>
<td>Shift again.</td>
<td></td>
</tr>
<tr>
<td>00 07</td>
<td>58</td>
<td>ABA</td>
<td>Add to A.</td>
<td></td>
</tr>
<tr>
<td>00 08</td>
<td>18</td>
<td>INC A</td>
<td>Increment A.</td>
<td></td>
</tr>
<tr>
<td>00 09</td>
<td>4C</td>
<td>STA A RND</td>
<td>Store result as new</td>
<td></td>
</tr>
<tr>
<td>00 0A</td>
<td>87 00 0E</td>
<td>RND</td>
<td>RNDM # and return.</td>
<td></td>
</tr>
<tr>
<td>00 0D</td>
<td>39</td>
<td>RTS</td>
<td>Random # storage.</td>
<td></td>
</tr>
</tbody>
</table>

---
William Leier sent us the following letter detailing his thoughts about APL and GRAPL. The latter is a new language Mr Leier is currently helping to develop.

I have used APL professionally for many years, implementing such things as Jay Forrester’s simulation of the world and a graphics animation package with which I have produced several movies. But there are many severe limitations to APL, some of which become critical on small systems like the typical microcomputer. A few of these are:

- All arrays in APL must be homogeneous, i.e.: all elements must be of the same type. Since APL does not allow data structures (like PL/I or COBOL), it is sometimes difficult to define variables that are convenient to manipulate. This results in more computer time being spent getting the data into an array for a simple APL matrix multiply than the time required to actually perform the multiply.
- APL simulates operations in parallel so well that there are no constructs for operations serially (such as a looping construct). This leads to much wasted computation (i.e.: testing all elements of a character vector to see if they are equal to a space when all you really want to do is find the first nonblank character). This may not mean much on, say, the IBM 370, but it slows a microcomputer down.
- APL is terrible for dataset management.
- APL has no interrupt action other than the ability to break to the terminal user. This requires explicit tests to be included for such things as zero divides, etc. There have been patches for this, but they are hard to use.
- Since APL creates and destroys large arrays frequently and at random, storage management must be done with some sort of free space list (which eats up storage) and a garbage collector with full compaction of free space (which really eats up time). This means that, while on a large system most FORTRAN or PL/I programs will completely fit in 128 K, an APL program is given (normally) 64 K bytes just for data and a symbol table, not to mention the space occupied by the APL system.
- Almost no translation can be performed on APL code. Every time a variable name is encountered, it must be looked up in the symbol table. A lot of wasteful data checking must be done before the simplest operation can be performed.
- Character handling in APL is clumsy and difficult to code. Only with great effort can APL code be made self-documenting. Trying to decipher old code (even my own) quickly leads to the funny farm.

But APL has many great features, several of which I wish would be available on a microcomputer. I have found many of these features in a language called GRAPL. GRAPL at first looks similar to APL, but there are changes and improvements, far too many to list here. But just to begin:

- GRAPL uses symbolic operators (like APL), but GRAPL uses the standard ASCII character set with no overstrikes. The large set of operators is derived by allowing two character operators.
- APL execution is from right to left; GRAPL is from left to right. No operators have precedence over others.
- GRAPL is block structured like ALGOL,
which allows a simple and efficient stacked storage management scheme.

- GRAPL programs are just character strings, so, like LISP, code can be written by other programs and executed. This technique is extremely powerful in GRAPL, because much of the GRAPL system is written in GRAPL to allow user modification. For example, in APL, all function editing is done by special function editing routines in a special function definition mode. Editing must be done a line at a time. Thus, simple tasks, such as changing all occurrences of the function name A to the name B, are made very time-consuming. In GRAPL, the function editing routines are written in GRAPL so that they are easily modified or rewritten to suit the user’s tastes.

- GRAPL has some pattern matching similar to SNOBOL4, which makes tasks such as program editing a lot simpler.

- GRAPL has a nice set of data types ranging from bit strings to integers to real numbers to three-dimensional points and lines. Needless to say, GRAPL is very good at computer graphics.

- As well as looping construct, there is a construct similar to a KEIL structure useful for computer aided instruction and other dialog.

- GRAPL programs are completely free form and, as in the case of FORTRAN, spaces are ignored. This allows programs to be formatted to make reading easier, or allows code to be compressed for efficient storage.

- When a program is executed, it is partially compiled and then executed interpretively. This is one of the fastest methods of execution.

- Errors are handled either by the user or by interrupt routines. Interrupts can be signaled in code or with a timer to allow for such things as concurrent processing and IO, or a limited form of multitasking.

- GRAPL retains the interactivity of APL.

I have been involved in the formal definition of GRAPL and its implementation on an IBM 370 for a year now, and am beginning a Z-80 version which I hope will fit in 24 K bytes of memory (including some space for user’s programs). GRAPL should prove to be not just a pacifier for people who want APL, but a distinct improvement with more general applications.

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BY THE NOVEMBER 1723
Concerning the APL articles in the August 1977 BYTE, I have not yet seen any mention of direct access file handling for APL. Since many small systems users are processing text, mailing lists, medical records, and scientific data, file searching on a floppy disk would seem to be of great importance.

In the past, the disk or tape access method software was generally cumbersome (and still is in languages like FORTRAN). Unfortunately, I am seeing the same mistakes made in the software development on microcomputers. I suggest taking a look at the virtual storage techniques used on systems like the IBM 370. A special access method called VSAM has been developed that allows data on disk or tape to be treated as if it were in programmable memory. Instead of giving a file record number, or track and cylinder address, one simply gives the address of the particular byte or block to be retrieved, and VSAM does the conversion to physical address. This also makes VSAM device independent!

My suggestion is this: instead of adding features to the interpreter (in the form of READ and WRITE commands as in FORTRAN) to handle direct access files, why not make the entire disk surface part of virtual memory. The available space will be the same as if the older direct access methods are used, but this gives the user the opportunity to store large files and data as arrays in memory. Thus one storage method is used and each disk surface can be treated as one large APL (or other language) workspace.

Since reference was made in one article to the difficulties of handling large arrays in user programmable memory, and the need for more than 20 K of memory to hold the interpreter and workspace, the use of a floppy disk as virtual memory could alleviate most of the problem. In fact, I used to work with APL on an IBM 1130 with one disk and only 8 K of core memory and almost all of the workspace was kept on disk. Most of the 8 K not used by the interpreter was used as temporary storage.

I hope that those who write the new APL interpreters will consider what the new technology has to offer before following the old designs.
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<td>3200</td>
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REMACHABLE MAGNETIC STORAGE MEDIA

Verbatim

Removable Magnetic Storage Media, manufactured by Information Terminals Corp.

<table>
<thead>
<tr>
<th>Name</th>
<th>Price</th>
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<tbody>
<tr>
<td>MiniDisks</td>
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<tr>
<td>MD205 1 (Soft Side)</td>
<td>29.95</td>
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<tr>
<td>MD205 10 (Hard Side)</td>
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<tr>
<td>MD205 16 (Hard Side)</td>
<td>29.95</td>
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<tr>
<td>Flexible Disks</td>
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<tr>
<td>FD34100 (Soft IBM)</td>
<td>9.99</td>
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<td>FD34100 (Hard Inner)</td>
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<td>FD65100 (Hard Outer)</td>
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<td>Flippky Disks</td>
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Digital Cassettes

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<tr>
<th>Name</th>
<th>Price</th>
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<tbody>
<tr>
<td>R200 Digital Direct</td>
<td>9.99</td>
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Circa 54 on inquiry card.

BYTE November 1977 227
A New Bar Code Scanner

Micro-Scan Corporation has announced a new bar code scanner designed to read bar code programs as featured in BYTE. The unit, called the Micro Scan, is capable of scanning varying contrast ratios (photostatic copies can be read) at rates of 10 to 36 inches (25 to 91 cm) per second. Documentation of loader programs for the 6800, 6502, 8080 and Z-80 processors are provided with each scanner. Power supply requirements are 11.5 to 18 V, unregulated. The Micro Scan is available for $97.50 from Micro Scan Corporation, POB 705, Natick MA 01760, (617) 655-5456.

A new conductive material with excellent sealing properties has been announced by Radcon Corporation, 246 Columbus Av, Rosele NJ 07203, (201) 241-5550. Free samples as well as a data sheet giving compression and electrical characteristics are available upon request. The material, called Multi-Con 2, is priced based on customers' applications. Please send for.

NEW! All IC's, sockets & hardware for WAMECO MEM-1 $144 Order PCBD separately below Special! 2102AL-4 1K x 1 ram less than $21.02 type rams, with power down, price of E2 200.32 ea 1.60, 64 ea 1.70 128 ea 1.60, 256 ea 1.50 9080A AMD 8080A Prime $20.00 B212745S12 Prime 4.00 B216 Prime 8.30 B216 Prime 4.95 B224 Prime 5.00 B228 Prime 8.90 B231 Prime 14.50 B235 Prime 14.50 1702A-4 AMD 4702 Prime 6.00 TMS-6001 UART Prime 9.95 2513 Char Gen Upper Prime 11.00 2513 Char Gen Lower Prime 11.00 1702A Intel Not Prime 4.00

An Unregulated DC Power Supply for Microprocessor(s)

A new DC power supply which provides unregulated power to microprocessors and peripheral equipment has been announced by Standard Power Inc. Designated the SMP-30B, the unit provides three voltages of 1 VDC at 1 A and 18 VDC at 0.5 A. It may be operated at 115 or 230 VAC, 50 or 60 Hz input.

Priced at $27.50 (single quantity), the unit measures 3 3/8 by 3 3/8 by 4 3/4 inches (8.57 by 8.57 by 12.1 cm) and weighs 2.1 pounds (0.95 kg).

Details are contained in Standard's Catalog C477, available on request from local distributors, or from Standard Power Inc, 1400 S Village Way, Santa Ana CA 92705, (714) 558-1172.

Circle 517 on inquiry card

Circ 518 on inquiry card

Circle 519 on inquiry card

Circle 520 on inquiry card

Attention APL Lovers...

MCM Computers is a Canadian firm which has been marketing small desk top APL machines for about five years. As this issue was going to press, we received word that the company is making available a $5000 package consisting of a complete self-contained computer with APL interpreter and dual cassette tape drives for work space. Contact the US office, 2125 Center Av, Fort Lee NJ 07048, (201) 944-2737.

Circle 521 on inquiry card

Circle 522 on inquiry card

Circle 523 on inquiry card

Circle 524 on inquiry card

Circle 525 on inquiry card

Circle 526 on inquiry card

Circle 527 on inquiry card

Circle 528 on inquiry card

Circle 529 on inquiry card

Circle 530 on inquiry card

Check or money order only. If you are not a regular customer and your order is large please send either a cashier's check or a postal money order, otherwise we will be a delay of two weeks for the check to clear. All items posted in the U.S. Gals. residents add 10% or $3.50. In Canada residents add 7%. Money back 30 day guarantee We C-WH0 1 accept unfumed IC's 1na1 clear All names post p&d 1n the US Cab!. r esidents add

419 Portofino Drive
San Carlos, California 94070
Please send for IC, Xistor and Computer parts list

WAMECO inc.

MEM-1 8KX8 fully buffered, S-100, uses 2102 type rams.
PCBD only $30 Mother Board 12 slot, terminated S-100, board only $30 10% discount on 10 or more of WAMECO PCBD in any combination

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PCBD only $30 Mother Board 12 slot, terminated S-100, board only $30 10% discount on 10 or more of WAMECO PCBD in any combination

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Please send for IC, Xistor and Computer parts list

WMC inc.
NEW BARGAINS

2708 PROM BOARD (10K) $59.95

Illustrated above is our 10K 2708 Board (2708)

Kit w/basic IC sockets. Any PROM addressable anywhere in memory map. ORDER AS C80-2708-2.

PROTOTYPE BOARDS

Prototype boards for the S-100 bus are available from many others—but only MINI MICRO MART supplies four different types. Two are wire-wrap versions and two are general-purpose DIP, for either point-to-point wiring. All boards come with a 5V regulator and a heat sink. The two “bus” versions are unique and have circuity etched on for buffering and address decoding, and include the decoders and necessary Tri-State buffers. (Illustrated below is the general-purpose DIP version, MODEL 01-2115.)

01-2115 GENERAL-PURPOSE DIP PROTOTYPE BOARD $18.95
01-2116 WIRE-WRAP PROTOTYPE BOARD ........... 19.95
01-2136 GEN-PURPOSE DIP BUS INTERFACE BOARD, incl. IC’s for address decoding and buffers ........... 29.95
01-2112 WIRE-WRAP BUS INTERFACE BOARD, incl. IC’s for address decoding and buffers ........... 30.95

BARE BOARDS

Bare boards for 8080 and Z-80 systems, as well as for 4K, 8K, and 16K static and dynamic memory boards—

BARE 4K S-100 MEMORY BOARDS, ........... ONLY $14.95

Add $2 for handling, shipping and insurance for each order (exception: Teletypes are shipped freight collect).

Send stamped, self-addressed envelope for details on any advertised items or for a copy of our catalog.

MINI MICRO MART has one of the largest selections of used, reconditioned, and rebuilt Teletypes in the U.S. — RO-33’s (printer only) ............... $395 to $595
KSR-33’s (keyboard & printer) ............... $495 to $695
ASR-33’s (prnt., keybd., reader & punch) ............... $695 to $895
Model 35 RO’s, KSR’s and ASR’s also available.

SURPLUS PERIPHERALS

MINI MICRO MART has a variety of surplus (new and used) items of interest to the hobbyist and commercial minicomputer user.

Our equipment list changes daily as we sell out of one item and add others. Among the items we currently have in stock are—

HIGH-SPEED PAPER TAPE PUNCHES: FACIT, BRPE, Digtronics, and others.
PRINTERS: Univac and others
HIGH-SPEED PAPER TAPE READERS: EECO, Digtronics, PERTEC TAPE UNITS
COGAR TAPE UNITS

We also have in inventory an item of interest to the homebrew builder — an electronic desk wired with line cord, line filter, circuit breaker, box fan, and card cage for 40 PC boards, new and used, from $49.95—up.

Write and get on our mailing list for these and other interesting surplus items.

PRIME COMPONENTS

2708 1K x 8 EPROM ............... $ 19.95
2716(TT) 2K x 8 EPROM ............... 39.95
Z-80’s (Zilog) ............... 29.95
8080A/AMD 9080A ............... 29.95
1702A’s (Intel/AMD) ............... 4.95
2102’s low power 450ns ............... 1.49

4K x 1 STATIC CHIPS (5V) 450ns for Heathkit and others boards ............... $ 8.49

MiniMicroMart
1618 James Street, Syracuse, N.Y. 13203, Phone: (315) 422-4467

Circle 94 on inquiry card.
Anyone who has an Altair 8800 series computer can now convert it to serve as the control center for a timesharing system. A special version of BASIC, called Timesharing BASIC, has been developed along with Altair Timesharing Disk BASIC Both are extensions of Altair extended BASIC and allow up to eight independent programs to be run simultaneously.

A memory partition technique is used to keep each program job in a unique area of memory. Each program area contains the BASIC program text, variable and string space, a workspace, plus approximately 300 bytes of the timesharing system. The system can be used with a variety of I/O devices including video displays and printers.

Control of a specific job may be transferred from one terminal to another with a single command. Various control characters allow suspension and resumption of each job without loss of data. Diagnostics are provided for program debugging and automatic line numbering is available during program entry. Both versions of Altair Timesharing BASIC furnish a line oriented text editor with line and character manipulation capabilities.

Extensive hardware is needed (in addition to the 8800 series mainframe and processor) to support both versions of Altair Timesharing BASIC. This includes a minimum of 32 K bytes of programmable memory, a vectored interrupt real time clock card, up to four 2510 serial interface boards for terminals and an optional line printer for the disk BASIC version. The disk version, of course, requires a floppy disk peripheral.

Contact MITS, 2450 Alamo SE, Albuquerque NM 87106.

A New General Purpose PC Board

Model H-PCB-1 is the first in a series of PC boards. The 4 by 4.5 by 1/16 inch (10.16 by 11.43 by .19 cm) board is made of glass coated epoxy laminate and features solder coated 1 oz copper pads and has a 22/22 two sided edge connector.

The board contains a matrix of .040 inch (.1 cm) diameter holes on .100 inch (.25 cm) centers. Two independent bus systems are provided for voltage and ground on both sides of the board. In addition, the component side contains 14 individual buses running the full length of the board which enable direct access from edge contacts to distant components.

Priced at $4.99 from OK Machine and Tool Corporation, 3455 Conner St, Bronx NY 10475, (212) 994-6600.

Attention Toronto Readers

Computer Mart in Toronto has been in operation since January 1977 and maintains at least three systems up and running for demonstration purposes. The store offers complete service facilities as well as programming services for microprocessor based systems. This includes operating system enhancements and accommodating unusual interface situations, both software and hardware. The store’s product line includes Processor Technology, Polymorphic, The Digital Group, Peripheral Vision, Cromemco, IMSAI, ICOM, IASIS, Lea-Siegler, North Star, TSC Software, Hitachi and Sanyo, Volker-Craig, Scientific Research, Sams, Hayden and AP Products, etc. Computer Mart’s policy is to provide the most effective guidance and general advice to our customers and continue this policy after the system is plugged in at the customer’s home. The store address is 1543 Bayview Av, Toronto, Ontario M4G 3B3 CANADA, (416) 484-9708.

A Small Shank Electric Drill from Wahl

Here is a device that should prove useful for the fabrication of printed circuit boards, as well as other applications involving the drilling and cleaning of small holes. The Wahl ISO-TIP electric drill is less than 5 inches (12.7 cm) long with drill bit removed and is designed to fit into tight corners. The on-off switch provides both intermittent and locked modes of operation, and the power cord is 10 feet (3.04 meters) long.

Operating at 9000 rpm, the drill is supplied with a collet chuck, three collets and two drill bits (#56 and #71). The unit is available in either 110 VAC or 12 VDC versions.

Contact the Wahl Clipper Corporation, 2902 Locust St, Sterling IL 61081 (815) 625-6525.

Data On the Cable?

OK Machine and Tool Corporation, 3455 Conner St, Bronx NY 10475, (212) 994-6600, has sent a picture of the new dual in line package cable termination assemblies, reselling at $3.75 to $4.35. Variations on this theme include double ended cables in lengths of 2, 4 and 8 inches (5, 10 and 20 cm) and single ended cables in lengths of 12 and 24 inches (30 and 61 cm); either 14 or 16 pin cables are available.

Circle 452 on inquiry card

Circle 451 on inquiry card

Circle 455 on inquiry card

Circle 453 on inquiry card

Circle 456 on inquiry card
A New Music System Program

Software Technology Corporation has announced the Music System, a hardware and software package designed to generate music by producing three simultaneous tones of fixed amplitude using a complex waveform which approximates the sound of a reed organ. These tones are generated using square waves, which are actually produced by a highly controlled pulsing of one of the Altair (S-100) bus status lines.

The Music System comes complete with a program on cassette tape, six sample selections, a user's manual and a circuit board with components.

Running in close to 2 K bytes of programmable memory, the program includes a monitor, text editor compatible with Processor Technology's ALS-8 file structure, and a high level music composing language compiler. Language capabilities include dotted notes, 4 octave range and staccato.

With the addition of a melody amplifier, speaker, cable and any Altair (S-100) bus computer, the Music System is ready to play. The price is $24.50. Contact Software Technology Corporation, POB 5260, San Mateo CA 94402, (415) 349-8080.

A Single Chip Stepper Motor Drive

North American Philips Controls Corporation, Cheshire Industrial Park, Cheshire CT 06410, (203) 272-0301, has introduced this integrated circuit stepper motor driver in a 16 pin dual in line package. The chip is intended to be used with 4 phase stepper motors which use 12 VDC and have 350 mA coils for each phase. This drive circuit includes the necessary logic to create motor motion in forward or reverse direction at rates determined by a clock input. The motors which North American Philips manufactures are listed in the brochure describing this part, and can typically provide working torque values in the 16 oz-in to 6 oz-in range with maximum stepping rates from 700 steps per second (lower torque motors) to about 200 steps per second (higher torque motors. TYPICAL SPECIFICATIONS FOR THE M.O.S. DRIVER ARE 7.5 and 15°. With gearing, this type of motor should prove quite useful for robotic mechanisms experiments. Price for the SAA1027 driver circuit is $4.75 in lots of 100.

Circle 473 on inquiry card.

New Additions to UPS
Uninterruptible Power Supply Family

National Upgrades SC/MP Electronics

Faster, lower power n channel metal oxide semiconductor versions of National Semiconductor Corp's SC/MP microprocessor are now available as retrofits for SC/MP kits. Called the SC/MP-II, the new 8 bit single chip device has all the features of the original p channel MOS version but will operate at twice the speed and will dissipate less than 200 milliwatts of power, about 25% of the power dissipated by the first SC/MPs introduced last year.

SC/MP-II requires only a +5 V supply, compared with the +5 and -12 V supplies required on earlier versions. Because of the +5 V only operation, the SC/MP-II can be interfaced with TTL and NMOS devices, and (by using pull up resistors) with CMOS devices.

The SC/MP-II microprocessor retrofit kit is available for $18.50. It includes the new SC/MP-II central processing unit (CPU), a 2 MHz crystal, a retrofit kit user's manual, an applications handbook, and a SC/MP-II data sheet. No software changes are required as long as the retrofit SC/MP-II runs at the same speed as its predecessor. Contact National Semiconductor at 2900 Semiconductor Dr, Santa Clara CA 95051.

Circle 471 on inquiry card.

No Transients Allowed

The Dyma AC Line Surge Protector is a suppressor and filter combination which is designed to protect equipment such as microprocessors and peripheral units from voltage transients on incoming power lines. The unit plugs directly into any standard AC outlet; equipment to be protected is plugged directly into the surge protector.

The 20A load model is priced at $49.95. Other ratings are available on special order. Contact Dyma Engineering, 213 Pueblo Del Sur, POB 1697, Taos NM 87571.

Circle 474 on inquiry card.
Olivetti P6060

- Brand New -
1. Fast efficient complier basic!
2. Twin full-size floppy disks!
3. 80 Char./Sec. Printer!
4. Full function 96-key keyboard!
5. Hassle-free maintenance (Olivetti)
6. 48k expandable to 80k!
7. Program chaining, strings variables
8. Matrix operations, plotting!
9. Output formats selected by program!
10. Complete integrated system

$8950 complete!
PLUG IN and USE

Warranted Cost-saving used peripherals

Olivetti 318

$875
Visitor tape reader/punch, electric type-
165 lb. Writer keyboard and 10-key numeric pad,
shipping standard paper/TAPE, OLIVETTI maintenance

Datapoint 2200-200 Console

This is a beautiful combination of
A univac 0769 printer, cabinet, and
Enough side space for an entire micro
System. It comes complete with power
Supply and PARALLEL INTERFACE, $495 30 char.

Datapoint 3300-200

Ideal small thermal 30cps printer
(NCR), PARALLEL ASCII, 80 COL, CRT
Compatible 5X7 dot matrix, solid-state, less than 25 moving parts,
96 characters, 110V.
$25 shipping $375

You can rely on
Computer Warehouse

"Your monitor arrived today and it
really adds to my system—no more
tired eyes!"
B.C., Philadelphia, Pa.

"I didn't expect your Centronics
printer would look and work so
well, thanks for a great deal!"
E.M., Columbus, Ohio

Centronics

For immediate shipment

Here are the choice printers that Systems houses, minicomputer
vendors, and top systems builders rely on for performance and
reliability! With thousands of these printers installed in the U.S.

101A...$1500
165 Char/Sec, 132 COL.
60 LPM, 2 CHANNEL VFU,
TTL, 8-BIT PARALLEL

102A...$2000
320 Char/Sec, 132 COL.
125 LPM, 2 CHANNEL VFU,
TTL, 8-BIT PARALLEL

103...$2000
165 Char/Sec, 132 COL.
70 LPM, L51, Boldface,
BIDIRECTION PRINTING,
INTERFACES FOR DEC, DG,
AND RS232 AVAILABLE

Looking for reliable small business system?
IBM System/3 and 1130 Systems...available now from our parent firm!
American Used Computer (617) 261-1100

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New Catalog
System Builders II

- Discounts up to 20%
- Wide range of microcomputers
- Super selection of good used
and cost saving peripherals!
- Over 250 books described and
ready to ship!
- In-detail descriptions of
hardware, kits, peripherals!
- Special selection of profes-
sional-grade computer systems!
- Microcomputer comparison chart!

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"Your monitor arrived today and it
really adds to my system—no more
tired eyes!"
B.C., Philadelphia, Pa.

"I didn't expect your Centronics
printer would look and work so
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E.M., Columbus, Ohio

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Here are the choice printers that Systems houses, minicomputer
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hardware, kits, peripherals!
- Special selection of profes-
sional-grade computer systems!
- Microcomputer comparison chart!

Send $1 today!!
Robot and Mechanism Hackers

Game Theory

Tired of Monopoly, Aggravation and Sorry? Looking for a game that teaches something about computers as well as being fun? Then try Computer Rage for a change. First of all it uses three dice, but they're binary dice, so you can move from zero to seven spaces per turn. There are priority interrupts, input and output channels with finite capacity, power failures, program bugs and branch points. Your objective is to get your three programs (shaped like miniature disk packs) from the input to the output weaving through a maze of program steps, checkpoints, IO queues, interrupts and decision points.

Computer Rage comes with a large (19 by 19 inch) game board, 12 playing pieces, three binary dice, 38 interrupt cards, rules and a booklet describing how to use the game as an educational tool. Recommended for ages 9 to adult, two to four players. Several playing variations are possible. Computer Rage is available for $8.95 postpaid from Creative Computing, attn: Pamela, POB 789-M, Morristown NJ 07960.

A Slick Dress for KIM-1

The Enclosures Group, 55 Stevenson St, San Francisco CA 94105, (415) 495-6925, has introduced this interesting enclosure for the KIM-1 product of MOS Technology. It should help to protect the circuit board of the KIM, especially during transit. The SKE 1-1 is available from stock in a variety of colors for $23.50.

3000 Hole General Purpose Prototyping Board

Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110, (714) 276-6911, announces the availability of a new general purpose prototyping board for use in the Micro-68 microprocessor systems. The 8 by 14.8 inch (20.3 by 37.6 cm) GP-2 board is Motorola Exorcisor bus compatible and has complete bus buffering already established using 8833 driver/receiver integrated circuits. The GP-2 board contains +5 V power and ground busing, 3000 holes worth of blank DIP patterns which allow for up to 35 large (24, 40 or 42 pin) DIP packages, or up to 107 small (14 or 16 pin) DIP packages. Price is $170, and they are said to be available from stock.

Here's an unusual item: Artisan Electronics has announced a new miniature solenoid designed with body dimensions equivalent to that of the TO-5 transistor case. Most applications for this TO-5 are for impulse duty, i.e. the generation of relatively high forces for short times or pulsed operations on intermittent duty. On such impulse duty, the average power should not exceed 0.6 W. Instantaneous power may be as high as 200 W, provided that the on time does not exceed 25 ms. At this duty, forces up to 50 grams may be generated at gaps of 0.100 inches (0.254 cm). For applications of continuous duty, the TO-5 solenoid will develop forces of from 1 to 10 grams with plunger travels up to .050 inches (0.025 cm). At this duty the solenoid is rated at ¾ W. A typical coil for operation on 12 VDC impulses would have a resistance of 1.5 W, pulsed at 12 VDC with a maximum on time of 25 ms and a minimum off time equal to 150 times the on time.

Contact Alan Seman, Artisan Electronics, 5 Eastmans Rd, Parsippany NJ, 07054, (201) 575-7684.

If you want to control things with a microprocessor system, boards like this product from Wintek, 902 N 9th St, Lafayette IN 47904, (317) 742-6802, will prove useful when applied with other products in the firm's line of modules. This photo shows the same board populated in two different ways to emphasize the fact that combinations of up to 16 output driver circuits or eight sensor inputs can be built on the same board, when ordered at a price of $69 plus $3 per driver and $12 per sensor. Drivers will handle up to 28 volts at 250 mA for use with relays, and sensors are optically isolated inputs for AC or DC voltages up to 240 V.

A Slick Dress for KIM-1

Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110, (714) 276-6911, announces the availability of a new general purpose prototyping board for use in the Micro-68 microprocessor systems. The 8 by 14.8 inch (20.3 by 37.6 cm) GP-2 board is Motorola Exorcisor bus compatible and has complete bus buffering already established using 8833 driver/receiver integrated circuits. The GP-2 board contains +5 V power and ground busing, 3000 holes worth of blank DIP patterns which allow for up to 35 large (24, 40 or 42 pin) DIP packages, or up to 107 small (14 or 16 pin) DIP packages. Price is $170, and they are said to be available from stock.

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Contact Alan Seman, Artisan Electronics, 5 Eastmans Rd, Parsippany NJ, 07054, (201) 575-7684.
D.R.C. ELECTRONICS

16K E-PROM CARD
S-100 (1MSA1/ALTaira) BUSS COMPATIBLE
IMAGINE HAVING 16K
OF SOFTWARE ON LINE AT ALL TIME!

KIT FEATURES:
1. Double sided PC Board with solder mask and silk screen layout.
2. Gold plated contact fingers.
3. All sockets included.
4. Phantom is jumper selectable to pin 67.
5. FOUR 7805 regulators are provided on card.

S-100
$24.95
with connector

COMPUTER GRADE CAP.
48.000 MFD 25 WVDC Mallory
$3.95
NEW!

T. I. ASCII CHARACTER GENERATOR
$3.50

MOTOROLA 7805R
VOLTAGE REGULATOR
Same as standard 7805 except 750 MA OUTPUT. TO-220. 5VDC OUTPUT.
$ .44 each
10 FOR $3.95

NATIONAL SEMI. MA1003 CAR CLOCK
Not a kit. Complete tested module. Works on 12 VDC, has on board time base. Sold by others at $24.95. Bright Green Digits. Same as used by Detroit in new cards.
$19.95

Z - 80 PROGRAMMING MANUAL
By MOSTEK. the major Z - 80 second source. The most detailed explanation ever on the workings of the Z - 80 CPU CHIPS. At least one full page on each of the 158 Z - 80 instructions. A MUST reference manual for any user of the Z - 80. 300 pages. Just off the press! A D.R.C. exclusive!
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8K LOW POWER RAM KIT!
USES 21L02-1 RAM'S.

4K STATIC RAM'S
NEW!
2114. The industry standard. 18 PIN DIP. Arranged as 1K X 4. Equivalent to FOUR 21L02's in ONE package! TWO chips give 1K X 8, with data.
$2 FOR $24
$450 N.S.

IC SOCKETS
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18 PIN — 4 FOR $1
22 PIN — 3 FOR $1

RCA HOUSE #2N3772
2 FOR $1

EDGECO NNECTOR — $1.50

TERMS: ORDERS UNDER $15 ADD $.75. NO C.O.D. WE ACCEPT VISA, MASTER CHARGE AND AMERICAN EXPRESS CARDS. MONEY BACK GUARANTEE ON ALL ITEMS. TEXAS RESIDENTS ADD 5% SALES TAX.

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Circle 50 on inquiry card.

BYTE November 1977 235
Andromeda's New Computer

Andromeda Systems has announced the Model 11/B, an LSI-11 based turnkey computer. The dual floppy system features 20 K by 16 bits of programmable memory and a 24 line video terminal with 80 characters per line. The terminal communicates with the computer via an R5232 interface at 9600 bps.

The 11/B uses the RT-11 operating system, the same system used by the Digital Equipment Corporation PDP-11 computer. It is designed for the single interactive user, although it can support up to eight users under multiuser BASIC (optional). System programs include a text editor, macroassembler, file manager and batch monitor. The user can choose from a variety of high level language options, including FORTRAN and FOCAL. The processor has a built-in floating point package.

The floppy disk system provides 512 K bytes of on line mass storage. A bootstrap loader program is built into the disk controller.

Contact Andromeda Systems, 14701 Armita St #1, Panorama City CA 91402, (213) 781-6000.

Circle 477 on inquiry card

EPA's Microcomputer and Floppy Disk

Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110, have announced a combined microcomputer and floppy disk system which uses the 6800 processor. The microcomputer is designated the Micro-68b and comes complete with 8K bytes of programmable memory, plus the Motorola MIKBUG monitor system, 20 mA current loop and RS-232 interfaces, and cassette interface. In addition, there is a built-in hexadecimal keyboard and LED display.

The Micro-68 floppy disk system is compatible with IBM standards and is available in either single or dual configurations. Both versions come complete with power supply and interface electronics.

The Micro-68b costs $1878; the single floppy disk system is $2595, and the dual version is $3295. Software available includes FORTRAN IV, BASIC, assembler language, an editor, and a floppy disk operating system.

Circle 480 on inquiry card

North Star's New Computer

North Star Computers Inc has announced the new North Star Horizon™ computer, which uses a full speed (4 MHz) Z-80 microprocessor and includes 16 K bytes of memory, a disk controller with one or two Shugart minifloppy™ disk drives, and full extended disk BASIC. A serial IO port is also provided.

Options include additional disk drives, hardware floating point arithmetic board, 24 line by 80 character display, lower case video display controller board, and 16 K memory board with parity check. The video display board, when used in conjunction with the 16 K memory board, will display high resolution (480 by 250 point) graphics on a video monitor. The Horizon computer uses the Altair (S-100) bus.

The single drive is $1599 in kit form and $1899 assembled. The dual drive is $1999 in kit form and $2349 assembled. Contact North Star Computers Inc, 2465 Fourth St, Berkeley CA 94710, (415) 549-0858.

Circle 478 on inquiry card

Attention London Computer Hackers

London's Computer Workshop has announced a new 4 terminal multiuser computer system including a printer and a BASIC compiler for under £3000. To obtain more information about this system, contact either Gordon Ashbee or John Burnett at the Computer Workshop, 174 Ifield Rd, London SW10 9AG, England, phone 01 373 8571.

Circle 479 on inquiry card

From RDA Inc comes news of the PRD11, an LSI-11 based microcomputer with the capacity for 56 K bytes of programmable memory and provisions for multiple terminal interfaces, a mass memory interface and a data acquisition subsystem. The entire unit weighs 23 pounds (10.43 kg) and is housed in an aluminum suitcase, a useful feature for the traveler.

Pictured with the PRD11 is a Computer Operations portable LINC tape mass memory compatible with the Digital Equipment Corporation's RT11 operating system. Software available includes a macroassembler, FORTRAN IV, multiuser BASIC, FOCAL and APL.

The PRD11 complete with 32 K bytes of programmable memory and a serial line interface is priced at $4,950. Contact RDA Inc, 5012 Herzel Pl, Beltsville MD 20705, (301) 937-2215.

Circle 476 on inquiry card

A Finished Product Concept

Vector Graphic Inc, 790 Hampshire Rd A-B, Westlake Village CA 91361, (805) 497-0733, has sent along this photo of the latest output of its design and production facility. This Vector 1+ is an Altair (S-100) bus computer product in an attractive cabinet, with provisions for the user to add a Shugart minifloppy™ (or equivalent) disk drive (not included), thus providing an integrated processor and mass storage combination rarely seen so far in the personal computing marketplace. Prices start at $659.

...4 on inquiry card

An LSI-11 Based Computer in a Suitcase

North Star Computer's New Computer

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APPLE II I/O BOARD KIT
Plugs Into Slot of Apple II Mother Board

FEATURES:
- 10 Bit Parallel Output Port (Expandable to 3 Ports)
- 1 Input Port
- 15mA Output Current Sink or Source
- TTL or CMOS Compatible
- Addressable anywhere in memory output area
- Can be used for peripheral equipment such as printers, floppy discs, cassettes, paper tapes, etc.

KIT INCLUDES:

PRICE:
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- 1 Input and 3 Output Ports for $64.00

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UNGAR SOLDERING IRONS

27W SOLDERING IRON KIT
Includes iron, 2 tips, roll of solder and iron stand $6.72

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3 DIGITS
A/D CONVERTER
Red or Green

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PUSH BUTTON SWITCH

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A FULLY PROGRAMMABLE SLIDE RULE
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- RPN logic with built-in hierarchy for increased speed and accuracy in calculating sequences involving arithmetic, trigonometric, logarithmic, power or exponential functions
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- Sine cosine tangent and inverse trigonometric functions
- Instant automatic calculation of powers and roots
- Instant conversions of radians to degrees or vice versa
- Square root and reciprocal calculations
- Pi change sign and register exchange keys
- Automatic recircuits
- Ability to automatically sum squares
- Storage memory
- Roll-down clear
- MOS LSI solid-state circuitry
- Engineered and manufactured by National Semiconductor Corp

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ONLY $63.00
ASCII KEYBOARD KIT

FURTHER IMPROVEMENTS, MORE FEATURES
- TTL Logic Circuits
- Power: +5V, 275mA
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- Full ASCII Set (Alpha Numeric, Symbols, Control)
- 7 or 8 Bits Parallel Data
- Optional Serial Output
- Selectable Positive or Negative Strobe, and Strobe Pulse Width
- 'N' Key Roll-Over
- Full Debounced
- Carriage Return Key
- Repeat Function Key
- Shift Lock, 2 Shift Keys
- 4 User Defineable Keys
- P.C. Board Size: 17-3/16" x 5"

OPTIONS:
- Metal Enclosure (Painted IBM Blue and White
- 18 Pin Edge Con. $2.00
- I.C. Sockets ... $4.00
- Serial Output (Shift Register) ... $2.00

KIT NUMBERS: Keyboard, P.C. Board, all required components and assembly manual.

NOTE: If you have this 63 Key Teletype Keyboard you can buy the Kit without it for $44.95.

FROM CONCORD
THE FIRST FULL FEATURE
LSI DMM KIT
INTRODUCTORY PRICE
$149.00

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- AUTO RANGING
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- AUTO ZERO
- 3 Large Digits (1/2"
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NI-CAD BATTERIES: $5.00
AC CHARGER: $4.95
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TEST LEADS: $2.95
SHUNT KIT FOR 3 CURRENT RANGES: $4.75

Minimum Order: $10.00

SHIPPING AND HANDLING
KEYBOARD, DMM and CALCULATOR: $3.50
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**What's New?**

**Gnat Leaps into Dual Minifloppy System**

The dual GNAT-PAC System 8 microcomputer is now available with dual minifloppy disk drive from Gnat Computer Inc., 1510 15th St., San Diego CA 92111. Each minifloppy has storage capacity of 80K bytes; operations include on-board data buffering, automatic seeking and initialization.

The system adds the dual disk System 8, and it comes equipped with the following features:

- 16K byte of programmable memory
- 2K byte of programmable read only memory (PROM) with space for an additional 32K byte
- Serial and parallel IO.
- Disk interface and controller.
- Hexadecimal front panel.

Software for the System 8 includes BASIC, monitor, bootloader, and disk operating system. The monitor and bootloader are PROM resident. The disk operating system features an assembler editor, and debugger with a test and debug capability. PL/M, BASIC, FORTRAN and other high level languages are available. Single unit price is $3690.

**A "Puzzling" New Development from Europe**

What's happening in Europe? One answer to the question is 15's new "Puzzle microprocessor system." Puzzle is a 6502 based system that uses European produced printed circuit boards and connectors. It consists of a printer, 16K bytes of read only memory, 4K bytes of programmable memory, and 1K bytes of programmable memory extension card, and an IO card.

For more information, contact Ing. Ernst Steiner, 1130 Wien, Linggasse 10 AUSTRIA, phone 82 26 74.

**Zilog Microcomputer Boards**

Zilog Inc. has introduced a family of Z80 based microcomputer boards to offer users a modular approach to building their own computing and processing systems.

The new MCB board series is designed with Z80 architecture. Each of the printed circuit boards is bus compatible and has direct interfaces with all of the boards in the series. All boards currently offered are available for delivery 30 days ARO.

Leading off the line is the Z80-MCB, a complete board, designed to operate as a single board computer, including its own 16K contained memory plus parallel and serial ports. The Z80-MCB provides 4K bytes of dynamic programmable memory plus up to 4K bytes of read only memory, or read only memory, or read only memory, or non volatile memory.

The Z80-MCB can be expanded to include more IO and memory, by adding other boards to the line. A strapping option allows users to put 16K bytes of dynamic programmable memory module in place of 4K by 1 bit programmable memory modules. Single unit price of the Z80-MC B is $495.

The Z80-MDC memory/disk controller board provides users with 12K bytes of dynamic or programmable memory, plus floppy disk controller. The board can handle up to eight floppy disk drives. The Z80-MDC has a strapping option for setting start address of each 1K byte page. Another feature is 1 bit cyclic redundancy check. Single unit price of 280-MDC is $795.

The 280-PMB PROM memory board provides up to 19K bytes of memory; jumpers allow each 1K byte of memory to reside in any segment of the 64K address space. The price is $395 for single units. Also included is the cost of program read only memory chips.

Also included in the MB series are the memory, microprocessor, and three interface boards. Standard card cages, connector boxes, and wire wrap boards are all available as options. For more information contact Dave West at Zilog 1005 Bubb Rd., Cupertino, CA 95014, 408 446-3666.

**Wintek Module Line**

Wintek Micro Modules is available with 16K bytes of memory, read only memory, read only memory, and read only memory, or non volatile memory. This unique line of modules includes: 16K bytes of memory, 1024 bytes of read only memory, 1024 bytes of read only memory, and 1024 bytes of read only memory. For more information contact Wintek, 2024 North 9th Street, Lafayette IN 47904, (317) 42-6802.

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*BYTE November 1977*
8Kx8 Econoram II single kit $163.84
3 kits - 24K1 $450

Low power Schottky

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74LS03 $0.30 74LS153 $1.38
74LS04 $0.33 74LS157 $0.95
74LS06 $0.36 74LS160 $1.40
74LS07 $0.36 74LS162 $1.60
74LS08 $0.33 74LS164 $1.20
74LS09 $0.30 74LS161 $1.30
74LS11 $0.33 74LS168 $1.87
74LS13 $0.36 74LS169 $1.67
74LS14 $0.30 74LS173 $1.65
74LS17 $0.30 74LS174 $1.25
74LS19 $0.33 74LS175 $1.15
74LS21 $0.33 74LS195 $1.30
74LS22 $0.33 74LS240 $1.88
74LS27 $0.30 74LS257 $1.25
74LS30 $0.39 74LS258 $1.25
74LS32 $0.36 74LS266 $0.33
74LS33 $0.36 74LS267 $0.33
74LS34 $0.45 74LS365 $0.33
74LS36 $0.45 74LS367 $0.33
74LS38 $0.45 74LS388 $0.33
74LS42 $0.98 80S50 $0.75
74LS47 $0.10 74LS366 $0.09
74LS48 $0.98 74LS98 $0.75
74LS49 $0.98 80S00 $0.95
74LS54 $0.50 74LS367 $0.50
74LS57 $0.68 80S07 $0.75
74LS57 $0.50 74LS368 $0.50
74LS58 $0.50 80S08 $0.50
74LS59 $0.50 74LS369 $0.50
74LS125 $0.63 74LS59 $0.63
74LS126 $0.63 81LS98 $0.63
74LS132 $1.25 81LS97 $1.25
74LS138 $1.10 81LS98 $1.10
74LS139 $1.15 81LS99 $1.15

25 PIN RS-232 CONNECTORS sub-
min 9 type... Male plug with 
plastic hood, part $0.95
Female jack part #03255 ...
$3.95

EDGE CONNECTORS: RS-100-1400T Gold plated solderable edge con-
ector, 0.140 spacing for Aliair Motherboards... 1/85, 5/202, 00
RS-1600T same but 0.200 spacing for IBM... 1/85, 5/202, 00
RS-1000W same but gold plated, 5 level wrap post: 1/85, 5/202, 00

MOTHERBOARD
10 Slots $90 18 Slots $124

Includes all edge connectors, plus active terminations to minimize crosstalk, noise, overshoot, and ringing that may be present with unterminated bus. Excel-
tent for stand-alone system, or add existing
Place ad $10 flat fee.

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HAVE OUR FLYER: 1) CMOS 2) LINEAR
3) MTR PROCESSES 4) POWER SUPPLIES
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PLAYS 8)结晶 9) VECTOR PRODUCTS
10) ENCLOSURES... ALL THE OTHER
THINGS WE CAN'T FIT INTO THIS SPAC

CIRCLE 61 OR INQUIRY CARD

FROM PARTS TO PERIPHERALS:
a one stop, mail order computer store,
serving computer enthusiasts since 1973.

Vector VBP Assembled Microcomputer Case

This adjustable packaging system for 5 100 bus microcomputers is compatible with AMSTRON and POLAR 1000 size cards. Outside, it is beautiful and, with the dark blue textured vinyl finish and lines unmarred by external weathering, it will provide years of service. Inside, there is space for 2 cards total (on 0.75" center) with a fully adjustable interior card mounting system (card guides and hard ware provided for 12 cards) The interior instantly accessible, the rear and front panels are removable and recessed. If you want a lassy home for your micro, check this out...it is the best we have seen.

VP2 ASSEMBLED MICROCOMPUTER CASE...

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STATE 3 TERMINAL CRYSTALS $4.95 each (all frequencies in Kc)
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500 KHz, series mode, fundamental, H61/U package, wire Leads 5.0 9.0 15.0 20.0 25.0 30.0
1 MR, series mode, fundamental, wire leads in 500 KHz package $5.95 each for 2 MHz, series mode, fundamental, wire leads in 560 KHz package...

ACTIVE TERMINATOR $29.50
Plug into any $100 Motherboard whose bus lacks active terminations

Music spoken here

Many if you are into music with your computer, some people generate sounds within the machine itself, others use them to control synthesizer hardware. Where we come in is the line of our music-Kit assaults designed by Craig Anderton, writer for Guitar
Popular Electronic's Contemporary Keyboard, and others. Music-Kits contain a circuit board, electronic components, and pots; user supplies case and hardware.

few are in...some you might like are the 8 In, 1 Out Mixer ($18, $20) which can mix up to 8 inputs to a common output, the Super Tone Control ($27, $10.50), a low noise, state variable filter that gives high, low, and bandpass outputs, a Reverberation Unit ($22, $13.00 less springs) for adding concert hall sound and acoustic depth. Want to know more? Check our flyer.

GOMBOU

Circle 61 on inquiry card
The new development is the TMS-9900 architecture. Inclusion of direct logic into the selection logic allows direct switches to be used in the board. The board uses a TMS-4051 dynamic memory chip which is 4 K by 16 bit words. These memory parts have a sufficiently fast response time to allow the 9900 to run at its maximum speed of 3.3 MHz clock. A fully populated 32 K byte version of the board sells under part number TEC9900-MA-32KB for $799 assembled and tested. (At the price of 3 cents/bit installed, who can haggle?) This is a very desirable item for the homebrewer willing to supply the finishing touches to a 16 bit minicomputer with 32 K bytes of memory. The economics can be summarized as follows:

- TEC-9900-55 Processor: $399
- TEC-9900 + ancillaries:
  - TEC-9900-MA-32KB Memory: $799
  - TEC-9900-PP Power supply: $149
- Total: $1347

To these assembled and tested module prices one should add the cost of a serial ASCII terminal, a cabinet or chassis in which to mount the equipment (homebrew style), and any mass storage required to complete the system.

A phone conversation with the firm at the time this note was being written (July 5 1977) brought out the fact that forthcoming additions to the line are a video and audio cassette interface board (TEC-9900-VA), and a floppy disk controller, both of which were expected to be available in the fourth quarter of 1977.

Memory Module from MIT

Motorola has sent along this photo and block diagram of a new addition to their M10800 family of high speed MECL 10,000 current mode logic. This family of logic is used in the highest speed contemporary processors, and due to the difficulties of designing with transmission line interconnections, tends to be ignored by experimenters favoring slower TTL logic. Illustrating the way future packaging trends are going, this MC10803 memory interface processor is mounted in a so-called "quad in line" (QUIL) package with four rows of 12 pins for 48 pins total.

Its internal logic, shown in the background, includes six 4 bit registers, an arithmetic logic unit (with encoded selections of function and operands) and data transfer circuitry. Its intended use is as a node in a large machine, dedicated to memory and peripheral operations. An example is performing the tasks of direct memory access control where intelligent programming is useful, but the versatility of a main processor is not needed.

The high speed nature of this device and its price ($40 in 100 quantity) say that this chip will be of most interest to those individuals designing new products subject to high performance specifications. For more information contact Jerry Tonn at Motorola Semiconductor Products, POB 20912, Phoenix AZ 85036, (602) 962-2515.

Attention Microprogrammed Computer Designers

RDA Inc., 5012 Herzl Pl., Beltsville MD 20705, (301) 937-2215, has sent along this picture of an LSI-11 option (Digital Equipment Corporation) which requires two slots of an LSI-11's backplane and provides 8 K bytes of storage using 2708s as memory elements. The memory is set up for selectable addressing. Power requirements are 1 A on each of three voltages: +5 V, -5 V and -12 V when all sixteen 2708 memories are plugged into the circuit in the empty sockets shown in the photo. (A separate programming device is required since this board does not include a built-in programmer.) Exclusive of the 16 memory chips, the price of this board is $285. Assuming a current mail order price of $35 for each 2708, fully stuffing the board will cost $560.

An LSI-11 EROM Board

MindTech, Inc. has just sent along an exciting new development for those readers interested in opting for the Texas Instruments TMS-9900 architecture. The firm manufactures a TMS-9900 based processor board, shown at the top in this photo. The new development is the board at the bottom, the TEC-9900-MA dynamic memory board which has a capacity of up to 32 K bytes (16 K 16 bit words) and plugs directly into the previous TEC-9900-SS product. The new board measures 7 by 16 inches (17.8 by 40.6 cm) and includes all the necessary refresh and control circuitry. Address selection logic allows 8 bit switches to specify any starting address for the 32 K byte region in 1 K address increments. The board uses Texas Instruments TMS-4051 dynamic memory chips which are organized 4 K by 1 bit. As a result, the board can be populated with any increment of 4 K 16 bit words. These memory parts have a sufficiently fast response time to allow the 9900 to run at its maximum speed of 3.3 MHz clock. A fully populated 32 K byte version of the board sells under part number TEC9900-MA-32KB for $799 assembled and tested. (At the price of 3 cents/bit installed, who can haggle?) This is a very desirable item for the homebrewer willing to supply the finishing touches to a 16 bit minicomputer with 32 K bytes of memory. The economics can be summarized as follows:

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An LSI-11 EROM Board
### DIODES/ZENERS

<table>
<thead>
<tr>
<th>Code</th>
<th>Value</th>
<th>Type</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>1N914</td>
<td>100v 10mA</td>
<td>.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N4005</td>
<td>600v 1A</td>
<td>.08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N4007</td>
<td>1000v 1A</td>
<td>.15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N4148</td>
<td>75v 10mA</td>
<td>.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N753A</td>
<td>6.2v</td>
<td>.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N758A</td>
<td>10v</td>
<td>.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N759A</td>
<td>12v</td>
<td>.12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N4733</td>
<td>5.1v 1.5</td>
<td>.26</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N5243</td>
<td>13v</td>
<td>.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N5244B</td>
<td>14v</td>
<td>.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1N5245B</td>
<td>15v</td>
<td>.25</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SOCKETS/BRIDGES

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-pin</td>
<td>PCB</td>
<td>.25</td>
<td></td>
</tr>
<tr>
<td>14-pin</td>
<td>PCB</td>
<td>.25</td>
<td></td>
</tr>
<tr>
<td>18-pin</td>
<td>PCB</td>
<td>.25</td>
<td></td>
</tr>
<tr>
<td>22-pin</td>
<td>PCB</td>
<td>.45</td>
<td></td>
</tr>
<tr>
<td>24-pin</td>
<td>PCB</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>28-pin</td>
<td>PCB</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>40-pin</td>
<td>PCB</td>
<td>.50</td>
<td></td>
</tr>
</tbody>
</table>

### TRANSISTORS, LEDS, etc.

<table>
<thead>
<tr>
<th>Code</th>
<th>Type</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>2N2222</td>
<td>NPN (Plastic)</td>
<td>.15</td>
<td></td>
</tr>
<tr>
<td>2N2907</td>
<td>PNP</td>
<td>.15</td>
<td></td>
</tr>
<tr>
<td>2N3906</td>
<td>PNP</td>
<td>.10</td>
<td></td>
</tr>
<tr>
<td>2N3054</td>
<td>NPN</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>2N3055</td>
<td>NPN 15A 60v</td>
<td>.50</td>
<td></td>
</tr>
<tr>
<td>TP125</td>
<td>PNP</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>D.L.747</td>
<td>7seg 6/8&quot; high common-anode</td>
<td>1.05</td>
<td></td>
</tr>
<tr>
<td>XAN72</td>
<td>7seg common-anode</td>
<td>1.50</td>
<td></td>
</tr>
<tr>
<td>FND 359</td>
<td>Red 7 seg comm-cathode</td>
<td>1.20</td>
<td></td>
</tr>
</tbody>
</table>

### C MOS

<table>
<thead>
<tr>
<th>Code</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>4000</td>
<td>.15 7400</td>
<td>.15</td>
</tr>
<tr>
<td>4001</td>
<td>.20 7401</td>
<td>.15</td>
</tr>
<tr>
<td>4002</td>
<td>.20 7402</td>
<td>.20</td>
</tr>
<tr>
<td>4004</td>
<td>.95 7404</td>
<td>.20</td>
</tr>
<tr>
<td>4006</td>
<td>.95 7406</td>
<td>.95</td>
</tr>
<tr>
<td>4007</td>
<td>.35 7407</td>
<td>.25</td>
</tr>
<tr>
<td>4008</td>
<td>.95 7408</td>
<td>.15</td>
</tr>
<tr>
<td>4009</td>
<td>.90 7409</td>
<td>.10</td>
</tr>
<tr>
<td>4010</td>
<td>.45 7410</td>
<td>.10</td>
</tr>
<tr>
<td>4011</td>
<td>.20 7411</td>
<td>.25</td>
</tr>
<tr>
<td>4014</td>
<td>.10 7414</td>
<td>.30</td>
</tr>
<tr>
<td>4015</td>
<td>.95 7415</td>
<td>.45</td>
</tr>
<tr>
<td>4016</td>
<td>.35 7416</td>
<td>.10</td>
</tr>
<tr>
<td>4017</td>
<td>1.10 7417</td>
<td>.25</td>
</tr>
<tr>
<td>4018</td>
<td>1.10 7418</td>
<td>.50</td>
</tr>
<tr>
<td>4019</td>
<td>.60 7419</td>
<td>.10</td>
</tr>
<tr>
<td>4020</td>
<td>.85 7420</td>
<td>.15</td>
</tr>
<tr>
<td>4021</td>
<td>1.35 7421</td>
<td>.45</td>
</tr>
<tr>
<td>4022</td>
<td>.95 7422</td>
<td>.15</td>
</tr>
<tr>
<td>4023</td>
<td>.25 7423</td>
<td>.30</td>
</tr>
<tr>
<td>4024</td>
<td>.25 7424</td>
<td>.35</td>
</tr>
<tr>
<td>4026</td>
<td>1.95 7426</td>
<td>.25</td>
</tr>
<tr>
<td>4027</td>
<td>.50 7427</td>
<td>.15</td>
</tr>
<tr>
<td>4028</td>
<td>.95 7428</td>
<td>.45</td>
</tr>
<tr>
<td>4030</td>
<td>.95 7430</td>
<td>.85</td>
</tr>
<tr>
<td>4031</td>
<td>.50 7431</td>
<td>.95</td>
</tr>
<tr>
<td>4033</td>
<td>2.50 7433</td>
<td>.65</td>
</tr>
<tr>
<td>4035</td>
<td>1.25 7435</td>
<td>.65</td>
</tr>
<tr>
<td>4040</td>
<td>1.35 7440</td>
<td>.95</td>
</tr>
<tr>
<td>4041</td>
<td>.69 7441</td>
<td>.70</td>
</tr>
<tr>
<td>4042</td>
<td>.95 7442</td>
<td>.25</td>
</tr>
<tr>
<td>4044</td>
<td>.95 7444</td>
<td>.85</td>
</tr>
<tr>
<td>4046</td>
<td>1.75 7446</td>
<td>.25</td>
</tr>
<tr>
<td>4048</td>
<td>.70 7448</td>
<td>.40</td>
</tr>
<tr>
<td>4050</td>
<td>.95 7450</td>
<td>.40</td>
</tr>
<tr>
<td>4052</td>
<td>.40 7452</td>
<td>.40</td>
</tr>
</tbody>
</table>

### TTL

<table>
<thead>
<tr>
<th>Code</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>74117</td>
<td>.25</td>
<td></td>
</tr>
<tr>
<td>74180</td>
<td>.85</td>
<td></td>
</tr>
<tr>
<td>74181</td>
<td>2.25</td>
<td></td>
</tr>
<tr>
<td>74182</td>
<td>.95</td>
<td></td>
</tr>
<tr>
<td>74190</td>
<td>1.75</td>
<td></td>
</tr>
<tr>
<td>74191</td>
<td>1.35</td>
<td></td>
</tr>
<tr>
<td>74192</td>
<td>1.65</td>
<td></td>
</tr>
<tr>
<td>74194</td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>74195</td>
<td>.95</td>
<td></td>
</tr>
<tr>
<td>7508A</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>75100</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>75110</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>75491</td>
<td>.50</td>
<td></td>
</tr>
<tr>
<td>75492</td>
<td>.50</td>
<td></td>
</tr>
<tr>
<td>75493</td>
<td>.50</td>
<td></td>
</tr>
<tr>
<td>75120</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75123</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75124</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75125</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75126</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75127</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75128</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75129</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75130</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75131</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75132</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75133</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75134</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75135</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75136</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75137</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75138</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75139</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75140</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75141</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75142</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75143</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75144</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75145</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75146</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75147</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75148</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75149</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75150</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75151</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75152</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75153</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75154</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75155</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75156</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75157</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75158</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75159</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75160</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75161</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75162</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75163</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75164</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75165</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75166</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75167</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>75168</td>
<td>.65</td>
<td></td>
</tr>
</tbody>
</table>

### MEMORY CLOCKS

<table>
<thead>
<tr>
<th>Code</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>74S182 (8223)</td>
<td>3.00</td>
<td></td>
</tr>
<tr>
<td>1702A</td>
<td>6.95</td>
<td></td>
</tr>
<tr>
<td>MM5314</td>
<td>3.00</td>
<td></td>
</tr>
<tr>
<td>MM5316</td>
<td>3.50</td>
<td></td>
</tr>
<tr>
<td>2102-1</td>
<td>1.75</td>
<td></td>
</tr>
<tr>
<td>2102L-1</td>
<td>1.95</td>
<td></td>
</tr>
<tr>
<td>TR 1602B/1602C</td>
<td>6.95</td>
<td></td>
</tr>
<tr>
<td>TMS 6011</td>
<td>6.95</td>
<td></td>
</tr>
<tr>
<td>8080AD</td>
<td>15.00</td>
<td></td>
</tr>
<tr>
<td>BT13</td>
<td>1.50</td>
<td></td>
</tr>
<tr>
<td>BT23</td>
<td>1.50</td>
<td></td>
</tr>
<tr>
<td>BT24</td>
<td>2.00</td>
<td></td>
</tr>
<tr>
<td>21078-4</td>
<td>4.95</td>
<td></td>
</tr>
</tbody>
</table>

### LINES, REGULATORS, etc.

<table>
<thead>
<tr>
<th>Code</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>2N3904</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>2N3906</td>
<td>.10</td>
<td></td>
</tr>
<tr>
<td>2N3054</td>
<td>.35</td>
<td></td>
</tr>
<tr>
<td>2N3055</td>
<td>15A 60v</td>
<td>.50</td>
</tr>
<tr>
<td>TP125</td>
<td>PNP</td>
<td>.35</td>
</tr>
<tr>
<td>LM739</td>
<td>1.50</td>
<td></td>
</tr>
<tr>
<td>LM739 (8-14)</td>
<td>.25</td>
<td></td>
</tr>
<tr>
<td>LM747</td>
<td>1.10</td>
<td></td>
</tr>
<tr>
<td>LM1307</td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>LM1458</td>
<td>.95</td>
<td></td>
</tr>
<tr>
<td>LM3900</td>
<td>.50</td>
<td></td>
</tr>
<tr>
<td>LM75451</td>
<td>.65</td>
<td></td>
</tr>
<tr>
<td>NE656</td>
<td>.50</td>
<td></td>
</tr>
<tr>
<td>NE666</td>
<td>.95</td>
<td></td>
</tr>
<tr>
<td>NE666</td>
<td>1.75</td>
<td></td>
</tr>
<tr>
<td>NE667</td>
<td>1.35</td>
<td></td>
</tr>
</tbody>
</table>

### INTEGRATED CIRCUITS UNLIMITED

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### SPECIAL DISCOUNTS

<table>
<thead>
<tr>
<th>Code</th>
<th>Total Order</th>
<th>Deduct</th>
</tr>
</thead>
<tbody>
<tr>
<td>$35</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$55</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$100</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$300</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$1000</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Circle 70 on inquiry card.
An EROM Programmer

MicroPeripherals, 24 Matford Close, Westbury on Trym, Bristol BS10 6LR ENGLAND, has announced this programmer for the popular erasable read only memories with part numbers 2704, 2708 and 2716. The product will program a 1 K chip in 2.5 minutes, a process which includes setting up the programmed pattern and verifying the pattern. The programmer is intended to be used with the user's processor as a peripheral, and comes in several models. The basic model is intended for use with 2704 (1/2 K bytes) and 2708 (1 K bytes) parts, borrowing power from the user's system. This model is priced at $199. The larger models feature built-in power supplies and manual operations via switches and LED readouts.

Circle 486 on inquiry card

Nonvolatile to the Core

For the first time, to our knowledge, a product has been designed for the Altair (S-100) bus which provides core memory for a personal computer system. The product is Micro Memory Inc's MM-S100 8 K by 8 bit programmable memory card. Of what use is a magnetic core memory in an age of semiconductor circuits? Nonvolatility is the answer. With a core memory, magnetic storage of data is involved, a technology which is not dependent upon continuous application of power. Turn off the power on a core memory, and it will retain its pattern unaltered "forever." Turn on the power and the active circuits, and it is functionally like any semiconductor programmable memory. This core memory card thus combines the nonvolatility of a read only memory with the programmability of dynamic or static semiconductor memories.

The MM-S100 unit plugs directly into the Altair (S-100) bus, and has the circuitry needed: timing, control logic, decode logic, drive circuits, address and data latches, power regulators, etc. It runs with a 1.0 µ; cycle time so that no wait states are needed with a standard 8080 clock rate. The price is $650 from Micro Memory Inc, 9438 Irodale Av, Chatsworth CA 91311, (213) 998-0070.

Circle 487 on inquiry card

At the Frontiers of Silicon Technology

This electron microscope image shows a new American Microsystems Inc. VMOS process memory device with a human hair juxtaposed on top of it. The magnification factor is on the order of 10,000 times the actual size. The V in VMOS is emphasized by the V-shaped slots in the structure of the devices. The part design from which this enlargement was made (the S4015-3 integrated circuit) is a new commercial volatile memory product which has an extremely fast access time (45 ns) and 1 K by 1 bit static operation. The product is intended for use with fast random access scratch pads, buffers, cache memories, etc. For those implementing microprogrammed machines on an experimental basis, this memory will prove ideal in a control store matched to the characteristics of the TTL bit slice parts such as the 2900 and the Texas Instruments' 745481 family. American Microsystems Inc is located at 3800 Homestead Rd, Santa Clara CA 95051, (408) 246-0330.

Circle 488 on inquiry card
### MICROCOMPUTER

<table>
<thead>
<tr>
<th>SUPPORT DEVICES</th>
<th>8212</th>
<th>4.00</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>8214</td>
<td>12.95</td>
</tr>
<tr>
<td></td>
<td>8216</td>
<td>5.25</td>
</tr>
<tr>
<td></td>
<td>8224</td>
<td>6.00</td>
</tr>
<tr>
<td></td>
<td>8228</td>
<td>9.25</td>
</tr>
<tr>
<td></td>
<td>8238</td>
<td>8.20</td>
</tr>
<tr>
<td></td>
<td>8251</td>
<td>12.00</td>
</tr>
<tr>
<td></td>
<td>8253</td>
<td>28.00</td>
</tr>
<tr>
<td></td>
<td>8255</td>
<td>12.00</td>
</tr>
<tr>
<td></td>
<td>8257</td>
<td>22.00</td>
</tr>
<tr>
<td></td>
<td>8259</td>
<td>22.00</td>
</tr>
</tbody>
</table>

#### 6800 SUPPORT

<table>
<thead>
<tr>
<th>SUPPORT DEVICES</th>
<th>6810P</th>
<th>6.00</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6820P</td>
<td>8.00</td>
</tr>
<tr>
<td></td>
<td>6828P</td>
<td>9.60</td>
</tr>
<tr>
<td></td>
<td>6834P</td>
<td>21.95</td>
</tr>
<tr>
<td></td>
<td>6850P</td>
<td>12.00</td>
</tr>
<tr>
<td></td>
<td>6852P</td>
<td>17.00</td>
</tr>
<tr>
<td></td>
<td>6860P</td>
<td>15.00</td>
</tr>
<tr>
<td></td>
<td>6862P</td>
<td>18.00</td>
</tr>
<tr>
<td></td>
<td>6880P</td>
<td>2.70</td>
</tr>
</tbody>
</table>

#### Z80 SUPPORT

<table>
<thead>
<tr>
<th>SUPPORT DEVICES</th>
<th>3881</th>
<th>15.95</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3882</td>
<td>15.95</td>
</tr>
<tr>
<td></td>
<td>3851</td>
<td>14.95</td>
</tr>
<tr>
<td></td>
<td>3852</td>
<td>14.95</td>
</tr>
</tbody>
</table>

#### FLOPPY DISC CONTROLLER

<table>
<thead>
<tr>
<th>PD317D</th>
<th>65.00</th>
</tr>
</thead>
<tbody>
<tr>
<td>1771</td>
<td>69.95</td>
</tr>
</tbody>
</table>

#### DYNAMIC RAMS

| 4140 (16P) | 5.50  |
| 1103 (16P) | 1.50  |
| 2104 (16P) | 6.50  |
| 21078 (22P)| 4.50  |
| 21078-4 (22P)| 4.00  |
| TMS4050 (16P)| 4.50  |
| TMS4056 (22P)| 4.50  |
| 4096 (16P)| 5.50  |
| MM5262 (22P)| 3.00  |
| MM5270 (18P)| 5.00  |
| MM5280 (22P)| 6.00  |

#### STATIC RAMS

| 31001 | 2.00  |
| 91111A | 4.25  |
| 91112A | 4.25  |
| 1101A | 1.00  |
| 2101 | 3.00  |
| 2102 (16S) | 1.25  |
| 2102 (15K) | 1.50  |
| 212A-4 | 4.45  |
| 2112A-4 | 3.00  |
| 25018 | 1.45  |
| 3103 | 2.95  |
| 4020A (2560S) | 13.75  |
| 4100 (2000S) | 11.95  |
| 4804 | 20.00 |
| 9173 | 20.00 |
| 745201 | 4.75 |
| 748201 | 7.00 |
| 7489 | 2.25 |
| 8225 | 1.50 |
| 8599 | 1.50 |
| 82509 | 9.00 |

#### DYNAMIC RAMS

| 14140AN | 3.00  |
| 1404AN | 3.00  |
| 2405 | 4.95  |
| 2505K | 3.00  |

#### SHROTT REGISTERS

| DYNAMIC | 1404AN | 3.00  |
| 1404AN | 3.00  |
| 2405 | 4.95  |
| 2505K | 3.00  |

#### MISC OTHER COMPONENTS

| NH0025CN | 1.75  |
| NH0026CN | 3.00  |
| N8720 | 4.00  |
| N826 | 3.25  |
| N8197 | 1.45  |
| 74367 | 1.00  |
| 74089 | 1.00  |
| 1488 | 1.95  |
| 1489 | 1.95  |
| 3205 | 6.20  |
| 3207A | 2.50  |
| C-3404 | 3.95  |
| P-3408A | 6.75  |
| P-4201 | 4.95  |
| MM-5320 | 7.50  |
| MM-5369 | 2.00  |
| DM-8130 | 3.00  |
| DM-8131 | 2.50  |
| DM-8831 | 2.50  |
| DM-8813 | 2.50  |
| MM-8135 | 2.50  |
| SN74LS367 | 1.00  |
| SN74LS368 | 1.00  |

#### PROM'S

| 1702A | 5.00  |
| 1702AL | 7.00  |
| 2704 | 20.00  |
| 2705 | 24.00  |
| 2716 | 75.00  |
| 3601 | 4.50  |
| 52030A | 7.00  |
| 52040A | 10.00  |
| 6834 | 21.95  |
| 6834-1 | 16.95  |
| 825238 | 4.00  |
| 82520B | 4.25  |
| 8223B | 4.00  |

### JADE Z80 KIT

- **S-100 COMPATIBLE**
- **-with PROVISIONS for ONBOARD 2708 and POWER ON JUMP**

**$135.00 EA.**

### JADE CO

- **Electronics for the Hobbyist and Experimenter**
- **5351 WEST 144TH STREET, LAWNDALE, CALIFORNIA 90260**
- **(213) 679-3313**

Discounts available at OEM quantities. Add $1.25 for shipping. California residents add 6% sales tax.

### Assembled & Tested

**8K Static RAM Board**

| 250ns. | $209.95 |
| 350ns. | $199.95 |
| 450ns. | $189.95 |

- **WILL WORK WITH NO FRONT PANEL**
- **FULL DOCUMENTATION**
- **FULLY BUFFERED**
- **$100 DESIGN**
- **ADEQUATELY BYPASSED**
- **LOW POWER SCHOTTKY SUPPORT IC'S**

**$169.95**

**$149.95**

**$139.95**
Motorola's New HEP Catalog

Motorola has announced its new cross reference guide and catalog describing the HEP line of semiconductor products. HEP products are designed primarily for hobbyists, experimenters, professional service technicians and dealers and consist of replacements for a large number of transistors, thyristors, diodes and FETs, as well as RTL, HTL, DTL, TTL and CMOS integrated circuits and linear devices. The catalog costs $2 and is available from the Motorola Technical Center, Motorola Semiconductor Products Inc, POB 20294, Phoenix AZ 85036, (602) 244-6900.

Circle 456 on inquiry card.

IEEE Offers Microprocessor Talks on Cassette

A recording of three talks given at a tutorial "How to Use Microprocessors" held at Stanford University in the Spring of 1976 is available on standard magnetic tape cassettes for $5 from the IEEE. The talks are by Dr. Robert Noyce, chairman of the board, Intel Corporation, Floyd Kvamme, vice president, National Semiconductor, and Dr. Adam Osborne, president, Osborne Associates.

Topics covered include future developments in microprocessors, the business aspects of producing them, and which of the current microprocessors is most suited to particular hardware requirements. The tutorial was sponsored by the IEEE Computer Society, the Electron Devices and the Reliability Groups, Santa Clara (Silicon) Valley Section.

To obtain your copy of the cassette tape, send a check for $5 to the IEEE Section Office, 701 Welch Rd, Palo Alto CA 94304. Notes on the blackboard presentations and view graphs of the speakers will be included.

Circle 457 on inquiry card.

Is the Dragon a Phoenix?

The theme of rebirth and renewal is a very real one, as exemplified by Phyllis Cole's transformation of People's Computers from a newspaper format tabloid (hard to keep track of) into the 64 page (including covers) saddle stitched publication shown in its May-June 1977 form in this photo. People's Computers is published bimonthly by People's Computer Company, 1263 El Camino Real, Box E, Menlo Park CA 94025. PCC is a tax-exempt, nonprofit corporation and donations are said to be tax-deductible. Subscriptions are $8 per year in the US. Single copy price is $1.50.

The editorial flavor which Phyllis brings to this publication is that of commentary on what's happening, light software, background information on computing and related peripheral issues. It is a magazine intended to be readable and enjoyable for the neophyte. (Our resident noncomputer people at BYTE grabbed the first issue so quickly that it became difficult to find a copy from which to abstract this short review.) Some titles from the first issue received here in the new format include:

Home Computing: An Introduction for Novices
Once Upon a Fair
Computers and Copyright Law
Women and Computers: A Dialogue
The Dot and the Line
Stock Market Simulations
BASIC Mortgages
Exagon
Women and Math Projects:
Lawrence Hall of Science
Space Colony: Living In a Garden of Illusions
Fortran Man
More Tiny BASIC
Make Believe Computers
Pilot
The Data Handlers Users Manual, Part 3
Announcements
Letters

It is an interesting and positive transformation which should be sampled to be believed...CH

Circle 458 on inquiry card.

A Special Free Offer from Radio Shack

Radio Shack is offering five free copies of their new Archer Semiconductor Reference Handbook to any interested organization.

The 128 page handbook, which normally sells for $1.95, lists over 36,000 replacement transistors, diodes and other devices, and includes a cross-reference guide, sections on the care and handling of transistors, soldering precautions, how to test transistors, and a glossary.

To get five free copies of the handbook, write on your club's stationery to Radio Shack, Dept SRH, 2617 W 7th St, Fort Worth TX 76107.

Circle 459 on inquiry card.

Home Computer Books Available

Dillithium Press has a new brochure detailing their computer books, all of which are slanted toward the home computer hacker. Beginner's books as well as more advanced books are included in the list, available for free from Dillithium Press, POB 92, Forest Grove OR 97116.

Circle 460 on inquiry card.

Fenwal Offers a New Thermistor Manual

Many people who read BYTE are interested in microcomputer applications involving temperature measurement. One way to monitor temperatures is with a thermistor. Fenwal Electronics is making available a free 34 page thermistor manual containing a variety of temperature coefficient tables, resistance temperature tables and so on. Contact Fenwal Electronics, 63 Fountain St, Framingham MA 01701, (617) 872-8841.

Circle 461 on inquiry card.
SOFTWARE

PDP-11 Software Information Available

"Real-Time Systems," a new brochure available from Digital Equipment Corporation, describes the hardware and software components of Digital's real-time computing systems based around the PDP-11 family of computers. The publication covers the RT-11, RSX and IAS operating systems, FORTRAN IV, FORTRAN IV-Plus and IAS COBOL high level languages. Also covered is special application oriented software for real-time data acquisition, analysis and reporting in biological and physical science laboratories and process monitor/control situations. The brochure also lists sample configurations ranging from PDP-11V03 to PDP-11/70 systems, laboratory and industrial real-time interfaces, and available supporting services. To obtain a copy, contact Communication Services, Digital Equipment Corporation, 444 Whitney St, Northboro MA 01532.

Circle 503 on inquiry card

New Information for Sphere Owners

If you've been looking for information about the Sphere computer, contact Programma Consultants, 3400 Wilshire Blvd, Los Angeles CA 90010. They offer a free catalog of new software and hardware, plus user group news pertaining to the Sphere. The catalog is arranged in question and answer format, and deals with such topics as the availability of FOCAL, FORTH, APL and cross-compilers for the unit.

Circle 501 on inquiry card

An Assembler/Text Editor for the KIM

Micro Software Specialists have announced their new assembler/text editor package for KIM and TIM computers. Documentation and a hexadecimal object code listing are included. The price is $19.95 for the program in either cassette or paper tape form. Contact Micro Software Specialists, POB 3292, E T Station, Commerce TX 75428.

Circle 502 on inquiry card

A High Level Programming Language for the Motorola Microcomputer

Intermetrics Inc has announced PL/M6800, the first high level programming language for the Motorola M6800 (or AMI 56800) microcomputer. The language is syntactically identical to Intel's PLM.

PL/M6800 has a 1 pass compiler which produces directly loadable object code and listings. The new compiler features a user controlled switch to determine whether the emitted code will be in the AMI or Motorola loader format. Other user controlled features include listings of source code, object code, and assembler code, as well as symbol table dumps.

The new compiler is available via the NCSS timesharing network, or can be purchased directly from Intermetrics for installation on IBM 360 or 370 computers. The purchase price of $1000 includes a tape containing the cross compiler and all library routines, a user's manual, a language reference manual, and product maintenance for one year.

The PL/M6800 compiler is compatible with the PL/M language developed by Intel to program their line of microprocessors. Intermetrics claims to offer "true software portability" in that PL/M6800 is not only "PL/M-like," but is syntactically identical to PL/M.

Information on PL/M6800 is available from PL/M6800 Product Support, Intermetrics Inc, 701 Concord Av, Cambridge MA 02138, (617) 661-1840.

Circle 503 on inquiry card

A Mini Word Processing System

The Software Store has announced its Mini Word Processing system designed to run on Altair equipment under disk extended BASIC, for $150. Mini Word Processing is designed to help the operator generate letters, text, and mailing labels or envelopes. The system consists of seven programs which are driven by a menu select routine. Each program interacts with the operator to establish file names and drive numbers. The options are selected by the yes or no responses to the detailed program prompts. After each function is completed, the system reloads the menu routine.

A user's manual consisting of 51 pages is provided with the system. The manual includes detailed instructions concerning all operator prompts and system error messages, plus a number of examples with test data and programming considerations for custom applications.

Contact The Software Store at 706 Chippewa Sq, Marquette MI 49855, (906) 228-7622.

Circle 504 on inquiry card

Computerized Plotting

Sylvanhill's Lab has announced the availability of 8080 software to control its series of plotters. Approximately 2 K bytes of memory are required. The software may be used in conjunction with application routines available from Micro-Visions Inc, 4926 Travis, Houston TX 77002. The plotters are shipped completely assembled and tested. The user mounts them on the drawing surface and completes the interconnection between the control board and the computer. An 8 bit parallel IO port, and 5 and 24 V power sources are also supplied by the user.

Applications include architectural, mechanical and schematic drawing; printed circuit board artwork; positioning of small objects; computer generated art; games. Sizes available are 11 by 17 inches (27.94 by 43.18 cm) for $750, 22 by 22 inches (43.18 by 55.88 cm) for $895, and 22 by 34 inches (55.88 by 86.36 cm) for $1200.

Contact Sylvanhill's Lab Inc at 1 Sylvanway, POB 239, Stratford MO 65757, (417) 736-2664.

Circle 505 on inquiry card

TEMPOS, a Multitasking Operating System for MITS Computers

Administrative Systems Inc (ASI) has announced its memory resident, multitasking operating system, the TEMPOS Operating System for MITS computers with MITS floppy disks. Up to seven on line users may access the system concurrently, using shared (reentrant) or different tasks. In addition, background tasks are supported as queued processes.

The TEMPOS system supports shared access to data files with a "lock" feature under program control. Extensive file handling capabilities, including user defined logical record length and random access to file, as well as logical record number, are featured.

A command macro feature may be invoked under the TEMPOS system, allowing an unlimited number of macros to be defined and recalled at the system and user program levels. Also, to facilitate debugging, a single step trace feature is included for assembly language programs.

The minimum recommended memory requirement for the TEMPOS multiuser, multitasking operating system, using two disks and three terminals, is 48 K bytes. The price of the TEMPOS system is $1000. For further information contact Administrative Systems Inc, 222 Milwaukee, Suite 102, Denver CO 80206, (303) 321-2473.

Circle 506 on inquiry card
**HEAT SINKS**

- 206-CB Beryllium Copper block finish for TO-5 $3.95
- 206-CB 36H Aluminum for TO-220 Transistors & Regulators $10.35
- 680-75A Black Anodized Aluminum for TO-3 $1.80
- 401-A Black Anodized Aluminum - provided mounting holes for TO-2; 4x1.25 $1.75

**DIP SWITCHES**

- 27 X A-1 4-pole, 1-pole double throw switch $2.95 ea
- 27 X A-1 4-pole, 1-pole double throw switch $1.95 ea

**SCREWBOARDS**

- 3062 Universal Microcomputer Processor Support $3.95 ea
- 22/44 50-pin header socket $2.95 ea
- 8002V Universal Microcomputer Processor Support $19.95 ea

**1/16 VECTOR BOARD**

- 4 new spaces * Present P P P P

**SPLIT-N-WRAP WIRE WRAP TOOL**

- No pre-cutting or stringing
- Comes complete with two 100 ft spools of 28 AWG wire Model P1013 $24.95

**HEXADECIMAL ENCODER 19-KEY PAD**

- ABCDEF
- Return Key
- One key for each period - Key

**63 KEY KEYBOARD**

- $10.95 each

**CONTINENTAL SPECIALTIES**

**PHOTO BOARD SPEEX**

- Upper CS Photo Boards

**PHOTO CLIPS**

- 4 x 5
- 5 x 7
- 12 x 18

**QT PROTO STRIPS**

- MAX-900 BAND PRINTED 5 x 70 DIP 900 LEADS

**TOOLP**

- PERMACEL P-29 PLUS Electrical Tape - All Weather 3/4" x 100 ft
- 2610-8 14" x 100 ft

**MICROPROCESSOR COMPONENTS**

- Z80A CPU $16.00
- Z80A Central Bus Driver $11.50
- Z812 8 Bit Input/Output $320 00
- Z812 Proprietary Interface $10.00
- Z821 Serial Communication $7.95
- Z824 Clock Generator Driver $15.00
- Z82356 8 x 8 ROM $9.50

**EXAR**

- XR 22206A Kit $19.95
- XR 22206A Kit $14.90

**CONNCTORS**

- PRINTED CIRCUIT EDGE-CARD
- 156 Spacing 1mm Double Head-Out
- Bushing Contacts - #024 to #070 P.C. Cards
- MIN TO 25 PIN D-SUBMINATURE

**VECTOR**

- Made to order $25.95 ea
- Enough for up to 15 circuits
- Frequency 1000 to 1200

**CULS**

- 27 X A-1 Connector kit 9 x 1.4 x 1.25

**TOOLING**

- Slit-n-wrap Wire Wrap Tool $24.95

**JE700 CLOCK**

- Dual 1/2 inch LED numbers
- 115 vac

**JE803 PROBE**

- Designed for use with JE700
- Can be used for any kind of probe
- $16.95 each
A 5100 System Mass Storage Device

Users of the IBM 5100 personal computer will appreciate this new addition from an independent vendor. Sykes Datatronics of 375 Orchard St, Rochester NY 14606, (716) 458-8000, showed off this IBM 5100 compatible dual floppy disk subsystem at the NCC show in Dallas TX in June of this year. What it does is give the user a truly random access 3740 compatible diskette hardware subsystem and file management software on 3M cartridges for the 5100. No changes to the 5100 are required, and this subsystem plugs directly into the 5100's serial I/O port. The software provided with this system includes ten BASIC files and 14 APL functions, and allows BASIC programs to communicate with APL programs using files on disk as an intermediary. The price is under $3000 for a single drive system, and under $4000 for dual drive.

Circle 481 on inquiry card

A New Cassette Recorder Interface

Dajen Electronics has announced a new cassette recorder interface with data transmission rates selectable from 800 to 12,000 bps. 12 K bytes of memory can be loaded in approximately 8 seconds. A 1 K byte monitor program is included to provide basic system operations and allow the saving of files. The unit is compatible with the Altair, IMSAI, Kansas City, Polymorphic Systems and Tarbell formats. Kit price is $120; the assembled unit costs $165. The price of the manual is $3.50.

Contact Dajen Electronics at 7214 Springleaf Ct, Citrus Heights CA 95610, (916) 723-1050.

Circle 482 on inquiry card

A Dual Floppy Subsystem

This photo shows the new Sykes Datatronics Series 9000 floppy disk system which is a complete mass storage subsystem with two drives and a built-in 6502 microprocessor controller. The system is offered in the dual drive version illustrated here ($3900) and a single drive version ($2800). All search, blocking, CRC verification and mechanical controls are handled asynchronously by the "smart" 6502-based controller of this device, and data is buffered using FIFO memories. The physical dimensions are table top compatible: 9.7 by 17 by 19 inches (25 by 43 by 48 cm). Hardware interfaces include an optional programmed 10 parallel interface, which will be of interest to homebrewers, as well as detailed interfaces for a variety of microprocessors and minicomputers. Typical interface costs are $300 above the base prices; using the non-IBM format "dual and a half" density recording format, approximately 630,000 bytes can be recorded on each cartridge, making the dual drive on line capacity approximately 1.26 million bytes. Sykes is located at 375 Orchard St, Rochester NY 14606, (716) 458-8000.

Circle 483 on inquiry card

Floppy Disk Drive

According to the manufacturer, General Systems International Inc, 1440 Allec St, Anaheim, CA 92805, (213) 378-9385, this drive uses both sides of the floppy disk recording medium for data as opposed to just one. We can expect to see personal computing systems with on line floppy disk storage capacities on the order of 1.5 million bytes per drive growing out of this type of drive technology. Price of this drive to manufacturers is "in the low $400 range."

Circle 484 on inquiry card

Attention Floppy Disk Correspondents...

A new lightweight mailing envelope for floppy disks which saves 44 to 50 cents per disk in first class postage compared with older corrugated mailers is available from Curtis 1000.

The new envelope accommodates one to five floppy disks with filing sleeves in a lint and dust free environment. Made of DuPont's Tyvek® fiber, the new Curtis 1000 "Disk-O-Mailer" mailing envelope is extremely resistant to tearing and puncturing forces, as well as such dangers to floppy disks as chemicals and wetness. It features fast, dry sealing closure. Its glossy whiteness and green triangles printed along all edges on both sides assure first class handling in the post office just like regular business letters. Retailers and floppy disk software distribution outlets should contact the firm at 1000 Curtis Dr, Smyrna GA 30080, (404) 436-6155.

Circle 485 on inquiry card

248 BYTE November 1977
## MITE COMPUTER PRINTER

Mite 123P Impact printer. Designed for small keyboard printer terminals. 64 characters per line on 8½ inch paper. 75 characters per line, 10 CPS. Printer only, no electronics. With 30 pages documentation. Used, good shape.

Shipping wgt. 18 lbs. $63.00

## VIATRON CASSETTE DECKS

The computer cassette deck alone $35.00

## CONRAC VIDEO MONITOR

Used, checked out. Operates on 115 volts 60 cycle AC. In cabinets as shown. 128 x 40 with bandwidth of 8 Mc. Ideal for computer or TV monitor. Green phosphor display, 9" tube. With data & schematic.

Shipping wgt. 16 lbs. $62.00

## SPECTRA FLAT TWIST

50 conductor, 28 gauge, 7 strands/conductor made by Spectra. Two conductors are paired & twisted and the flat ribbon made up of 25 pairs to give total of 50 conductor. May be peeled off in pairs if desired. Made twisted to cut down on "cross talk." Ideal for sandwiching PC boards allowing flexibility and working on both sides of the boards. Cost originally $13.00/ft

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</thead>
<tbody>
<tr>
<td>SP-324-A</td>
<td>$1.00/ft</td>
<td>10 ft/$9.00</td>
<td></td>
</tr>
<tr>
<td>SP-324-A</td>
<td>$1.00 ft 50 cond. 10 ft/$9.00</td>
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<td>SP-324-B</td>
<td>.90 ft 32 cond. 10 ft/$8.00</td>
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## WIRE WRAP WIRE

TEFZEL blue #30 Reg. price $13.28/100 ft. Our price 100 ft $2.00, 500 ft $7.50.

<table>
<thead>
<tr>
<th>Footage</th>
<th>10'</th>
<th>50'</th>
<th>100'</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 Cond.</td>
<td>#24</td>
<td>$2.50</td>
<td>9.00</td>
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<tr>
<td>12</td>
<td>22</td>
<td>3.00</td>
<td>11.00</td>
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<tr>
<td>14</td>
<td>22</td>
<td>3.50</td>
<td>13.00</td>
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<tr>
<td>24</td>
<td>#24</td>
<td>5.00</td>
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<td>7.50</td>
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Great savings as these are about 1/4 book prices. All fresh & new.

## MULTI COLORED SPECTRA WIRE

Footage 10' 50' 100'

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<thead>
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<th>12</th>
<th>14</th>
<th>24</th>
<th>29</th>
</tr>
</thead>
<tbody>
<tr>
<td>10'</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>#24</td>
<td>22</td>
</tr>
<tr>
<td>50'</td>
<td>3.00</td>
<td>3.50</td>
<td>3.50</td>
<td>5.00</td>
<td>7.50</td>
</tr>
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## TOUCHTONE ENCODER CHIP

Compatible with Bell system, no crystal required. Ideal for repeaters & w/specs.

$6.00

## CHARACTER GENERATOR CHIP

Memory is 512x5 produces 64 five by seven ASCII characters. New material w/data

$6.00

Please add shipping cost on above. Minimum order $10

FREE CATALOG NOW READY

P.O. Box 62, E. Lynn, Massachusetts 01904

Circle 83 on inquiry card.
PERIPHERALS

What's New?

Do You Want to Draw Pictures on Your Display?

Users of personal computers who are interested in graphics input will find this new peripheral of great interest, and at a price which makes it attractive for personal use. Scientific Accessories Corporation, 970 Kings Highway W, Southport CT 06490, (203) 253-1526, has introduced the Model GP-101 sonic digitizer for a single unit price of $800. What you get is a stylus with or without ink or a cursor, an electronics package, and the L-frame sensor seen in this photo. It is intended to be used in any situation where input of XY position data is required. Typically, a computer oriented artist might make a rough sketch of graphic display information on paper and then trace the outline of the figure with the stylus after positioning the rough within range of the sensors. The artistic digitization could also be done interactively with the display in a freehand mode.

To use this device, some additional logic and timing circuitry will be required since the basic electronics simply produces TTL level signals which have a known start edge time and a variable delay time representing the X and Y distances to the stylus or cursor unit. The user must also provide power supplies and custom software to analyze the signals for particular purposes.  

Sargent's New Altair (S-100)

Prototype Board

Sargent's Distributing Company, 4209 Knoxville, Lakewood CA 90713, has introduced this new Altair (S-100) bus prototype board. The board is constructed of epoxy G-10 material. There is space for four 7805 type voltage regulators. It accommodates 14, 16, 18, 24 and 40 pin wire wrap sockets with room for a maximum of forty-eight 14 or 16 pin sockets. Also available is a complete set of plans for a S-100 bus compatible front panel and bootstrap system which it features direct parallel ASCII keyboard input, one additional parallel input port, and two parallel output ports. This design uses PROMs for instant turn on and reset. Start cassette tape and your system is fully loaded and running in about 30 seconds, and can be wire wrapped using the prototyping board. Price of the prototype card is only $25 postpaid; the plan set is $7.50 postpaid; and a complete kit of all parts for the front panel design is $79.95 postpaid. 

A New Model Self-Scan from Burroughs

The Electronic Components Division of Burroughs Corporation, POB 1226, Plainfield NJ 07061, has introduced this new single line 40 character version of Self-Scan II technology, intended for use in any product where a limited size alphanumeric display is required. Special effects include left or right data entry, moving message effects, blinking subfields within the 40 character line, etc. Self-Scan is a registered trademark of Burroughs Corporation.

Centronics Introduces High Speed Microprinter

Centronics Data Computer Corporation has announced a high speed compact microprinter called the Mini-1 for $595. Aimed at the home, hobby and microprocessor markets, the 240 character per second Mini-1 is offered as a complete unit including case, power supply, 96 character ASCII generator and interface, paper roll holder, low paper detector, bell, and multiline asynchronous input buffer.

The microprinter produces copy on aluminum coated paper by discharging an electric arc to penetrate the coating, which is less than one micron thick. Toners and ribbons are not required.

The printed characters are said to be impervious to light, temperature and humidity. The machine prints 180 lines per minute on 4 3/4 inch roll paper in 20, 40 or 80 column widths, selectable by the user. The special aluminum coated paper used by the unit costs nominally more than standard paper.

This is an excellent way to get acceptably high speed listings at relatively low prices. Contact Centronics Data Computer Corporation, Hudson NH 03051, (603) 883-0111.

A 60 Character per Second Printer

The Altair C700 from MITS is a 60 character per second serial printer using a 5 by 7 dot matrix and the 64 character ASCII subset. The unit is designed to be interfaced to the Altair 8800 computer and features automatic motor control, paper runaway inhibitor and automatic line feed after carriage return. The printer is bidirectional and can print 26 132 column lines per minute. It can accommodate 15 inch wide forms.

Dimensions are 7 by 28 by 24.5 inches (17.8 by 63.5 by 62.2 cm). Contact MITS, 2450 Alamo SE, Albuquerque NM 87106.
Now low-cost memory stacks up in reliability!

Introducing a new generation of ECONORAM dynamics with SynchroFresh reliability

Meet ECONORAM* III with SynchroFresh™, the 8Kx8 dynamic memory for S-100 bus computers that really works. And uses less than half the power of static designs. And costs just $149 for an assembled 8K.

Unlike previous attempts at building a low-cost dynamic memory, ECONORAM* III is entirely reliable because of SynchroFresh™, a new approach to memory refresh that is simple, elegant and totally effective.

SynchroFresh™ was invented by George Morrow, designer of the original ECONORAM*. Instead of arbitrarily interrupting your CPU to perform memory refresh cycles, Morrow designed SynchroFresh™ to weave refresh invisibly into the natural timing of the S-100 bus. SynchroFresh™ circuitry simply monitors your computer's machine states, utilizing all of the normal opportunities for memory refresh. It's that simple.

And simplicity means reliability and dramatically lower cost. That's why a SynchroFresh™ design was chosen for the first ECONORAM* dynamic, to follow in the footsteps of the largest-selling static memories for personal computers.

ECONORAM* III with SynchroFresh™ is an 8Kx8 dynamic board, configured as two individually addressable 4K blocks for flexibility. It is available assembled, tested and warranteed for one full year for just $149. This unprecedented warrantee offers a full refund of purchase price if ECONORAM* III does not run reliably with your S-100 CPU—evidence of our confidence in its performance.

It is also available as a kit with complete assembly instructions and documentation for $159. ECONORAM* III with SynchroFresh™ in assembled or kit form, may be ordered directly from Thinker-Toys™. Write 1201 10th Street, Berkeley CA 94710 or call (415) 527-7548. Call BAC/MC orders toll-free to 800-648-5311. Or ask your computer store to order it for you.

NEW LOW PRICE

$149
8K assembled, tested, warranteed
1 year

A product of Morrow's Micro-Stuff for

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*ECONORAM is a trademark of Godbout Electronics.
Apple II Features Built-in Color Capability

The Apple II is Apple Computer Inc.'s entry in the home computer market. The unit uses the MOS Technology 6502 processor and can display alphanumeric characters and video graphics in 15 colors using any standard color television set.

A BASIC language package is permanently stored in 6 K bytes of read only memory; execution speed is fast enough to run many video games. The integer BASIC language includes special functions related to color video display programming.

In both the color graphics mode and in the high resolution graphics mode, four lines of text may be optionally displayed at the bottom of the screen to annotate displays. The Apple II also features a built-in cassette interface.

Minimum memory configuration available includes 4 K bytes of programmable memory and 8 K bytes of read only memory. A 2 K byte monitor provides debug commands, a mini-assembler, disassembler, floating point package and software-simulated 16 bit arithmetic capability.

The unit comes complete with a switching power supply which requires no fan. The computer is housed in a plastic case with dimensions of 18 by 15.25 by 4.5 inches (45.72 by 38.74 by 11.42 cm). It comes with two game paddles and a demonstration cassette for $1298. It is also available in board only form, without case, keyboard, power supply or accessories for $598.

Contact: Apple Computer Inc, 20863 Stevens Creek Blvd., Bldg B3-C, Cupertino CA 95014.
Circular 512 on inquiry card

An Altair Bus Compatible Music Board

Newtech Computer Systems' Model 6 Music Board is designed to enable experimenters having Altair (S-100) bus computers to produce music and sound effects. Applications include generating melodies, rhythms, sound effects, Morse code and touch tone synthesis.

The Music Board comes assembled and tested. Features include selectable output port addresses, a latched 6 bit digital to analog converter, audio amplifier, speaker, volume control and RCA phone jack for connection to external audio systems. It employs a glass epoxy printed circuit board with plated through holes and gold plated fingers.

A user's manual, which is supplied with the board, includes a BASIC language program for writing musical scores and an 8080 assembly language routine for playing them. The price is $59.95. Contact: Newtech Computer Systems Inc, 131 Jeralean St, Brooklyn NY 11201, (212) 625-6220.
Circular 515 on inquiry card

A CT-1024 Scroll Mod

Lenwood Computer Systems, POB 67, Hiawatha IA 52233, has announced a modification to Southwest Technical Products Corporation’s CT-1024 terminal product. The Model SM-2 scrolling modification board is available at $19 plus $1.50 postage and handling, and converts the CT-1024 style display from a page oriented display to a scrolling display. The photo shows the board mounted on the CT-1024 main board using a stand off stud.

Circular 514 on inquiry card.

Infoton, Second Av., Burlington MA 01803, (617)272-6660, has introduced this pair of video terminal products. The Model 200 is the low end version, a Teletype replacement with multiple additional features and 80 character by 24 line display. The Model 400 is a model with more features, including upper and lower case display, additional keyboard functions, etc. Both models feature RS-232C, 20 mA current loop and 60 mA current loop serial interfaces at 16 switch selected data rates to 19,200 bits per second. No price was given in the documentation from which this note was abstracted.
Circular 515 on inquiry card

Several Gimix for the SwTPC 6800 Bus

We received a sales brochure for three products available from Gimix Inc, 1337 W 37th Pl, Chicago IL 60609, (312) 927-5510, which plug directly into the Southwest Technical Products Corporation's 68000 bus. One of these products is a $119 read only memory board which holds up to 8 K of 2708 EROM parts (not supplied), and can be placed on any even 8 K memory address boundary (ie: 0000, 2000, 4000, 6000, 8000, A000, C000, or E000) using switches. A second product is a $25 extender board for use when troubleshooting or debugging a prototype card. The third product is a video output board which contains a 1 K by 8 bit volatile programmable memory region which can be connected at any 1 K boundary in memory address space using jumpers. This $249 generator can be set up for 16 lines of 32 characters or 16 lines of 64 characters; output is EIA video with adjustable "density" and left-hand margin. These products are fully assembled.
Circular 516 on inquiry card

PERIPHERALS
NOW-THE ULTIMATE RAM BOARD
32K FOR $427.

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Memory Write Protection
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PC board comes with sockets for 32K operation
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BUY AN $100 COMPATIBLE 8K RAM BOARD AND UPGRADE
THE SAME BOARD TO A MAXIMUM OF 32K IN STEPS OF
8K. MERELY PURCHASE YOUR ADDITIONAL RAM CHIPS FROM S.D. SALES AT A GUARANTEED PRICE.
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Board fully assembled and tested for $50.00 extra.

8K FOR $139.

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Z-80 CPU BOARD KIT Complete Kit

FEATURES
- Litronix dual 1/2" displays
- Single I/O segment driver
- SCR digit drivers
- Greatly simplified construction.
- More reliable and easier to build.
- Kit includes all necessary parts (except PC board & Xfer optional). Eliminate the hassle - avoid the confusion with Non Alarm kits sold by our competition!

P.C. Board and all parts (less Case) included
Alarm option - $1.50
AC FKMFR - $1.50

$139.

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MUSICAL HORN
ONE TUNE SUPPLIED WITH EACH KIT. ADDITIONAL TUNES - $5.00 EACH
SPECIAL TUNES AVAILABLE - YOU SUPPLY THE SHEET MUSIC
WE SUPPLY PROGRAMMED FROM YOU PROPER TUNES TO
- DIXIE - EYES OF TEXAS - ON WISCONSIN - YANKEE DOODLE DANDY - NOTRE DAME FIGHT SONG - PINK PANER - AGGIE WAR SONG - ANCHORS AWAY - NEVER ON SUNDAY - BRIDGE OVER RIVER WAHU
CAR & BOAT KIT
HOME KIT
$34.95
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ROM'S

- Z-80 included manual.
- Z-80A included manual.

- $9.95 KIT

SUCCESSFUL MUSICAL HORN BUILT INTO THE BOARD

- FEATURES
- Litronix dual 1/2" displays
- Single I/O segment driver
- SCR digit drivers
- Greatly simplified construction.
- More reliable and easier to build.
- Kit includes all necessary parts (except PC board & Xfer optional). Eliminate the hassle - avoid the confusion with Non Alarm kits sold by our competition!

P.C. Board and all parts (less Case) included
Alarm option - $1.50
AC FKMFR - $1.50

$139.

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JUMBO LED CLOCK KIT
FEATURES
- A Bowman Jumbo 5 inch LED array.
- MOSTEK - 50250 Super Clock Chip
- On board precision crystal time base
- D.C. or 24 hour Real Time Format.
- Perfect for cars, boats, vans, etc.
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New Terminal from TEI

TEI Inc. of Houston TX has announced a new processor terminal. Designated the Model MCS-PT, the unit is a self-contained computer system with display and disk storage, keyboard, and a 12 slot motherboard. It may be used either as a stand alone processor or as a processor terminal in a larger system.

Features include a 15 inch (38.1 cm) high resolution video monitor with a full upper and lower case ASCII character set keyboard, eight user designated special function keys, and a 16 key numeric cluster pad. A 3 meg 5A-400 mini-floppy disk drive is standard.

The 12 slot mainframe contains a processor board featuring an 8080 processor and a special circuit that implements a start up "jump to" routine to any user selected memory address. 16 K bytes of programmable memory is provided with additional capacity available as an option. The disk controller (which can handle up to four drives) and the video board are also standard. The IO board provides three parallel and three serial ports with selectable data rates of 75 to 19,200 bps. RS-232C or TTL interfaces are provided. Power is provided by a constant voltage transformer (CVT) power supply.

Software provided includes a CP/M disk operating system and BASIC on disk. The processor terminal is $3495, fully assembled and tested. The kit is $2995. The unit without the disk drive and controller is $2495 assembled, or $2195 in kit form.

Contact Bill R Tatroe, CMC Marketing Corp, 7231 Fondren Rd, Houston TX 77036, or call (713) 774-9526.●

Circle 495 on inquiry card.

NEC "Spinwriter" Technology

The latest in a series of low inertia spinning plastic font impact printers to come to our attention is this NEC Information Systems "Spinwriter" terminal, intended for commercial markets. This terminal comes with a choice of five standard interfaces, 10 or 12 characters per inch spacing (4 or 4.7 characters per cm), ASCII character codes, and a variety of plastic "thimble print mechanism" fonts for different type faces. The typing elements are rated at over three million impressions per character. No pricing information was given in the press release, other than the vague comment "10% below most competitive printers." If past experience is any guide this means a price above $3000 in unit quantities. Deliveries of this printer begin in October 1977 and are expected to be 60 days after receipt of orders thereafter. NEC Information Systems is located in Lexington MA.●

Circle 496 on inquiry card.

A Selectric Interface for Microcomputers

The latest in a series of low inertia spinning plastic font impact printers to come to our attention is this NEC Information Systems "Spinwriter" terminal, intended for commercial markets. This terminal comes with a choice of five standard interfaces, 10 or 12 characters per inch spacing (4 or 4.7 characters per cm), ASCII character codes, and a variety of plastic "thimble print mechanism" fonts for different type faces. The typing elements are rated at over three million impressions per character. No pricing information was given in the press release, other than the vague comment "10% below most competitive printers." If past experience is any guide this means a price above $3000 in unit quantities. Deliveries of this printer begin in October 1977 and are expected to be 60 days after receipt of orders thereafter. NEC Information Systems is located in Lexington MA.●

Circle 497 on inquiry card.

Video Display Memory Board for LSI-11 Systems

Computer Technology, 6043 Lawton Av, Oakland CA 94618, (415) 451-7145, has introduced a board which plugs into the LSI-11 bus of Digital Equipment Corporation, and creates a video display peripheral which features 16 lines of 64 ASCII characters accessed as a 1 K byte region of memory address space. According to the information received here, the board fits into one dual width half slot segment of the LSI-11 backplane and requires only +5 V and +12 V power supplies. Output is EIA RS-170 composite video (2 volts peak to peak, negative sync) mA matched to 75 ohm coaxial cable. The photo shows a typical display on a video monitor. Individuals using LSI-11 systems may find this to be quite a useful addition to memory address space.●

Circle 498 on inquiry card.

A New Desktop Teleprinter Terminal for APL Users

Designed to meet the special character set requirements of APL users, the newly announced Anderson Jacobson A1 860/A desktop Teleprinter terminal produces both an APL character set and a high resolution ASCII character set. Using a 9 wire dot matrix printer mechanism, the A1 860/A prints each 9 by 5 character in a 9 by 12 character cell. The APL character set includes all of the standard APL overstrike characters, while the ASCII character set includes lower case, underscore and selectable double wide characters. Alternate selection of either the 128 code APL character set or the 128 code ASCII character set is done from the keyboard or remotely by code selection.

Standard features include operator selectable speeds of 10, 30, 45 or 60 cps, horizontal and vertical tabulation, reverse line feed, autopagination, dual gate forms tractor, self-test diagnostics, and a 350 character receive-only buffer with buffer overflow protection. Single unit purchase price is $3285 from Anderson Jacobson, 521 Charcot Av, San Jose CA 95131, (408)263-8520.●

Circle 499 on inquiry card.
NEW COMPUTER INTERFACE BOARD KIT
Our new computer kit allows you to interface serial TTL to RS 232 and RS 232 to TTL. There are four of these supplied with the kit, so you can run up to four devices on one TTL or four separate TTL to RS 232 devices.
Typical use: You can use your computer ports to run an RS 232 printer, video terminal and two other RS 232 devices at once, without constantly connecting and disconnecting your terminals.

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GENERAL PURPOSE COMPUTER POWER SUPPLY KIT
This power supply kit features a high frequency torroid transformer with switching transistors in order to save space and weight. 115V 60 cycle primary. The outputs with local regulators are 5V to 10A, in one amp increments, –5V at 1A, ±12V at 1A regulators supplied 6 340T-5 supplied.

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This memory board may be used with the F8 and with minor modifications may be used with KIM-1/4up.
32-2102-1 static RAM's, 16 address lines, 8 data lines in, 8 data lines out, all buffered. On-board decoding for any 4 of 64 pages, standard 44 pin, .156" buss.

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A fantastic bargain for only with the following features:
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